R30

5MPix, 30fps CMOS Image Sensor with very low temporal line noise

G.G. Storm, M.D. Purcell, J. K Moore, M. Wigley, D. Tolmie, L.A Grant
STMicroelectronics Imaging Division, 33 Pinkhill, Edinburgh, EH12 7BF.
Email: Graeme.Storm@st.com
Tel: +44 (0) 131 3366233
Fax: +44 (0) 131 3366001

1. Introduction

Temporal noise in a CMOS Image Sesnor(CIS) is a commonly reported upon subject[1] with the vast majority of works discussing the noise of single pixels in the resultant image. Far less correspondence is found detailing the temporal noise which is common to a row or column in the final image. This is certainly not because the noise is less important, in fact the contrary is true: row or column noise is more visible to the human eye and needs to be in the order of ten times lower than the random noise of the pixel to prevent it being visible[2].

The most common CIS architecture addresses all pixels of a row at the same time and reads their data out in a column parallel fashion. The pixel readout is column parallel even if the ADC is not. Thus pixels addressed and readout at the same time will contain noise from signals that are common to the row. In contrast, pixels from the same column are addressed and readout at different points in time, de-correlating the noise associated with readout.

This paper presents a CIS with very low line based noise, well below 1/10th of the pixel temporal noise. Although the temporal line noise is discussed in more detail, HFPN is also reported since the final image requires both these levels to be low. The device achieves low temporal line noise through both architecture choice and design of pixel, pixel regulators and column ADC. In particular it shows effective reduction of temporal line noise using a S/H technique in a pixel regulator.

2. Architecture

The device presented is a 5MPix CMOS Image sensor using 1.4um pixel pitch. Four photodiodes are shared between a single sense node to give an average 1.75 transistors/pixel(1T75)[3]. The device operates with a line time of just under 16.5µs to achieve a frame rate of 30fps.

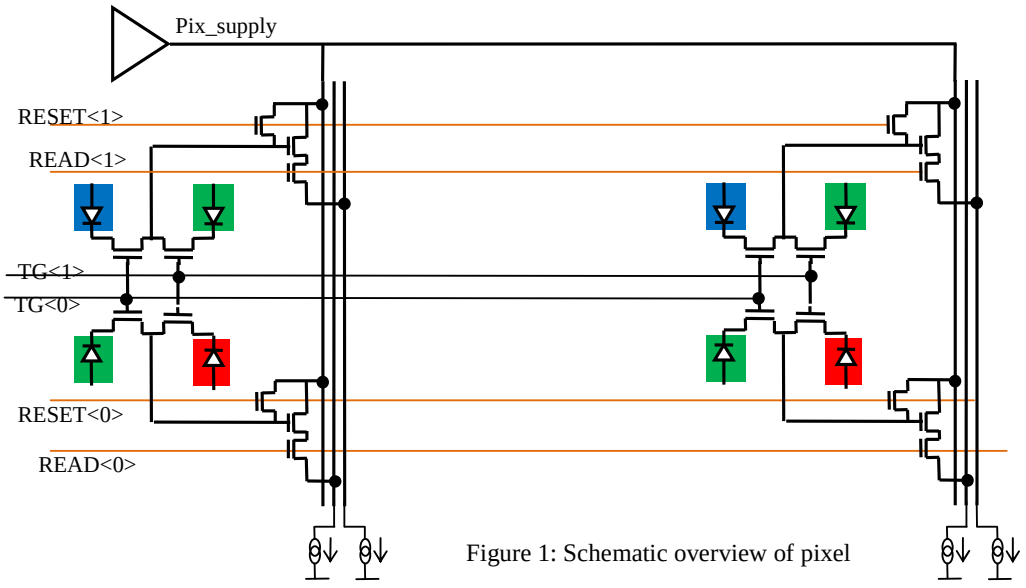

Figure 1: Schematic overview of pixel

The pixel architecture as mentioned is 1T75. As can be seen from Figure 1, the activation of a single TG line does not access all the pixels of a single row. Thus a pixel row in the final re-ordered image

will have pixels readout at two different times with un-correlated line noise. The re-ordering of data has been implemented elsewhere as a means of reducing VFPN[4]. As shown in Table 1 the 1T75 pixel architecture and re-ordering has been measured to reduce the temporal line noise by around 20%.

The reduction measured is applicable to a monochrome sensor. The final line noise in a colourised image will be dependent on the interpolation algorithm applied.

3. Pixel regulator

There are a number of signals common to a row of pixels (TG, READ, RESET, Pix_supply), plus the column current sources. The pixel supply was identified to be limiting the temporal line noise thus a modified regulator design with S/H stage was implemented. The regulator is split into two stages, as shown in Figure 2, with the second stage being a low noise output stage realised with a NMOS source follower. The sample switch is opened prior to the pixel settling to the black or reset level. This samples the thermal noise from the first stage of the regulator and the reference voltage so that it is common to both periods of the CDS operation.

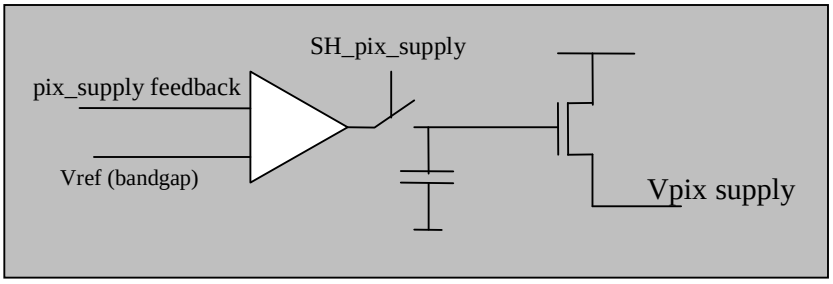

Figure 2: Pixel supply regulator including S/H between first and output stages

When the S/H switch in the pix_supply regulator is opened there is a shift in the pix_supply voltage due to sampling operation. Charge injection, clock feed-through, and thermal noise will all contribute to this voltage shift and needs to be considered with respect to:

1. the acceptable variation in common mode of pix_supply to prevent variation in pixel response.
2. the time for the 1st stage amplifier to settle when it is again connected to the output stage.

The timing is shown in Figure 3. The SH_pix_supply is shown to be low for the majority of the line time due to the ADC operating without a column sample and hold. The regulator noise is thus required to be held until the end of the ADC conversion. The line noise improvement measured using the S/H within the pixel supply regulator is shown in Table 1. It can be seen that the temporal line noise is reduced by almost 50% (from 0.72codes to 0.41 codes).

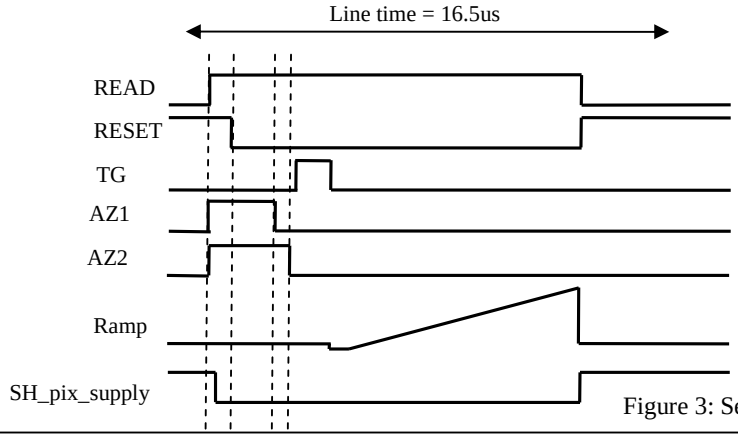

Figure 3: Sensor timing

4. ADC

As mentioned, and shown in Figure 4, the single slope ADC operates on the column voltage which is continually driven from the pixel for the duration of the conversion [5]. Noise sources common to all ADCs need to be considered carefully to ensure the readout circuitry does not introduce line noise. Bias voltages for current sources are such signals common to all ADCs in the readout. To minimise their impact, the first comparator stage is designed to be differential.

Measurement of only the ADC line noise is performed by grounding the pixel column line since the input of the ADC is AC coupled. In this configuration the temporal line noise contribution of the ADC was measured to be 0.15codes.

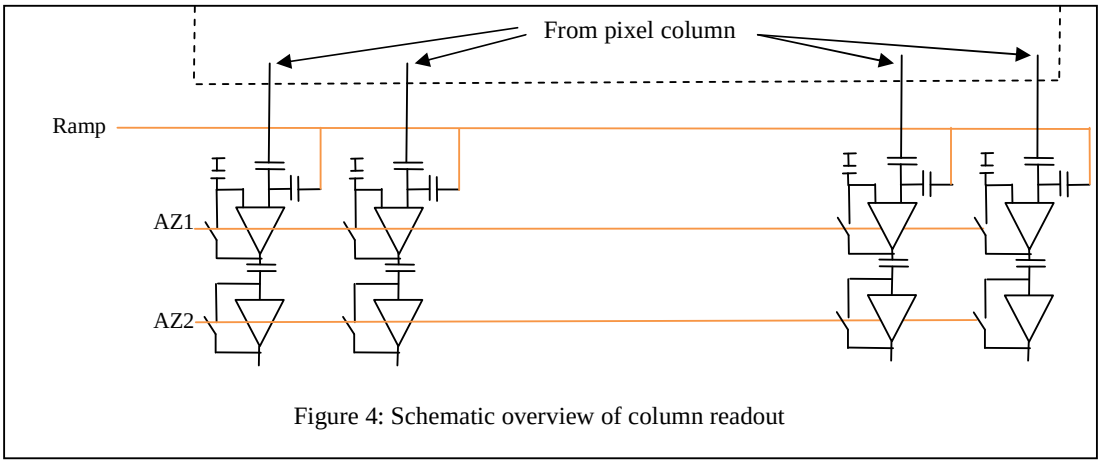

Figure 4: Schematic overview of column readout

In addition to the low noise design of the comparator the continuous time (CT) architecture itself was compared with a column S/H scheme with regard to temporal line noise. Considering the timing of a column S/H operation, all pixel and column noise sources are sampled at the same time and are thus stored with the data for every pixel in the row. For the CT architecture, any noise on the pixel signal lines is continually modulating the column voltages and thus the input to the ADC. It was investigated if the pixel noise would cause sufficient spread in the comparator flip point to de-correlate some of the line noise.

Measurements were made operating the device in a test S/H mode where a sample capacitor is connected to the pixel column lines at the input of the ADC. The results are plotted in Figure 5 against the clock frequency of the device. Also plotted is 1/10th of the pixel noise measured. Although the line noise using a column S/H operation was slightly higher than the equivalent CT measurement the difference was not significant.

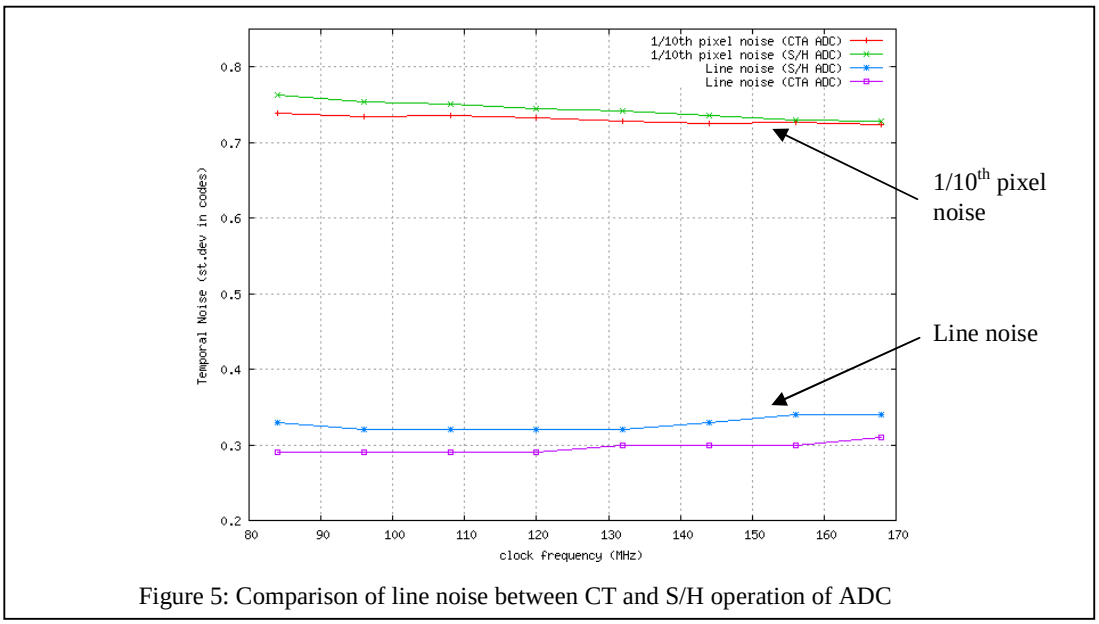

Figure 5: Comparison of line noise between CT and S/H operation of ADC

Sensor parameters and measured results are shown in Table 1. For temporal line noise measurements the value quoted is:

$$Temporal\ Line\ noise = \frac{st.dev\ of\ row\ averages\ of\ the\ difference\ of\ two\ frames}{\sqrt{2}}$$

where the frames are taken in the dark with zero exposure.

It should be noted that this measurement method becomes limited for reduced resolution sensors since the reduction in pixel noise is given by √ (# of columns in pixel array). In this instance the pixel temporal noise is reduced by approx. 50 from 7.9codes to 0.15codes.

Parameter	Value
Pixel size	1.4um
Array resolution	2600x1952
Measurement (analogue Gain16)	
Volts/code	29.2µV/code
Pixel temporal noise	7.9codes
Temporal Line noise (pixel re-ordering disabled, S/H in pix_supply regulator enabled) (pixel re-ordering enabled, S/H in pix_supply regulator disabled) (pixel re-ordering disabled, S/H in pix_supply regulator disabled) (ADC only, column grounded)	0.32codes (0.41codes) (0.55codes) (0.72codes) (0.15codes)
HFPN	0.14codes

Table1: Sensor parameters and measurements

5. Conclusion

A 5MPix CIS with low temporal line noise has been presented. Pixel architecture, pixel supply generation and ADC design all contribute to achieving the final line noise of less than 1/20th of the pixel noise. Such design will allow reduction of the pixel temporal noise without negatively impacting the perceived image quality.

References

1. Shoji Kawahito, “Noise at the circuit level”, 2007 IEEE ISSCC Forum: Noise in Imaging Systems, San Francisco, Feb.2007
2. Rick Baer, “Noise at the system level”, 2007 IEEE ISSCC Forum: Noise in Imaging Systems, San Francisco, Feb.2007
3. M. Mori, M. Katsuno, S. SKasuga, T. Murata, T. Yamaguchi, “A 1/4in 2M Pixel CMOS Image Sensor with 1.75Transistor/Pixel”, in IEEE ISSC Dig. Tech Papers, pp110-111, Feb 2004.
4. M.F. Snoeij, A.J.P Theuwissen, K.A.A.Makinwa, J.H. Huijsing, “A CMOS Imager With Column-Level ADC Using Dynamic Column Fixed-Pattern Noise Reduction”, IEEE Journal of Solid-State Circuits, Vol41, No.12, 2006
5. G.G. Storm, M.D. Purcell, A. Laflaquiere R.A. Elliott, L.A. Grant, T.Lule, F. Mutze, M.Sommer, “Continuous Time Column Parallel Readout for CMOS Image Sensor”, International Image Sensor Workshop 2007, Maine, USA