# Dark fixed pattern noise generation by Negative-Bias-Temperature (NBT) stress on CMOS imager pixel transfer gate

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#### Introduction

Negative bias on transfer gate is an efficient way to reduce dark current by Shockley-Read-Hall (SRH) mechanism generated via Si-SiO2 interface states at a transfer gate channel [1] [2] [3]. But it has also been reported that lower negative gate bias increases dark current noise, such as dark current generated bv Gate-Induced-Leak (GIL) Trap-Assisted-Tunneling (TAT) mechanisms [2] [3] [4] [5], thus setting appropriate negative gate bias is an important issue to avoid additional noise generation. This contribution reports newly discovered dark Fixed-Pattern-Noise (FPN) generation caused by Negative-Bias-Temperature (NBT) stress on transfer gate. The dark FPN has similar behavior to Vth shift after NBT stress usually observed in p-type MOS-FET [6][7][8]. The dark FPN dependency on stress condition was investigated with test pixel array AC operation, and the root cause model of the dark FPN is proposed.

## Test Procedure

The test pixel array with 1.75um pitch 2-way shared pixel was used for the dark FPN measurements. The pixel schematic used in the test pixel array is shown in Figure 1. The negative gate bias is applied from external power supply. The pixel raw data are taken after the on-chip Correlate Double Sampling (CDS) circuitry and Analog to Digital Converter (ADC). Operational timing is controlled by an on-chip timing controller. Sensor chip temperature is varied by controlling the test chip atmosphere temperature. The dark image analysis is done after averaging 10 dark images so that a temporal noise in dark image can be minimized.

## **Experimental Results**

Figure 2 compares dark signal distribution before NBT stress to dark signal distribution after NBT stress. The NBT stress applied is -2.5V negative gate bias, 60  $^{\circ}$ C temperature, and 30 minutes stress time. Dark signal distribution was taken by normal dark image readout operation with -1.5V negative gate bias as a transfer gate low level. As shown in Figure 2, the dark signal distribution tail in lower dark signal level is slightly varied after NBT stress is applied. Figure 3 shows dark image from test pixel array after NBT stress. Darker pixels, which appear to be black defects, generated by NBT stress are observed. It also is observed that dark distribution shift is more obvious when negative gate bias is lower or temperature is higher. In order to see the dark distribution shift behavior is caused the similar mechanisms with ordinary bv pMOS-FET Vth shift after NBT stress, dynamic behavior of off-stress dark signal distribution right after the NBT stress is observed. Figure 4 shows dark signal distribution recovery after NBT stress. Fast recovery of dark distribution (about ~50% of dark level shift) is observed as is often observed in pMOS-FET Vth shift after NBT stress. This result

suggests that the root cause of the dark FPN generation has similar mechanisms to that of pMOS-FET Vth shift after NBT stress. Figure 5 shows black defect probability dependency both on negative gate bias and on temperature. BT stress time is 30 minutes. As shown in Figure 5, Black defect probability is 0 when stress bias is -1.5V but increases when stress bias is lower than -1.5V, especially when temperature is higher than 60  $^{\circ}$ C. The proposed mechanism of black defect generation by NBT stress is shown in Figure 6. Since the dark FPN dependency on NBT stress and the dark FPN dynamic recovery behavior after NBT stress are similar to those of the ordinary pMOS-FET Negative Bias Temperature instability (NBTI), root cause of the dark FPN is probably similar to that of the pMOS-FET NBTI. Key phenomenon is the interaction of accumulated holes with Si-SiO2 interface. During NBT stress, accumulated holes and H atoms terminating Si dangling bond react and generate interface states[6][7][8]. Reaction products are captured in gate dielectric and produce positive fixed charge. The positive fixed charge generates potential pockets in a transfer gate channel. After the NBT stress, when dark electrons accumulated in photo-diode are readout while transfer gate is ON, a part of dark electrons are captured in the potential pocket and then recombine with accumulated holes via generated interface states when transfer gate goes OFF. In order to see the transfer gate Si-SiO2 surface has a critical role in the dark FPN generation, dark signal distribution dependency on negative gate bias is compared between before NBT stress and after NBT stress. Figure 7 compares dark signal cumulative distribution before NBT stress and after stress. The NBT stress are -3.5V negative gate bias, 30  $^{\circ}$ C temperature, and 30 minutes stress time. Dark current increase is observed after NBT stress when negative gate bias is -0.8V, whereas less dark current increase is observed after NBT stress

when negative bias is -1.5V. The results indicate that the number of interface states at transfer gate channel is increased by NBT stress, and dark current with SRH mechanism is increased via generated interface states. It can be concluded that NBT stress on transfer gate generates electron trap level at transfer gate channel and produce dark FPN, if NBT stress with large negative bias with high temperature is used.

## Conclusion

Dark FPN generation caused by NBT stress was found. Cause analysis of the dark FPN was investigated with test pixel array AC operation, and the root cause model of the dark FPN is proposed. The proposed root cause for the dark FPN is the generation of interface states by interaction of accumulated holes with Si-SiO2 interface, as is often observed in pMOS-FET NBTI.

## References

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<u>Figure 2</u> Dark signal distributions comparison between before and after NBT stress. NBT stress are -2.5V negative gate bias and 60 °C temperature, and stress time is 30 minutes. Dark signal distributions are taken with Vxfer=-1.5V and with 30 degree temperature. (a) Dark histogram, (b) Enlarged dark histogram.



<u>Figure 3</u> Enlarged dark image taken after NBT stress. Circles show black defect pixel.



<u>Figure 4</u> Dynamic behavior of off-stress dark distribution right after NBT stress. NBT stress are Vxfer=-2.5V, Temperature is 60degree, and stress time is 30minutes.



<u>Figure 5</u> Black defect probability dependencies on negative gate bias and on temperature. Stress time is 30 minutes. Dark signal distributions are taken with Vxfer=-1.5V and with 30 degree temperature.





Figure 7 Dark signal cumulative distribution comparison between before and after stress. NBT stress are Vxfer=-3.5V and 35 °C temperature, and stress time is 30 minutes. Dark signal distributions are taken with Vxfer=-1.5V and with 30 degree temperature. Obvious change of dark signal distribution is observed after NBT stress when dark signal distribution is taken with Vxfer=-0.8V.