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Experimental Comparison of Four Different CMOS Pixel Architectures Used in Indirect Time-of-Flight Distance Measurement Sensors

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Abstract— **Four different pixel architectures to be used in CMOS based indirect time-of-flight (ToF) rangers were designed, fabricated and characterised. The measured results are presented here for their direct comparison. Sharing a very similar, yet case optimised readout circuitry in each case, three fabricated CMOS rangers were based respectively on a pinned photodiode (PPD), a photogate, and a newly developed CMOS intrinsic lateral drift-field photodiode (LDPD), having a 40µm pixel pitch in each case, and finally compared to the pixel configuration based on a CMOS standard *n*-well based photodiode (PD). In all four cases, ranging is based on pulsed laser illumination and indirect time-of-flight measurements.**

I. INTRODUCTION

In our approach, a scannerless 3D scene reconstruction based on indirect time-of-flight (ToF) principle relies on measurements of the time elapsed between the moment in which a light signal, actively modulated as a 905nm wavelength laser pulse and widened by a special diffusing lens to cover an entire scene, is sent by a laser source, and a moment at which, after being reflected by different objects in a scene, it impinges at the photosensor usually collocated aside this laser source. The indirect ToF measurement utilizes the integration of the photogenerated charge during an ultra short shutter time. For example, for d_{max}=4.5m distance measurements, T_{pulse}=30ns laser pulse lengths are required, as it can be deduced from Eq. (1) [1], which defines the basic indirect ToF measurement principle, c being here the speed of light.

$$d_{\max} = \frac{c}{2} \cdot T_{pulse} \qquad (1)$$

The range resolution Δd delivered in ToF measurements is, as it can be concluded from Eq. (2) [2], directly proportional to the equivalent noise charge (ENC) - a noise floor defining the minimum amount of detectable signal charge in the pixel - and indirectly proportional to the wavelength dependent optical sensitivity $S(\lambda)$ (in A/W) and the impinging irradiance value E_R (in W/m^2). In Eq. (2) [1], q stands for the elementary charge.

$$\Delta d = \frac{c \cdot q \cdot ENC}{2 \cdot S(\lambda) \cdot A_{Ph} \cdot E_R} \qquad (2)$$

For a 4.5m distance, it is common that the reflected laser pulses have an impinging irradiance value deep below 100W/m^2, depending on the reflectivity of the object. At the same time, the background illumination may as much charge as the laser pulse. So, an in-pixel background illumination suppression is required. The full-well capacity (FWC) of the pixel must be high enough to deal with sometimes huge amounts of total generated charge or to enable the possibility of accumulating charge over various (N) measurement cycles without performing reset. Since all the high-frequency noise is uncorrelated, the signal-to-noise ratio (SNR) would increase in this way with $\sqrt{N}$, and extend the sensor range resolution by the same factor.

II. N-WELL PHOTODIODE BASED PIXEL FABRICATED IN STANDARD CMOS TECHNOLOGY

The first pixel architecture, technology cross section and schematic diagram of which can be observed in Fig. 1(a) [2], was fabricated in logic-standard 0.5µm 1P3M twin-well LOCOS CMOS technology. The *n*-well PD requires an additional pixel storage capacitor C_s=1pF where a voltage proportional to the charge photogenerated during the integration phase can be stored enabling synchronous integration. During the initial reset phase, the *n*-well PD and Cs are charged to the reference voltage U_{ref_PD} via the reset (RST) PMOS transistor switch and the shutter transistor M1, before each integration period (see Fig. 1(a)). After the RST switch is turned OFF, the discharge of the PD and the Cs begins due to photo- and thermally generated currents flowing in the *n*-well PD. Deactivating the shutter switch M1 enables the integration time control. Through the activation of the row-select transmission-gate switch, the voltage stored at the Cs is read out to the CDS and multiplexed analog memory circuit. The first integration time (Tint1) of the pixel (first shutter window) is synchronized with the laser pulse and delivers the first pixel output signal voltage V1. Following, a second photocurrent integration is performed, this time without a laser pulse to be fired, i.e.

the photocharge is generated by background illumination only, using Tint1 again. The CDS stages, one per array column, are also used as a row-wise multiplexed analog memories, adding an extra CFx capacitor per pixel to each CDS circuit [2].

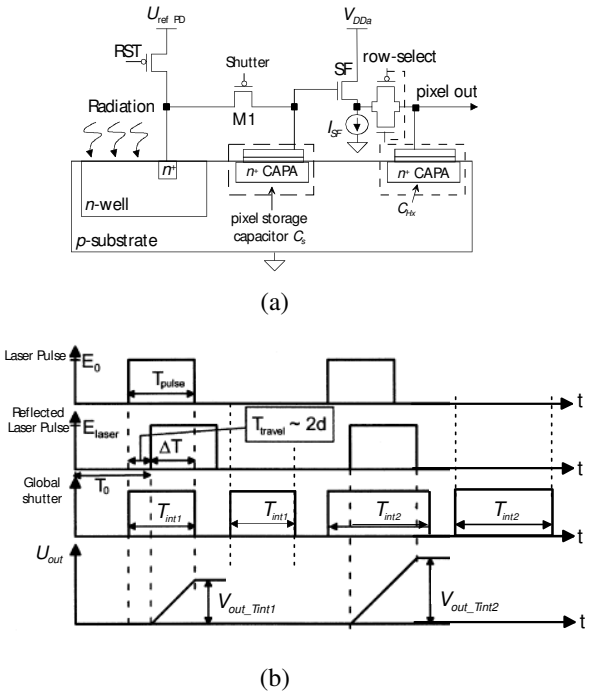


Figure 1. (a) *n*-well PD TOF ranger sensor pixel architectures in cross-section [2]; (b) Time diagram used for ToF measurements based on the pixel architecture depicted in (a) [1].

The second pixel output voltage V2 is then substracted from the already stored V1, and the resulting voltage difference Vout_Tint1 is stored at the chosen CFx. The time diagram corresponding to the range measurement described so far can be observed in Fig. 1(b). This measuring method is called *multiple double short time integration* (MDSI) [3]. The maximum distance measured using MDSI is defined through Eq. (3).

$$d_{\max} = \frac{c}{2} \cdot T_{pulse} \left(1 - \frac{V_{out\_T_{\text{int}1}}}{V_{out\_T_{\text{int}2}}} \right) \qquad (3)$$

The 130µm x 573µm huge pixel yields 52% fill-factor [2]. The in-pixel storage capacitor Cs=1pF limits the FWC to $4x10^6 e^-$, and a measured spectral responsivity is $25V/\mu J/cm^2$ [2] for T_{pulse}=30ns. The problem of this architecture is nevertheless the fact that for the SNR_{max}=72dB related to the FWC mentioned, the ENC is $1030e^-$, which based on Eq. (2), for $S(\lambda)$=0.13A/W and E_R=200W/m^2 yields a distance resolution of 2.44cm for 4.5m distance. As it can be inferred form Eq. (2), this resolution is only possible due to the huge A_{ph} used in the designed pixels. The imminent reduction of the pixel pitch forces a drastic reduction of the ENC.

III. SURFACE-CHANNEL PHOTOGATE (PG) AND PINNED PHOTODIODE (PPD) BASED PIXEL STRUCTURES

Using a standard 0.35µm 2P4M LV/HV CMOS process, we fabricated surface channel PG [4] based pixels. As it can be observed in Fig. 2(a), the PG consists of a polysilicon layer deposited on a thin gate-oxide. For charge transfer to the n^+ floating diffusions (FD) readout nodes, four transfer gates *(TX)* overlapping the four edges of the square PG are used. Each FD is connected to a reset transistor and a source-follower buffer (see Fig. 3(a)).

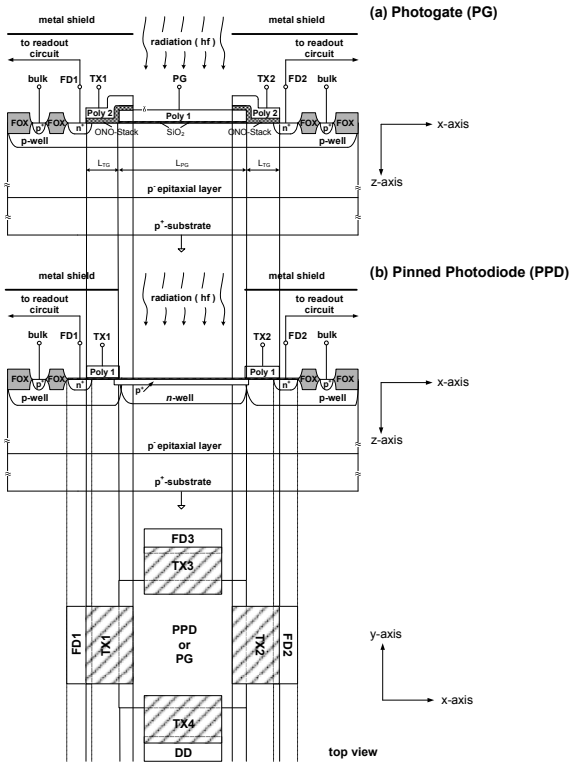
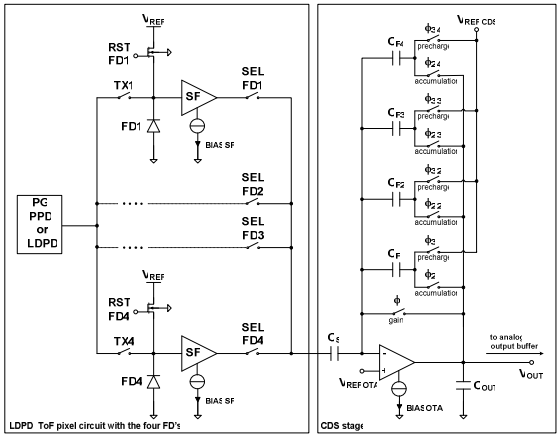
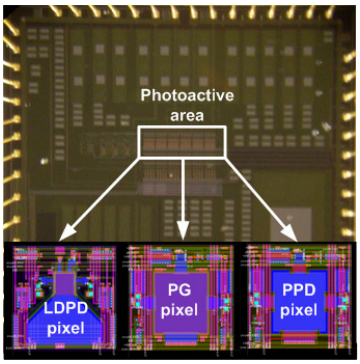


Figure 2. TOF ranger sensor pixel architectures in technology cross-section: (a) PG pixel; (b) PPD pixel.

Based on the same idea pursued by the PG based pixel, a PPD based pixel structure was fabricated as shown in Fig. 2(b). Using the same 2P4M 0.35µm CMOS process, two additional implantation steps were incorporated into the original process flow to obtain an acceptable p^+ highly doped grounded Si-surface pinning layer, and a self-depleted "shallow" *n*-well, yielding an acceptable FWC and a 100% CTE in as a short T_{trans} as possible. The advantages of the PPD pixel over the PG based one are lower dark currents due to the increased doping concentration and the pinning of the Si-surface, and higher S(λ) in the NIR part of the spectra due to a PPD *p-n* junction located deeper in Silicon if compared to the surface channel of the PG (see Fig. 2). Both pixel structures and one additional one, based on an intrinsic lateral drift-field photodiode (LDPD) described in the next section, were fabricated as 4x4 pixel mini-arrays. The chips microphotograph and the schematic representation of the accompanying readout circuit can be observed in Fig. 3.



(a)



(b)

Figure 3. (a) Readout circuit developed for the PG, PPD and LDPD based ToF pixels; (b) fabricated test-field micro photography with the layouts made for each of the pixels.

The two pixel structures shown in Fig 2 enable a different ToF ranging approach. FD1 and FD2 are used here to collect the charge carriers generated by the reflected laser pulse. The first shutter activation (T_{TX1}=T_{pulse}) begins synchronously with the emission of the laser pulse, followed by the second shutter activation (T_{TX2}=T_{pulse}) starting directly at the end of the TX1 pulse, as shown in the time-diagram in Fig. 4. If the time delay T_D between the laser emission and the impinging light of the reflected laser pulse on the photodetector is equal to zero, the whole laser pulse is included in the first shutter window (TX1). Otherwise, the laser contribution is divided into two parts and the amount of charge transferred to FD1 and FD2, respectively, includes the information of the T_D. After TX2 shutter window ends, a short cycle of charge draining (using the drain diffusion (DD) shown in Fig. 2 connected to the reset voltage) follows, shutting TX4 ON, to clear the A_{ph} of undesired charge. Afterwards, an additional measurement using FD3 is performed with T_{TX3}=T_{pulse}, only without the reflected laser pulse radiation impinging on the photoactive area of the pixel, to determine the amount of charge generated by background illumination. During all other operation times, the pixel remains in drain modus (TX4 is ON). This cycle is then repeated enabling charge accumulation at the FDs to further diminish the ENC until short before the FD potential wells get full and the pixel saturates (see Fig. 6). After several charge collection cycles N, the accumulated photogenerated charges (NQ_{FD1} to NQ_{FD3}) at the floating diffusion FD1 to FD3 are used to calculate the distance information d, based on Eq. (4), where T_D is the time delay of the reflected laser pulse compared to the actual laser pulse length (T_{pulse}) as shown in Eq. (5).

$$d = \frac{c}{2} T_D = \frac{c}{2} \frac{Q_{FD2} - Q_{FD3}}{Q_{FD1} + Q_{FD2} - 2Q_{FD3}} T_{pulse} \qquad (4)$$

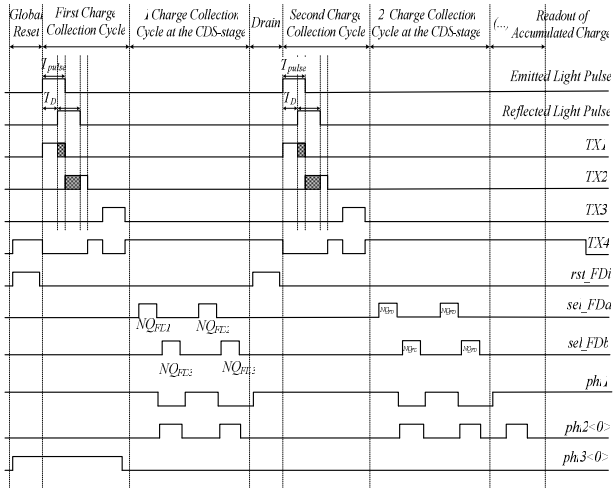


Figure 4. Time diagram used for ToF measurements.

The low spectral responsivity of $\Re$=6.8V/µJ/cm^2 for T_{pulse}=30ns measured at the PG pixels is directly related to T_{trans} of 360ns (see Fig. 6), i.e. CTE<100%. On the other hand, the PPD pixel yields a $\Re$=7.9V/µJ/cm^2 for the same operating conditions with T_{trans}=95ns (Fig. 6). The long charge transfer times from the A_{ph} to the FDs are due to a constant electrostatic potential in the photoactive area, where the charge transfer results enabled only through thermal diffusion mechanisms and insufficiently extended fringe fields at the TX edge.

IV. Intrinsic Lateral Drift-Field Photodiode (LDPD) Pixel for ToF Ranging

Emulating the advantages of the PPD approach and pursuing a shorter T_{trans}, a doping concentration gradient was fabricated within the surface pinned LDPD n-well [5] in such a way that it induces an intrinsic lateral drift field parallel to the Si-surface in the direction of the pixel readout node (x-axis in Fig. 5) as well as from the periphery of the n-well in the direction of the n-well centre (y-axis), as shown in Fig. 5. The potential distribution within the n-well resembles a hopper leading the photogenerated charge directly to the assigned readout nodes (FDs). A MOS capacitor-based *collection-gate* (CG) is fabricated at the one end of the n-well, which remains biased at a certain voltage V_{CG}. It induces an additional electrostatic potential maximum in the system, thus accelerating the photogenerated carriers even more on their way into any of the FDs and enables the proper

and symmetrical distribution of the signal charge among them [5]. The principle of the ToF measurement remains identical and is based on the time diagram from Fig. 4.

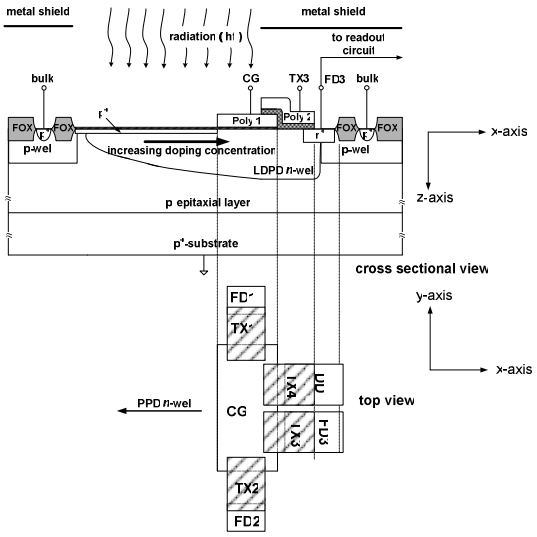


Figure 5. Technology cross-section of the LDPD pixel.

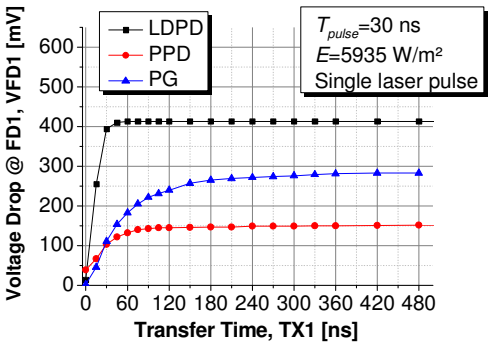


Figure 6. Indirectly measured transfer time for all 3 pixel structures.

The measured responsivity of the LDPD pixel is of 76.7V/µJ/cm² delivering 100% CTE, as shown in Fig. 6. The measurements with in-pixel accumulation have shown that each FD can accumulate photocharge resulting from over 2000 laser pulses with excellent linearity (see Fig. 7). For a single pulse, the pixel delivers ENC=17.4e⁻ for DR=66.3dB, which results in Δd=3.6cm by 4.5m distance measurements and 33% fill-factor. After 2000 readout cycles, millimeter scale resolution is achievable.

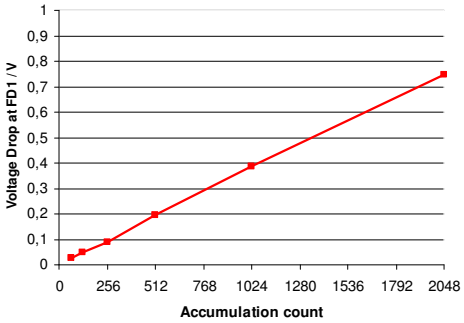


Figure 7. Output voltage at FD1 versus accumulation count.

V. SUMARY OF THE EXPERIMENTAL RESULTS

In Table I, a summary of the characteristics measured on all four pixel structures is presented for comparison.

Parameters	*n*-well PD	PG	PPD	LDPD
CMOS Technology	0.5µm	0.35µm	0.35µm + PPD	0.35µm + LDPD
Pixel size, µm	130x573	40x40	40x40	40x40
Fill-factor, %	52	56.25	56.25	33
T_{trans}, ns	/	360	95	~30
ℜ, V·cm²/µJ	25	6.8	7.9	76.7
FWC, e⁻	4x10⁶	52434	52434	36000
DR, dB	77	64.4	68	66.3
ENC for one laser pulse	1030	31.7	25.38	17.43
Δd, cm for one laser pulse	2.44	/	/	3.6 <1 for 100 accumulations

TABLE I. Summary of the measured charateristics of all pixel structures presented.

VI. CONCLUSIONS

Four different pixel architectures were designed, fabricated and characterized using two different ToF ranging measurement principles. It was shown that for reduced pixel sizes, charge coupling based photodetector structures are required, only fabricated in optimized CMOS technologies. CTE and T_{trans} problems are detected in PG and PPD based pixels with 40µm pixel pitches. A special LDPD pixel yielding an intrinsic lateral drift-field in the photo-active area and enables over more than 2000 charge accumulations was fabricated to overcome this problem delivering a millimetre distance resolution.

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