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A highly manufacturable backside illumination technology for CMOS image sensor

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Abstract

In this paper we report cost-effective and highly manufacturable technology for Backside Illumination (BSI) CMOS Image Sensor (CIS) with high performance even at the small pixel pitch. Our BSI process consists of void-free wafer bonding, uniform silicon thinning and backside silicon treatment including low temperature anneal, metal interconnect and color filter formation. Using above methods, we can achieve high yield with improved sensitivity, suppressed dark current and dark defects.

Introduction

Smart phones spread intensify pixel resolution competition among image sensor makers. As the sensor pixel size is shrunken, metal interconnection layers are increased, so optical performance such as sensitivity, crosstalk, and incident angle dependency worse in conventional CIS. BSI structure is proposed to overcome the optical challenges for getting high quantum efficiency, low crosstalk and insensitive chief ray angle without any side effect. Despite these merits, mass fabrication of BSI sensor needs more complicated process than FSI sensor. Emerging technologies for mass production such as, wafer bonding, damage reduced grinding, one stop wet etch, low temperature anneal, silicon surface treatment and enhanced measurement method are needed. We successfully fabricate in large quantities of high performance 1.4um and 1.1um BSI chips at low cost by using these innovative methods.

Technology and Pixel performance

Guaranteed wafer bonding process is key technology to achieve higher production yield and process stability. Defects in boned wafer are long-pending trouble for mass production.

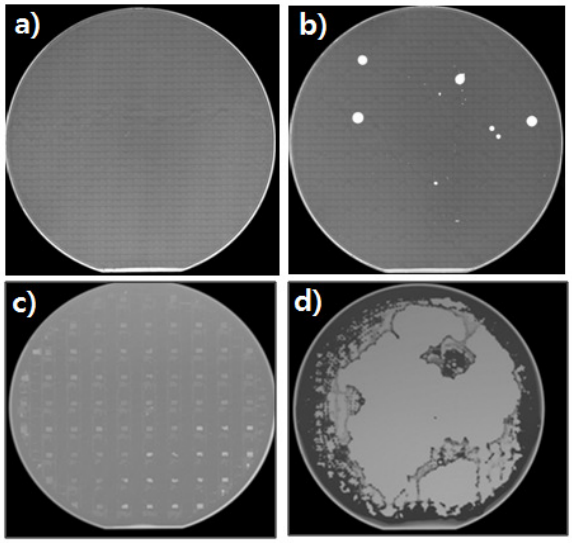

Fig. 1. SAM (Scanning Acoustic Microscopy) image of wafers a) defect free b) particle induced void c) local deformation defect d) bad surface roughness de-bonding

We removed various causes of void such as particles, silicon local deformation and surface roughness. Thin film stress level adjustment

method and adequate heat treatment after wafer bonding was adapted to increase bonding quality. Figure 1 shows some kinds of bonding defect. Well-tuned bonding recipe enables to get defect free bonded wafer with high bonding strength and raised productivity.

Widely used epi wafer, instead of SOI (Silicon On Insulator), was chosen for lower cost BSI products. In case of using bulk silicon, wafer thinning is the most important process to realize uniform pixel characteristics in BSI structure. Our thinning process adapts multi- step mechanical grinding and following one-stop wet etching with high selectivity as shown Fig. 2.

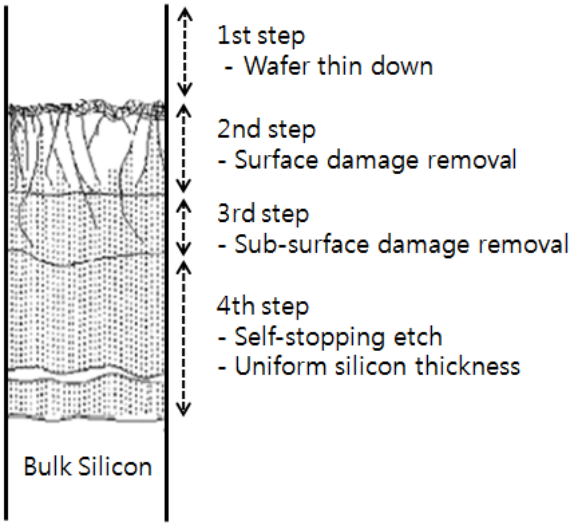

Fig. 2. Schematic of defect free and guaranteed wafer thickness thin down process

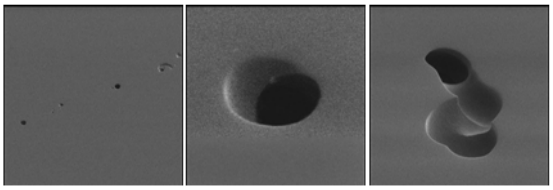

Fig. 3. Silicon wafer pit defects related with mechanical grinding damage and following wet etching

Multi-step wafer thinning method can reduce grinding damage which causes wafer pit defects during one-stop wet etching process as shows in Fig. 3.

Figure 4 shows controllability of remain silicon thickness variation within 3% by using one-stop wet etching with elaboratively mixed chemical and well –tuned recipe.

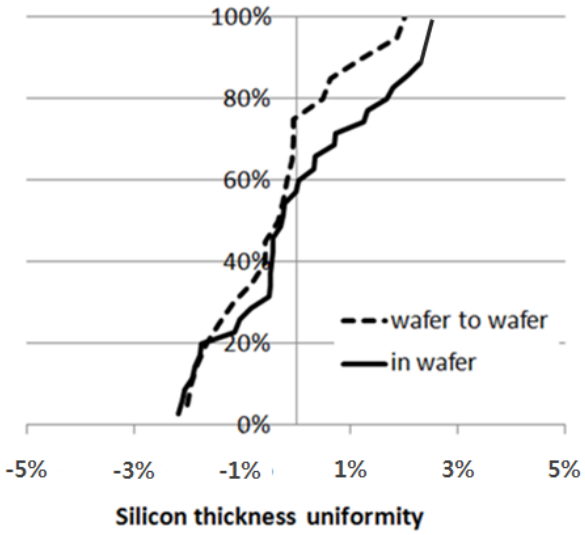

Fig. 4. Silicon wafer thickness uniformity by multi step wafer thin down method

It is most critical to electrically passivate backside surface to suppress dark current and white spot. It is not easy to get clean silicon surface due to limitation of low process temperature. We have successfully integrated a backside passivation process using p-type doping, post low temperature annealing and post annealing treatment.

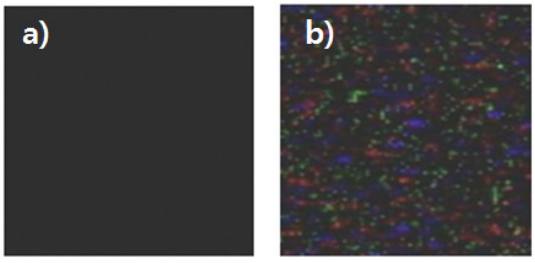

Fig. 5. Raw dark image a) after backside surface treatment b) without any surface treatment

By using these methods we can get very low

dark current and extremely small number of white spot as shown Fig. 5. Dark image quality of BSI sensor is almost same as FSI sensor's one.

To obtain high quantum efficiency, low crosstalk and insensitive chief ray angle we adapt shortest optical path between color filter array and photodiodes with optimized curved high fill factor micro lens as shown in Fig. 6.

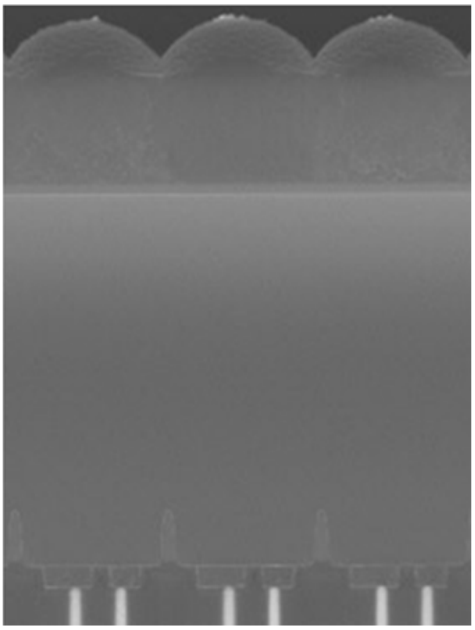

Fig. 6. Cross-sectional image of 1.4um pixel BSI sensor

Low distance variation between silicon and color filter array is important for uniform optical performance. These cost effective fabrication methods are specially designed for not only high pixel performance but high fabrication yield.

Well defined deep photo diode in thick silicon has been adapted with anti-reflection layer optimization specific to BSI structure. As silicon is thicker, quantum efficiency goes higher, if electrical crosstalk is well suppressed. Fabrication of isolated photo diode between adjacent pixels is key technology to use thick silicon. We developed simple and cost-effective photo diode formation method to maximize pixel performance by using thick silicon as shown in Fig. 7.

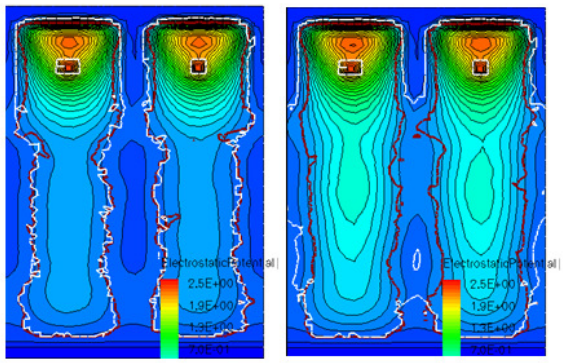

Fig. 7. Simulation result of deep photo diode

As shown in Fig. 8, 18%, 39%, 48% improvement of sensitivity has been achieved in the blue, green and red channels respectively compared with typical 1.4㎛ pixel with low dark current and few white spots.

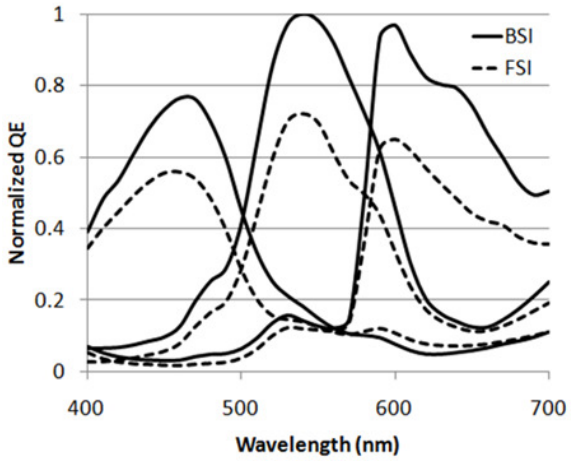

Fig. 8. Optical performance of 1.4 BSI sensor

Image evaluation result in figure 9 shows improved image which has higher SNR and lower white spot under low light.

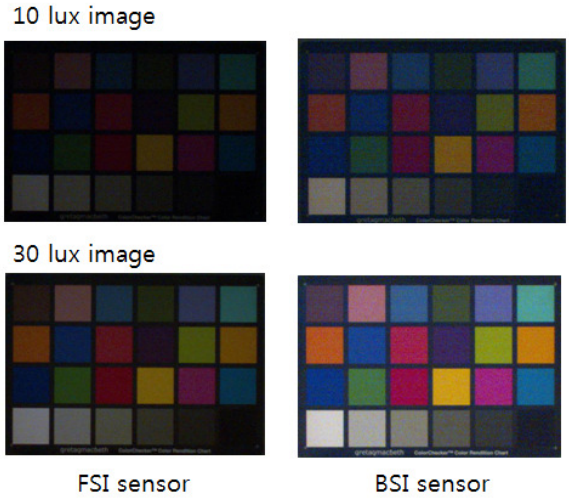

Fig. 9. Image of FSI and BSI sensor under low light

Conclusion

A cost-effective and manufacturable BSI process has been introduced in this paper. Bulk silicon is used instead of SOI wafer with damage reduced grinding and one-stop wet thinning technology for tightly controlled remain silicon thickness. Well aligned and void free wafer bonding process was developed for high production yield. Low dark level and white spot can be achieved by enhanced silicon surface treatment which include ion implantation, laser anneal and post surface treatment. Optimized optical path and photo diode was designed for higher optical performance with simple method. We can get more over 40% R/G/B QE and low dark current. This technology platform also can be applied for 1.1um pixel and beyond.

Reference

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