

High Performance and High Yield Junction Formation with Full Device Exposure Laser Thermal Annealing

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Abstract- Pulsed Laser Thermal Annealing (LTA) of Silicon in the nanosecond regime has attracted a considerable attention regarding the activation process for nanodevices. Pulsed LTA with an Excimer laser is of a particular interest for the activation of dopants in shallow implanted layers such as the backside junction formation for 3D-integrated devices including sensing devices. Indeed, high activation of the surface layer can be achieved, without harming the underlying buried device layers. In this work, Backside Illuminated CMOS Image Sensors passivation with the LTA process was studied for various implantation and process conditions. It is shown that both melt and non-melt regime can be well suited for an optimal pixel performance. Moreover, it was hinted that a uniform and stitchless annealing process is necessary to achieve high sensor performance. Here, the ability of the Full Device Exposure (FDE) feature of the LTA tool to adapt the processed area to various sensor geometries is demonstrated.

I. INTRODUCTION

With the continuous downscaling of device geometries for many semiconductor applications such as thin wafer power devices, backside illumination sensors or other 3D-integrated devices, ultra low thermal budget processing is now a critical issue. The thin junctions obtained by ion implantation require high activation and low surface roughness. The necessary thermal annealing step should induce high temperatures near the surface while keeping the underlying metal and device layers at low temperature. Laser Thermal Annealing (LTA) is the most adapted processing solution to achieve these specific requirements. Indeed, highly activated junctions with excellent surface roughness have already been obtained with the LTA process [1-8]. Another major challenge, more specific to imaging sensors, is to achieve excellent backside activation uniformity within the sensitive area. Macroscopic (within wafer) and microscopic (within shot) sheet resistance uniformity have recently been obtained on samples processed with LTA thanks to its unique Full Device Exposure (FDE) capability [4,5], thus

demonstrating the high yield achievable with this process. In the case of BackSide Illuminated CMOS Image Sensors (BSI-CIS), high quantum efficiency was obtained over all the visible spectra, especially for the blue wavelengths, thus enabling high quality image sensors with excellent sensitivities [4,7].

This unique high performance and very uniform process can be applied to any high added value annealing process, such as those requested for present and future CMOS Logic manufacturing

Many factors may influence BSI-CIS performance, especially those concerning the ultra-thin sensitive Si layer properties. The design of the thin backside junction is one of the critical parameters to optimize the sensor quality. In this perspective, the LTA process was studied for various implantation and process conditions on thick SOI and on actual device. The influence of dopant dose and LTA process regime (non-melt or melt) on pixel performance (dark current and sensitivity) was analyzed. Moreover, a stitch-less and uniform annealing process over the full sensor area was shown to be mandatory [5,6]. Such a requirement is achievable thanks to the FDE feature of the LTA process. The capability of the LTA to provide field sizes adapted to device geometries is demonstrated.

II. EXPERIMENTS

In this work, thick p-type SOI samples (similar to actual BSI-CIS sensor layer stacks) were implanted with Boron. The buried oxide (BOX) of the SOI substrate is used here as an etch-stop layer and is removed prior to implantation. Laser Thermal Annealing was realized with Excico LTA equipment, based on UV ($\lambda = 308$ nm, pulse duration < 200 ns) laser head, with a maximum beam size of 20×20 mm². Various laser Energy Densities (ED) were considered to investigate both melt and non-melt LTA conditions. ED values are referenced in % relatively to the melting threshold energy density.

Multiple pulses were also applied in the non-melt regime. Finally, actual devices were annealed for specific implantation and LTA conditions. Sensitivity in the blue region as well as dark currents have been measured. Melt duration was monitored with in-situ Time Resolved Reflectivity (TRR) at 632.8 nm [1]. Dopant chemical profiles were obtained by Secondary Ion Mass Spectroscopy (SIMS). Sheet resistance (R_s) was measured with four-point probe. Within shot surface roughness was measured by Atomic Force Microscopy (AFM). Alternate laser beam sizes and shapes obtained with the FDE feature were characterized on amorphous silicon wafers (a-Si / SiO₂ / Si).

III. RESULTS AND DISCUSSION

A. Junction properties

The Boron profiles obtained by SIMS after LTA for different laser ED (94% to 150%) and the as-implanted profile for the $3 \times 10^{13} \text{ cm}^{-2}$ boron dose are plotted on Fig. 1. In all cases, the melting of the processed area was monitored by the TRR signal. Since the B diffusion is much higher in the liquid than in the solid phase ($\approx 10^6$ times), there is no visible diffusion in the non-melted region [1-8]. Two main trends can be observed depending on the melted depth. When the melted depth is shallow, close to the tail of the as-implanted profile, some slightly retrograde gradient can be seen. For deeper melt, this effect tends to disappear and the final profile is more box-like. This dopant pile-up effect is still under investigation, but could be explained by recrystallization transients, as studied in [9]. This effect can be solved by using shallower implantation methods (e.g. screening oxide or pre-amorphization) or multiple pulses [5]. In the non-melt cases (94%), no change in the dopant profile was observed, even with multiple pulse conditions (not shown). This demonstrates the diffusion-less character of the LTA process in the non-melt regime.

Fig. 2 shows R_s measurements for the $3 \times 10^{14} \text{ cm}^{-2}$ dose case for single and multiple pulses. In the single pulse case, the general trend is typical of the LTA activation mechanism. In the non-melt regime, there is a limited but significant R_s lowering, mainly dependant on the activation rate (up to 34% at ED = 94%). In the melt regime, a sharp drop is observed and R_s is nearly constant, as a consequence of the activation rate close to 100%.

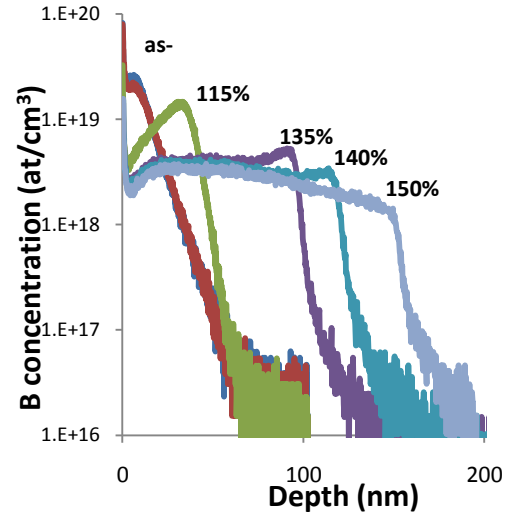


Fig. 1 B profiles (SIMS) for B, $3 \times 10^{13} \text{ at/cm}^2$ dose: as implanted and ED = 94% to 150% of the melting threshold ED.

Interestingly, in the non-melt regime, it can be seen that higher activation rates were obtained in the multiple pulse cases (up to 52% for 9 pulses). As discussed in [8], this cumulative effect can be explained by the additional thermal budget applied with each pulse, which gives enough energy for the interstitials to diffuse into substitutional sites in the lattice. Although the activation rates are still lower than in the melt regime, the major advantage of the non-melt regime with multiple pulse is that the final junction profile is only limited by the implantation.

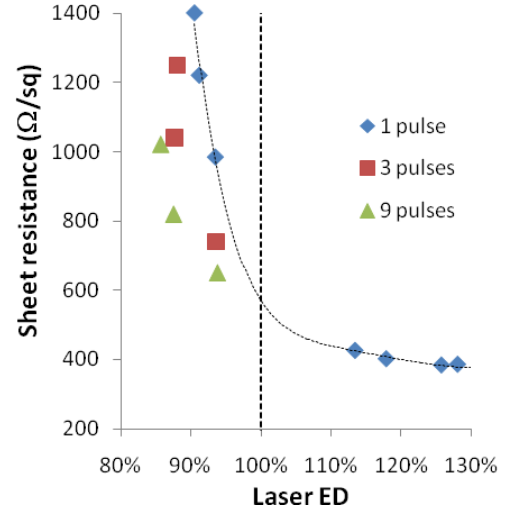


Fig. 2 R_s vs. ED for B, $3 \times 10^{14} \text{ at/cm}^2$ dose. Diamonds: 1 pulse, squares: 3 pulses, triangles: 9 pulses.

These results confirm that junctions suitable for the backside passivation of BSI sensors can be successfully achieved with shallow implantation followed by LTA.

B. Device performance

In order to confirm this on actual devices, such backside passivation was done on actual BSI-CIS wafers using thick SOI substrates.

Fig. 3 shows the typical roughness vs. laser ED with the associated AFM pictures. The surface roughness trend shows excellent values (equal to initial value) both in non-melt and melt regime, with a high value peak near the melting threshold. This can be explained by the micro non-uniformity of the beam, which has an influence only near the melt threshold, since the irradiated area is only partially melted.

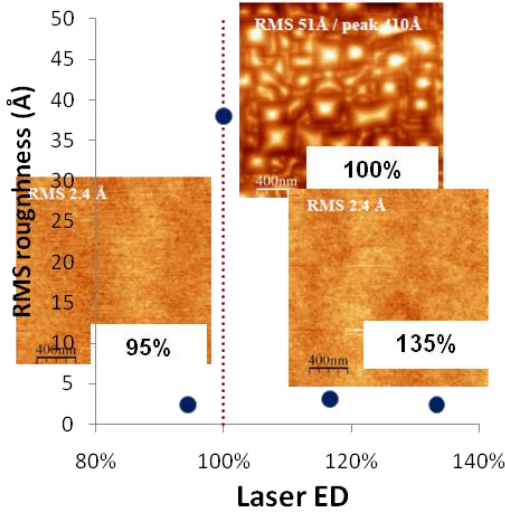


Fig. 3 Surface roughness vs. ED on device wafers.

Fig. 4 shows final device performance in terms of sensitivity in the blue wavelength region and dark current (I_{dark}) as a function of laser ED and for 2 implantation doses. The best performance is achieved for the lowest dose case (Dose1) in the melt regime.

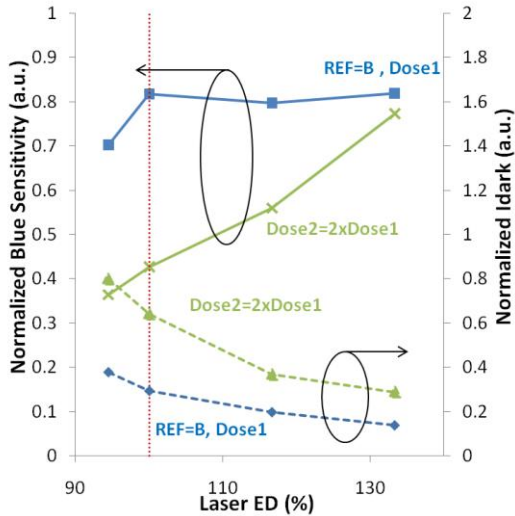


Fig. 4 Device performance vs. ED: blue sensitivity (solid lines) and I_{dark} (dashed lines) for 2 implant doses.

However, even in the non-melt regime, acceptable sensitivity and I_{dark} could be achieved for this dose. In the case the dose is doubled (Dose2), acceptable performance could only be reached in the melt regime. This poor performance may be caused by the higher amount of unactivated dopants remaining in the dopant profile tail. In this case, performance increases as the ED, which is consistent with a better damage recovery in the deeper regions (deeper melt). Similar trends were observed for pre-amorphized junctions and higher implantation doses (not shown).

I_{dark} performance for non-melt LTA is shown on Fig. 5 as a function of the number of pulses, with the associated R_s value obtained on the blanket SOI wafers. As it can be seen, I_{dark} and R_s trends are similar. However, I_{dark} values close to the melt regime reference can be reached with 9 pulses, whereas the corresponding R_s value is still high. This is a signature of an excellent post-LTA crystal quality, even though some non activated dopants remain. Therefore, as discussed in [8], multiple pulse LTA in the non melt regime is one of the solutions to achieve good device performance. It should be noted that this behavior is favored by the use of longer pulse duration than other Excimer laser sources, which are typically closer to 30 ns.

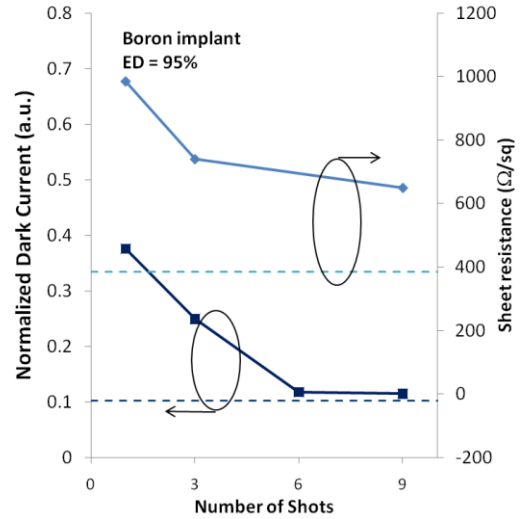


Fig. 5 Dark current (device) and R_s (blanket) vs. number of shots in the non-melt regime (ED = 95%). Dashed lines: respective melt regime references.

These results show that the junction properties and associated device performance are highly dependent on the laser energy density considered. Therefore, a highly homogenous process is required with the sensor area to avoid final junction non-uniformities.

C. FDE capability

As it was shown previously with micro-scale sheet resistance measurements [5], the overlap effect on shallow junction properties is two-fold. First, it induces a slightly deeper junction, which may impact the electric field profile and induce higher recombination. Second, in some cases, mostly in the melt regime, it can induce a peaked non uniformity due to the presence of the shot border [5].

In order to fulfill the requirements for a uniform process, the shot area has to be changed according to the device (or sensor) geometry. Indeed, as it was shown previously using micro-scale sheet resistance measurements [5], the presence of the shot border or overlap within the area of interest may induce significant non-uniformities in junction properties. Since the junction properties (thickness, activation rate) may influence carrier recombination, sensitivity in the blue wavelength region as well as the collection of the photo-generated carriers, they should be carefully controlled.

As a consequence, the sensors should be annealed within a Single Shot Area (SSA). This SSA is defined as the area which is guaranteed to be irradiated within the top hat of the laser beam and only once, taking also into account within wafer and wafer to wafer positioning accuracy. Examples of a-Si wafers annealed for 2 different shot sizes are shown on Fig. 1 and Fig. 2, at laser ED corresponding to the top hat area of the beam. As it can be seen, both square and rectangular areas can be obtained. Shot-to-shot distances close to scribe line widths were achieved. Thus, large sensors with high fill factors can be processed. It is to be noted that with such large sizes, depending on device design, one or several dies could be annealed within each SSA, thus optimizing the throughput of the system.

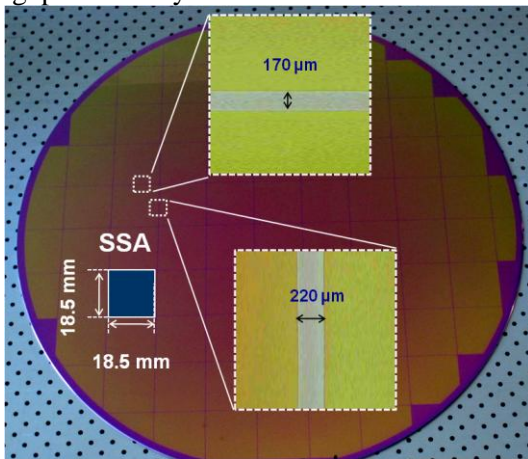


Fig. 1 Shot map on a-Si wafer for configuration 1 (Square Single Shot Area of 18.5x18.5 mm²).

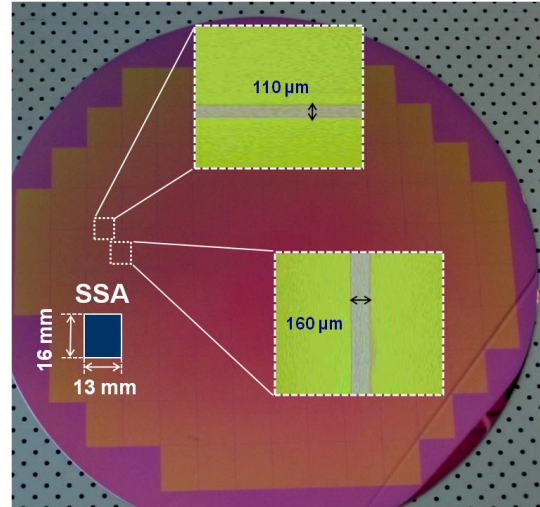


Fig. 2 Shot map on a-Si wafer for configuration 2 (Rectangular Single Shot Area of 13x16 mm²).

IV. CONCLUSION

In this work, the LTA process for shallow junction formation for the backside passivation of BSI sensors was investigated on blanket SOI and device wafers. Both non-melt and melt regime fulfill the requirements for a good backside passivation, thus ensuring excellent device performance.

The best performance was obtained in the melt regime, thanks to activation rates close to 100% and complete recovery of the implantation induced crystal damage.

In the non melt regime, although reasonable performance was achieved with a single pulse process, a multiple pulse approach shows better activation (up to 50%) and excellent crystal recovery thanks to the thermal budget accumulated with each additional pulse.

Moreover, with the Full Device Exposure feature, the ability of the LTA tool to provide several shot sizes and shapes adapted to device geometry has been demonstrated on a-Si wafers. Depending on die sizes and fill factors, one or several sensors could be annealed within a single shot area.

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