The Mass Production of Second Generation 65 nm BSI CMOS Image Sensors

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Abstract

Backside Illumination (BSI) CMOS image sensors have now been in high volume mass production for over two years, supplying OmniBSI™ products to the high performance mobile handset market.[1] A major development in imager technology was the mass production of first generation BSI technology using 0.11 µm Al processing for image sensors at low cost and high yield.[2,3] The second generation BSI products will use 65 nm Cu processing on 300 mm wafers. The OmniVision-TSMC R&D Alliance reports that the pixel and process development has enabled this second generation BSI technology node. To reduce cost and accelerate the transition from FSI to BSI, OmniBSI technology used 0.11µm CIS design rules, identical to OmniPixel3-HS™ FSI technology. Shrinking the CIS design rules to 65 nm and developing new CIS process modules has enabled a 1.1µm pixel and further improved the performance of 1.4µm and 1.75µm pixel products. The low cost bulk silicon technology that was developed for OmniBSI is maintained on the OmniBSI-2™ 300 mm Cu production line. We will report the performance on all three OmniBSI-2 pixels. In addition to reporting on our development work, we will include the performance of the first four OmniBSI-2 products in mass production ramp. For the 1.1µm pixel, peak quantum efficiencies of 56%, 72%, 72% has been achieved in the red, green and blue channels respectively, with low crosstalk, excellent Gb/Gr performance, no lag, no FPN, dark current of 7 e/sec at 60°C, and low white pixel defect density. For 1.4µm and 1.75µm pixel products, the baseline OmniBSI-2 process has been re-optimized to achieve peak QE of 59%, 72%, and 72% in the red, green, and blue channels, respectively. Our reliability testing has found no reliability issue associated with OmniBSI-2 architecture.

Introduction

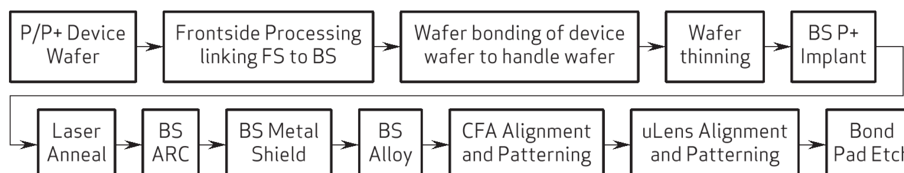
Early predictors of the CIS technology roadmap wrote that the advantage of CIS was that this new imaging technology would follow in the shadow of mainstream logic development.[4] Many CIS technologists developing the new processes knew that CIS would depend heavily on marrying CCD and logic or DRAM processing know-how and, to be successful, would forge its own set of design rules and process modules appropriate for an optoelectronic device.[5] A clear break between past CCD and logic/DRAM production processes occurred with the move of advanced CMOS imagers into BSI, not as a scientific imager for space telescopes or low volume DSC products, but into high volume mass production for high performance smart phones.[1,2] The first generation BSI products required the development of multiple new process modules for both the frontside (FS) and backside (BS) process modules. For the second BSI generation, OmniBSI-2, seven new design improvements and ten new process modules were developed and implemented into our first OmniBSI-2 products. OmniBSI provides several realized advantages over frontside illumination (FSI) sensors: quantum efficiency, crosstalk, color shading, sensitivity, stack height, 100% fill factor, better acceptance of higher speed lenses, and improved performance across the entire image plane. Another BSI key advantage is the elimination of the bulk substrate, which substantially reduces both the diffusion component of dark current and electrical crosstalk. OmniBSI-2 provides eight performance improvements over the first generation OmniBSI products:

1. 20% higher QE
2. 30% higher Sensitivity
3. 33% better SNR10
4. 20% higher FWC
5. 2 dB higher Dynamic Range
6. 3X lower (improved) Dark Current
7. 20% lower (improved) PRNU
8. 2 dB higher SNR_max

OmniBSI-2 Products, Design Rules, and Pixel Design

The data to be presented comes from the characterization of our 65nm development chip and four OmniBSI-2 products. The 1.1µm pixel data comes from our development chip data. The 1.4µm and 1.75µm pixel data comes from four OmniBSI-2 products. The second generation OmniVision-TSMC jointly developed OmniBSI-2 technology uses a combination of 65 nm and 90 nm design rules using standard Cu BEOL processing on 300 mm bulk silicon wafers. The design rules are specifically tailored and pushed where needed to improve the pixel design and the image performance.

BSI Process



The process begins with a low cost p/p+ bulk silicon device wafers. A new BSI frontside (FS) process was developed to link a low noise, fully depleted, no lag FS photodiode with the BS surface. A total of 18 new process modules were evaluated during the development stage and ten were adopted for mass production. After FS processing, the metalized side of the device wafer is bonded to handle a wafer with no voids and no added defects. The exposed BS surface of the device wafer is then thinned to the final target epi thickness. QE and crosstalk are critically dependent on both the FS processing and the BS thinning. A proprietary thinning process module is used to provide a reproducible final epi thickness on standard p/p+ device wafers. Figure 1 shows the final epi thickness uniformity of of the 1.1µm pixel on 300mm wafers. Good thickness uniformity is achieved. BSI manufacturing based on SOI starting wafers is expensive and destroys profit margins. The worldwide supply of SOI wafers is limited, destroying the ability to supply to products in very high volume as demanded by the smart phone market. Figure 1 clearly shows that SOI wafers are not required to achieve acceptable final epi thickness reproducibility and uniformity. OmniBSI is the only BSI technology that has delivered a p-epi on p+ in very high volume over the last two years.[1] To achieve good blue response, low dark current, and low white pixel defect density, the BS surface is passivated with a BS P+ implant and laser anneal. A BS anti-reflection coating (ARC) is deposited to further improve QE at all wavelengths. A color filter array followed by a microlens is aligned and patterned on the backside surface of the thinned device wafer. The final step is the opening of the bond pads. See Figure 2 for a cross-section of the 1.1µm pixel. That low cost p/p+ OmniBSI technology has now been successfully transferred to the 300 mm Cu OmniBSI-2 line.

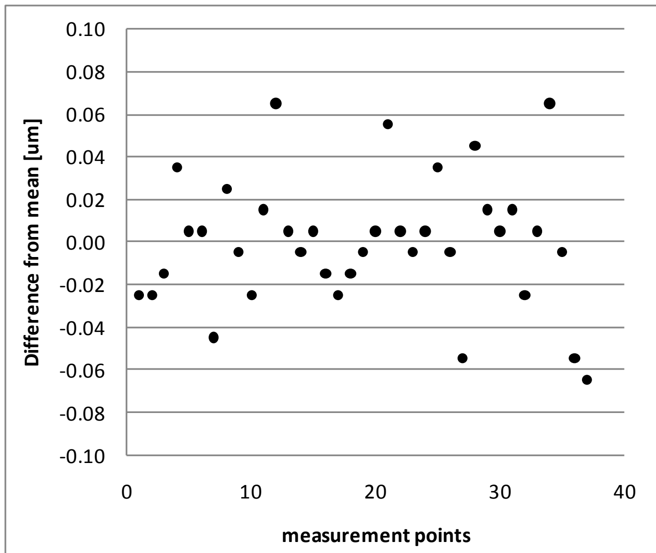


Figure 1. Final epi Thickness Uniformity on 300 mm Wafers (39 points measured across wafer in a 1.1µm pixel array)

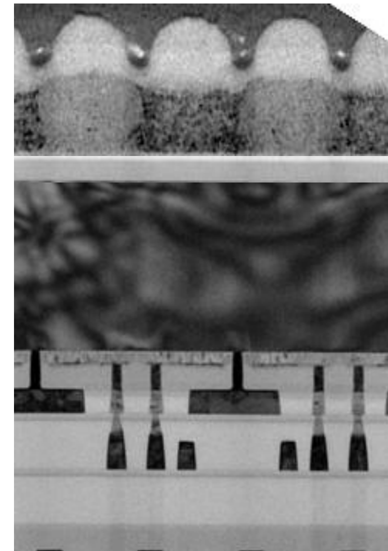


Figure 2. 1.1µm Pixel Cross-section

1.1µm OmniBSI-2 Pixel Performance

Figure 3 displays the quantum efficiency of the R, G, and B channels versus wavelength of the 1.1µm pixel. Peak quantum efficiencies of 56%, 72% and 72% are achieved at the R, G, and B channels, respectively, as well as low optical and electrical crosstalk. We measure a black and white QE of 60%, 74% and 95% at the R, G, and B peaks which agrees with our calculations.[6] As there is no metal in the array, the microlens fill factor is 100% and the microlenses serve to focus the incident radiation to improve crosstalk. The high blue QE is a strong indicator of effective passivation of the BS surface. The linear FWC is 4500e. The Gb and Gr channels are explicitly shown in Figure 3 to demonstrate the nearly identical performance of these channels which is an indicator of low crosstalk and a symmetric pixel design. An advantage of low crosstalk is that raw images produce reasonable color reproduction without a CCM under all source illuminations. The low BSI stack height enables the use of high speed, low F/# lenses. It also provides a wide acceptance angle so that high QE/low crosstalk performance is maintained across the entire image array.

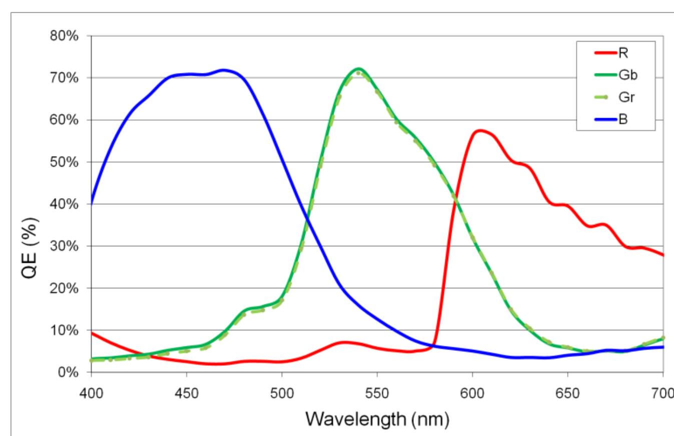


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Figure 3. Quantum Efficiency R, G, and B channels Versus Wavelength

To measure the low light S/N performance of the 1.1µm pixel, raw images through a F/2.8 lens are collected from an 18% gray patch from a 3200K light source. After AWB and CCM, the experimentally measured luma S/N is plotted in Figure 4 versus the incident Lux level on the gray patch. For the 1.1 µm pixel, an S/N of 10 is achieved at 105 Lux which agrees with the theoretically calculated performance based on the QE performance shown in Figure 2.[7] A sensitivity of 650 mV/lux-sec is achieved at 530 nm.

Lag variation can be a noise source, appearing as pixel FPN. In Figure 5, we show lag as a function of transfer gate (TX) pulse width at two different signal levels. Lag is <1e for the standard pulse width of 500 ns and can only be measured when the TX pulse width is reduced to 20 ns. As the floating diffusion fills up with electrons under higher signal measurement conditions, the voltage drop across the transfer gate is reduced and lag can increase to unacceptable levels. The data in Figure 5 clearly shows that lag is not an issue on the 1.1 µm BSI pixel at all signal levels.

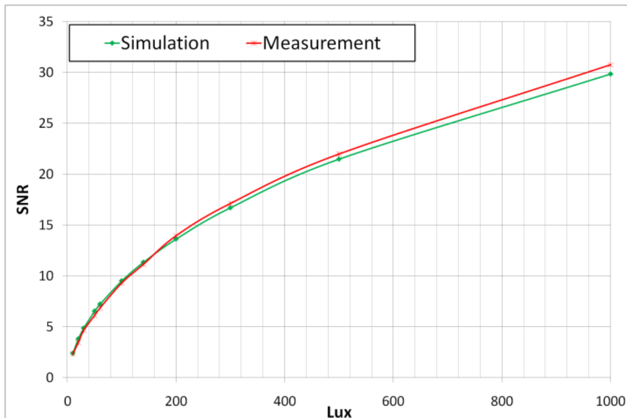


Figure 4. Luma S/N After CCM and AWB Versus Light Level (Lux)

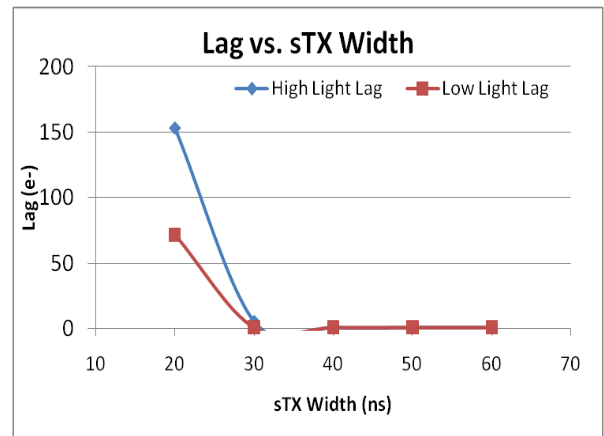


Figure 5. Lag(e) Versus t_tx for 1.1µm Pixel

Dark current and FPN are critical parameters for all image sensors. High dark current can impact low light performance, add FPN, and reduce yield. Some high speed, autofocus, zoom module applications can drive the internal junction temperature to 85°C. At such high junction temperatures, low dark current is a critical performance parameter. Shown in Figure 6 is a raw dark image taken at 85°C, 7.5 fps and 8x analog gain. No column or row FPN is observed.

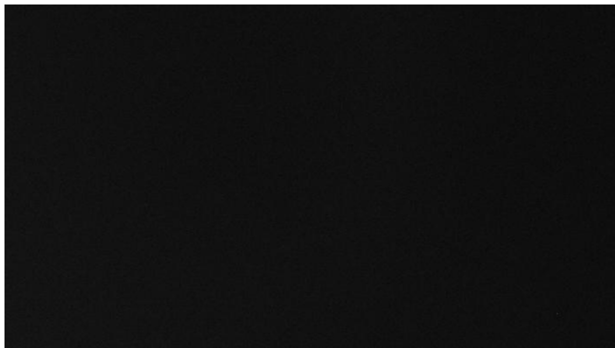


Figure 6. RAW Dark Image

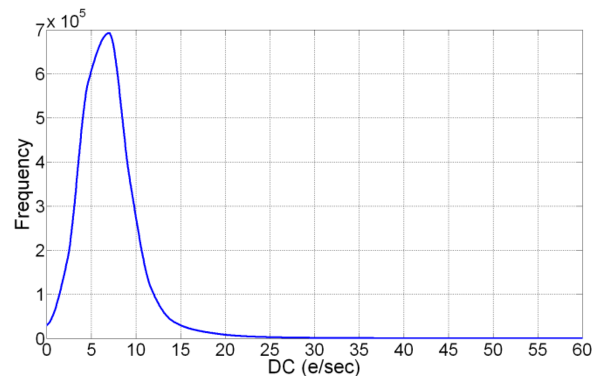


Figure 7. Dark Current Histogram for 1.1µm Pixel at 60°C

A histogram of the individual pixel dark current at 60°C for the entire 2 Megapixel sensor is shown in Figure 7. The dark current peak at 60°C corresponds to 7 e/sec.

In Figure 8, we show the temperature dependence of the measured dark current for the 1.1 µm and 1.4 µm pixels measured after complete BS processing. Fully processed BSI parts achieve 7 e/sec and 10 e/sec dark current at 60°C for the1.1 µm and 1.4 µm pixels, respectively. An activation energy close to the 1.12 eV silicon band gap is measured for both pixels.

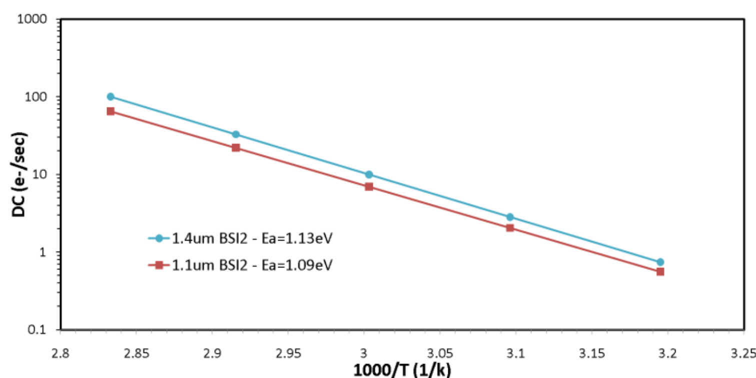


Figure 8. Dark Current Versus Temperature

Table 1 summarizes the 1.1µm, 1.4µm, and the 1.75µm OmniBSI-2 pixel performance. The excellent PRNU is a result of the low optical/electrical crosstalk.

Table 1. 1.1µm, 1.4µm, and 1.75µm OmniBSI-2 Pixel Performance

Parameter	1.1 µm	1.4 µm	1.75 µm
Linear FWC	4500 e	5300 e	9000e
Peak QE - R	56.00%	59.00%	59.00%
Peak QE - Gb	72.00%	72.00%	72.00%
Peak QE - Gr	72.00%	72.00%	72.00%
Peak QE - B	72.00%	72.00%	72.00%
R/B	5.00%	3.00%	3.00%
G/B	13.00%	13.00%	13.00%
R/G	9.00%	7.00%	7.00%

Parameter	1.1 µm	1.4 µm	1.75 µm
B/G	30.00%	30.00%	30.00%
G/R	28.00%	28.00%	28.00%
B/R	9.00%	9.00%	9.00%
Sensitivity (530nm)	650 mV/Lux-sec	860 mV/Lux-sec	1330 mV/lux-sec
PRNU	1.00%	0.80%	0.60%
Lux for 10:1 SNR	105 Lux	68 Lux	41 Lux
Dark Current (60°C)	7 e/sec	10 e/sec	15 e/sec

Comparison of the OmniBSI Versus the OmniBSI-2 Pixel Performance at the Same 1.4µm Pixel

The smallest pixel that we have fabricated in the 0.11µ OmniBSI process is a 1.4µm pixel. To evaluate the effect of the improved design rules, pixel design architecture changes, and new process modules, we compared the performance of OmniBSI versus OmniBSI-2 at the same 1.4µm pixel size. Table 2 summarizes this performance.

Table 2. OmniBSI Versus OmniBSI-2 Performance at the Same 1.4µm Pixel Size

Parameter	1.4 µm OmniBSI	1.4 µm OmniBSI-2
Linear FWC	4500 e	5300 e
Peak QE - R	51.00%	59.00%
Peak QE - Gb	60.00%	72.00%
Peak QE - Gr	60.00%	72.00%
Peak QE - B	62.00%	72.00%
R/B	5.00%	3.00%
G/B	11.00%	13.00%
R/G	11.00%	7.00%

Parameter	1.4 µm OmniBSI	1.4 µm OmniBSI-2
B/G	35.00%	30.00%
G/R	34.00%	28.00%
B/R	7.00%	9.00%
Sensitivity (530nm)	670 mV/Lux-sec	860 mV/Lux-sec
PRNU	1.00%	0.80%
Lux for 10:1 SNR	88 Lux	68 Lux
Dark Current (60°C)	30 e/sec	10 e/sec

In addition to using 65 nm design rules on 300 mm Cu bulk silicon wafers, OmniBSI-2 incorporates five improvements to our pixel design architecture and ten new process modules. The result is the simultaneous improvement of eight performance parameters as shown in Table 2:

1. 20% higher QE
2. 30% higher Sensitivity
3. 33% lower SNR10
4. 20% higher FWC
5. 2 dB higher Dynamic Range
6. 3X lower (improved) Dark Current
7. 20% lower (improved) PRNU
8. 2 dB higher SNR_max

A comparison of the QE versus wavelength for these two technology nodes for the same 1.4µm pixel is shown in Figure 9. Also shown in Figure 9 for comparison is the QE versus wavelength for the 1.1µm pixel. From Figure 9 and the data in Table 2, it can be seen that the OmniBSI-2 1.4µm pixel performs better than the first generation OmniBSI 1.4µm pixel. From Figure 9 and Tables 1 and 2, it can be seen that the OmniBSI-2 1.1µm pixel performs similar to the first generation OmniBSI 1.4µm pixel. Further performance improvements to OmniBSI-2 technology will be available soon.

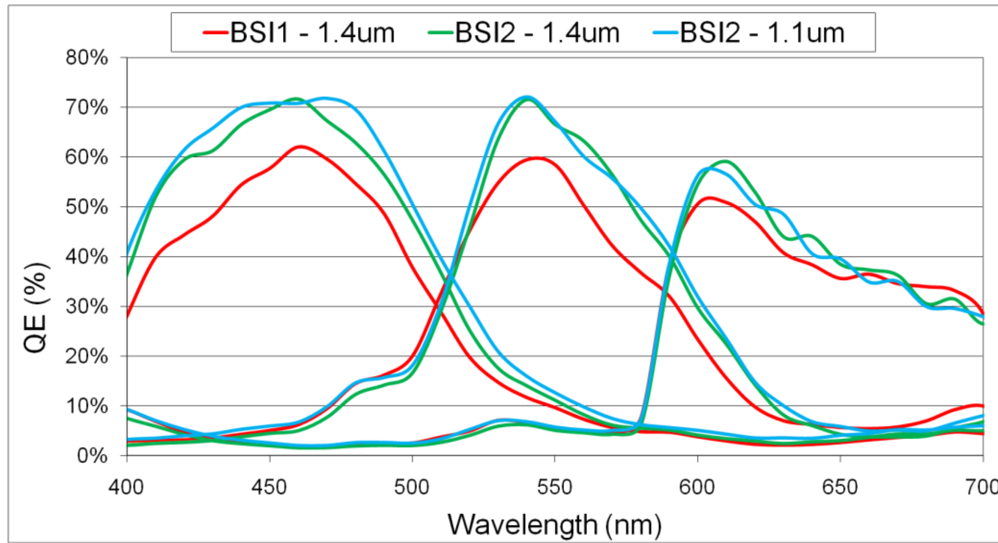
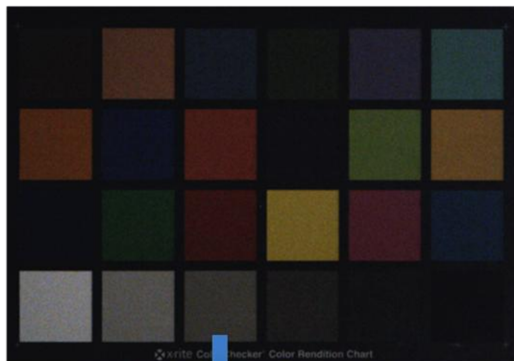


Figure 9. QE Versus Wavelength Performance

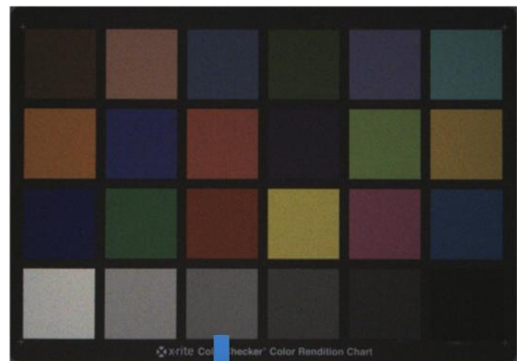
The color image performance of the 2011 1.4µm OV8830 OmniBSI-2 8 Megapixel sensor product is shown in Figure 10 at 10 lux (A light) and 1/15 s exposure compared to the 2009 1.4µm OV8810 OmniBSI 8 Megapixel sensor. A low light 3.4 dB SNR improvement is measured.

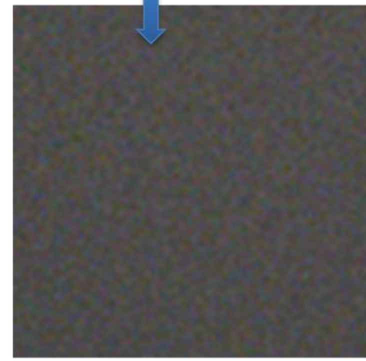
2009 OV8810 Pixel Technology



SNR=13.649 dB

2011 OV8830 Pixel Technology





SNR=17.053 dB

Figure 10. 1.4µm Megapixel Products at 10 Lux

The color image performance of the raw 1.1µm OmniBSI-2 Megapixel development chip is shown in Figure 11 at four different lux levels at 15 fps.

Figure 11. 1.1µm Raw Development Chip 30, 60, 100, and 300 Lux and 15 fps

OmniBSI-2 Reliability

OmniVision's reliability qualification of the 300mm OmniBSI technology requires testing of CLCC packaged parts. The reliability tests include: 1) 1000 hours of High Temperature Operating Life (HTOL) at 125°C, 2) 1000 hours High Temperature Storage (HTS) at 125°C, 3) 1000 cycles of Temperature Cyling (TC) from -40°C to 125°C, 4) 1000 hours of unbiased Temperature Humidity (TH) at 85C/85% RH, 5) 1000 hours of Temperature Humidity Bias (THB) at 85C/85% RH, 6) ESD testing, and 7) Latch-up testing. To date, a set of three separate lots have been tested with zero (0) fails for all tests at all readpoints. Our reliability testing has found no reliability issue associated with OmniBSI-2 technology.

0.9µm SMP OmniBSI-3™ Performance

With OmniBSI-2 in place, it is now possible to continue the pixel shrink to the 0.9µm Sub-Micron Pixel (SMP) pixel technology node. OmniBSI-3 will benefit from more advanced 40 nm design rules, multiple new process modules, more accurate patterning and implant accuracy, faster operation from shrunk transistors and short RC delay, smaller chip size/higher resolution as a result of the smaller pixels size and denser circuitry, new pixel designs, lower dark current, better noise performance, improved isolation technology, and new CFA technology. By moving to 40 nm design rules, the photodiode area can be made large enough to provide reasonable full well capacity at the 0.9µm pixel. By going to a buried channel source follower, the read noise can be improved and dynamic range increased[8]. Our 3D TCAD modeling and simulation of the 0.9µm SMP indicates that reasonable sensitivity performance is possible using OmniVision's proprietary hole detector and RGBClear technologies.

Conclusions

CMOS imagers have gone through an exciting period of process and pixel technology development driven by the need to maintain performance for ever shrinking pixels. To achieve best-in-class performance at the1.1µm pixel size, OmniBSI-2 is an enabling technology. The performance parameters of the OmniBSI-2 1.1µm pixel are better than the first generation OmniBSI 1.4µm pixel. Significant gains in performance are seen when this leading edge technology is ported back onto the larger OmniBSI-2 1.4µm and 1.75µm pixel products. The low cost OmniBSI technology has been successfully transferred to the OmniBSI-2 300mm Cu production line.

Acknowledgements

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References

1 OmniVision announcement, May 27, 2008
2 H. Rhodes et al, 2009 Int. Image Sensor Workshop, 2009
3 S. G. Wu et al, 2009 Int. Image Sensor Workshop, 2009
4 H.-S.P. Wong et al., IEEE Trans. El. Devices, pp. 889-894, April, 1998.
5 H. Rhodes et al., Workshop on Microelectronics and Electron Devices, p. 7-18, 2004
6 Y. Wu, P. Cizdziel, H. Rhodes, SPIE Electronic Imaging Conference, 2009
7 J. Alakarhu, Int. Image Sensor Workshop, p. 1-4, 2007
8 X. Wang et al., Int. Image Sensor Workshop, p. 223-225, 2007