Pixel-to-Pixel isolation by Deep Trench technology: Application to CMOS Image Sensor

A. Tournier, F. Leverd, L. Favennec, C. Perrot, L. Pinzelli, M. Gatefait, N. Cherault, D. Jeanjean, J.-P. Carrere, F. Hirigoyen, L. Grant, F. Roy
STMicroelectronics, 850, rue Jean Monnet – F-38926 Crolles Cedex – France
Tel: +33 4 38 92 21 67 Fax: +33 4 38 92 29 51 E-mail: arnaud.tournier@st.com

Abstract

Deep Trench technology for CMOS image sensor was successfully developed and industrialized for best-in-class 1.4µm pixel Front-Side Illumination (FSI) technology. The performance achievements on QE both on and off-axis without any degradation of other pixel parameters show the need of a perfect pixel isolation for better color fidelity. Comparison with other pixel isolation architectures show that Deep Trench is the best approach to suppress electrical crosstalk.

1. Introduction

In recent years, the resolution increase of CMOS image sensor used for consumer application (mobile phone, digital still camera, camcorder and other mobile devices) has led to the development of technology with pixel sizes down to 2µm x 2µm, and even sub-1µm [1,2].

In this trend, one of the major challenges has become the need to suppress all parasitic charge exchange between neighbouring pixels, also called crosstalk. This crosstalk can cause a loss in image quality.

Crosstalk can be divided in three parts as explained in figure 1.

First, spectral crosstalk is inherent to color filters properties. It corresponds to the signal rejection of color filters in the range of wavelengths where they have to be opaque (i.e. transmission to be zero pourcent)

Then, optical crosstalk corresponds to a photon exchange between neighbouring pixels before electron/holes pairs generation. It mainly appears in back-end stack due to optical mechanisms (reflexion, refraction or diffraction) but can also occur in silicon substrate.

Finally, electrical crosstalk consists in the diffusion of electrical charge (electrons or holes depending the pixel type) between adjacent pixels. It occurs in silicon material due to electrical mechanisms (diffusion and drift).

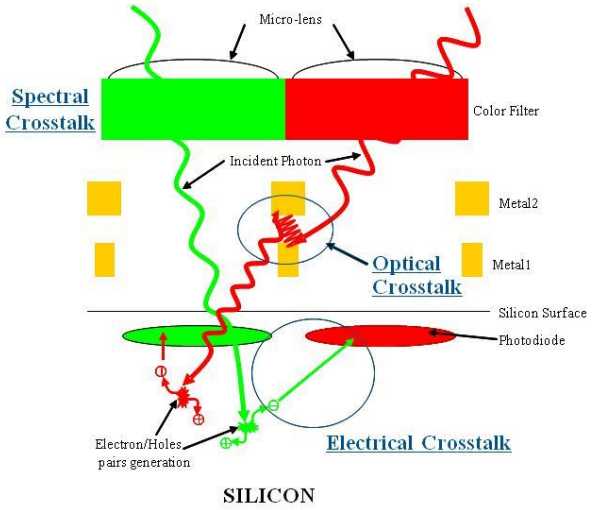


Fig. 1. *Illustration for mechanism of electrical and optical crosstalk in image sensor*

Many pixel isolation architectures have been proposed to suppress this last effect as shown on figure 2.

Starting from a conventional structure [3], a first solution is to isolate neighboured pixels by using dedicated P+ implants with varying energies to create a wall [4]. The purpose is to optimize differently the photon collection for each color and to isolate laterally the pixels.

Another solution consists in the use of adapted pinned deep diode on n-substrates [5]. In this case, the inter-pixel isolation is realized by p-implants at multiple energies and doses, in order to create a junction isolation wall. These isolation walls are said to be 4-11 times more effective than the first solution.

Finally, the pixel isolation can be done by deep trench structure [6]. In this case, it is the interface Si-SiO_2 which is used as a wall against electron diffusion.

In this paper, we will present the successful development and integration of this last solution in a 1.4µm pixel Front-Side Illumination (FSI) technology. We will compare the different isolation solutions described before and will explain the optimization of deep trench depth versus substrate P- epitaxial layer thickness. Angular response and dark current parameters will be also discussed.

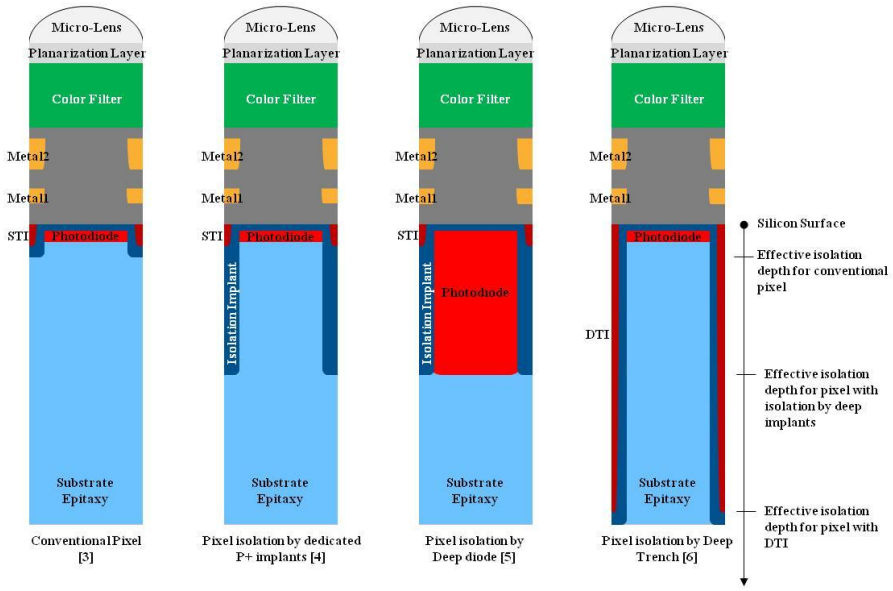


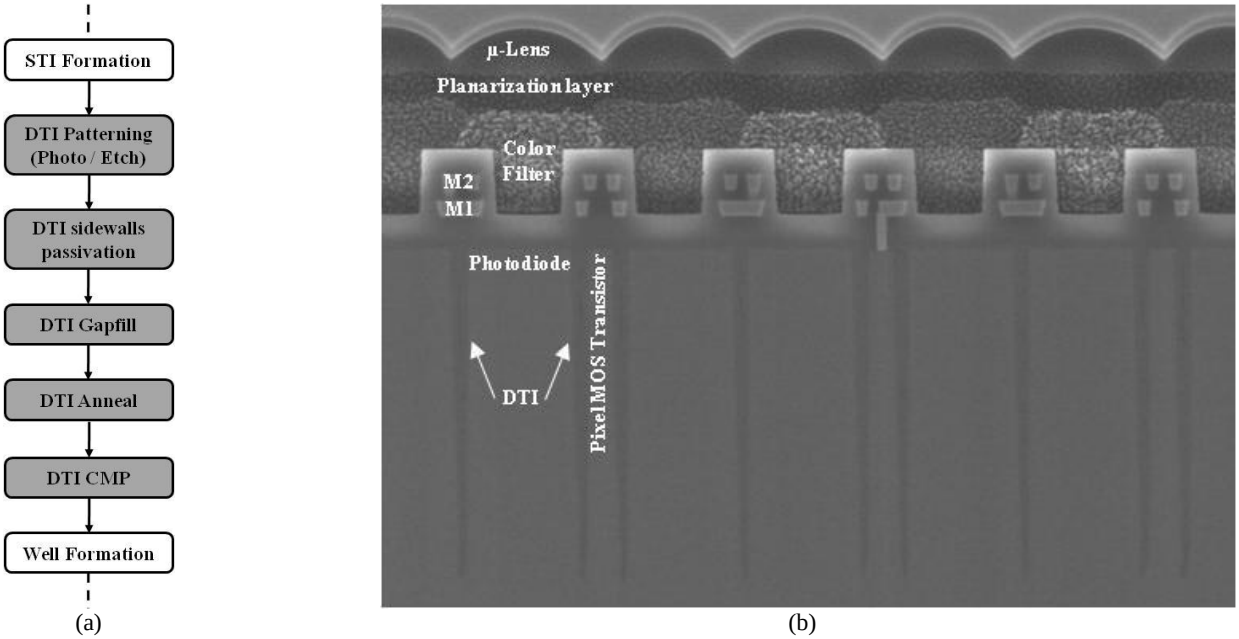
Fig. 2. *Pixel isolation architectures*

2. Deep Trench Process Integration Description

To form Deep Trench Isolation (DTI) between pixels, only one extra mask is needed. A simplified process flow is shown in figure 3a.

DTI formation is performed after Shallow Trench Isolation (STI) formation (for digital area around pixel matrix). Photolithography and Etch process are performed on standard core CMOS tools used for advanced node such as 45nm technology and permit to achieve DTI with an aspect ratio higher than 1:25. Before gapfilling the deep trench, a DTI sidewalls passivation step is needed to avoid any degradation on dark current and white pixel number due to additional interface defects caused by DTI etch. Then standard gapfill, anneal and CMP are realized to finalize DTI formation.

Following this process flow, Deep Trench isolation was integrated in a 1.4µm pixel Front-Side Illumination (FSI) technology. Cross-section inside pixels array is shown on figure 3b. This technology is based on 90nm front-end and 65/45nm back-end process, including 3 metal levels in digital area and only 2 for pixel routing. It also comprises cavity above the pixel array, per-pixel cavity filled by color filter and zero gap micro-lenses to improve as much as possible photon focalization and collection.



(a) (b)

Fig. 3. a) *Deep Trench Process Integration Flow and b) Cross-section view of a 1.4µ pixel in Front-Side Illumination (FSI) technology with pixel-to-pixel isolation by Deep Trench*

3. Quantum Efficiency and Angular Response

With this DTI integration, Quantum Efficiency (QE) for 1.4µ pixel (figure 4) shows equal peaks for Blue, Green and Red pixels, with maximum higher than 50%. Crosstalk is extremely low and permits a great color fidelity to be achieved.

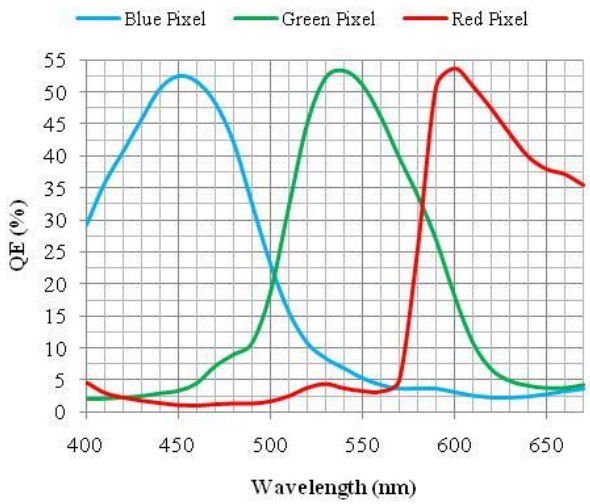


Fig. 4. *QE curve for 1.4µ pixel in FSI technology with pixel-to-pixel isolation by Deep Trench*

This level of performances has been reached thanks to the DTI depth optimization versus substrate P- epitaxial layer thickness, as shown in figure 5.

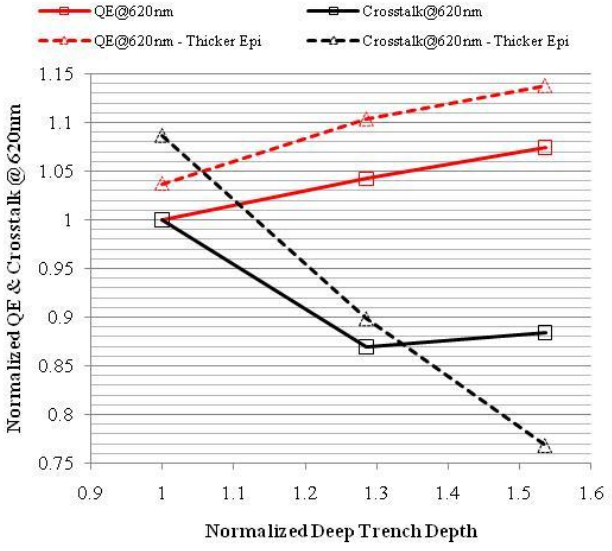


Fig. 5. *QE and Crosstalk versus DTI depth for two different Epi substrate thickness*

It appears that both deeper DTI and thicker P- epitaxial layer permit the increase of QE peak mainly on red wavelength (>600nm) which is in accordance with electro-optical charge generation in silicon. But regarding crosstalk, DTI depth has to be managed according to the P- epitaxial layer thickness in order to avoid any additional electrical crosstalk if P- epitaxial layer is thicker than DTI.

We have also studied the level of performances of each isolation solution described previously in figure 2 and found that the best solution is clearly the isolation by Deep Trench as shown in figure 6.

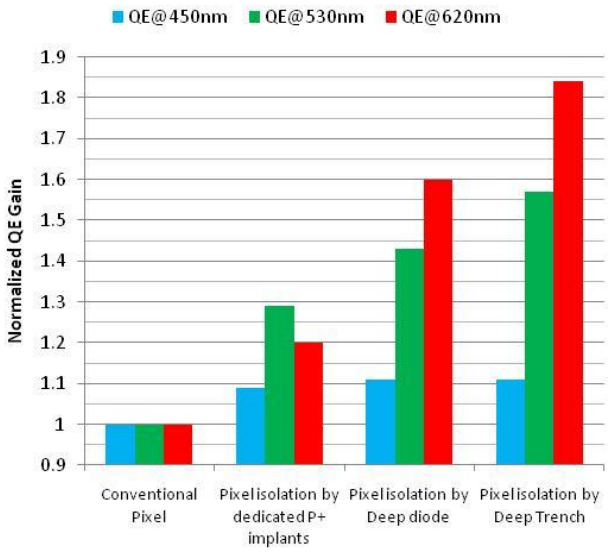


Fig. 6. *QE Gain for different pixel isolation architectures*

The gain between conventional structure and the first solution (use of dedicated P+ implants) is explained by the creation between neighboured pixels of a potential wall of around 160mV leading in less electron diffusion.

For the second solution (Deep N photodiode isolated by p-implants), this effect is strongly increased in the range of 400mV to more than 1V (depending the doping level of each zone) leading to a quiet perfect electrical isolation.

Finally the DTI structure benefit is the possibility to achieve very high aspect ratio isolation and thus a high charge collection volume (i.e. DTI deeper than Deep Diode) leading in QE improvement mainly in Green and Red wavelengths.

In addition to the performances achieved under normal incidence illumination (also called on-axis) and explained before, an other benefit of DTI can be discussed : the performances achieved under non normal incidence illumination (also called off-axis). The merit factor in this case, called Angular Response, can be greatly improved thanks to the waveguide-like structure formed by silicon and DTI (SiO_2-Si interfaces) ensuring the confinement of light inside the silicon as shown in the simulation results in figure 7. This waveguide-like structure at silicon level is due to differences in refractive index between SiO_2 (n=1.5 at 532nm) and Si (n=4 at 532nm), providing an efficient

optical isolation between adjacent pixels which is not present with the 3 latter solutions.

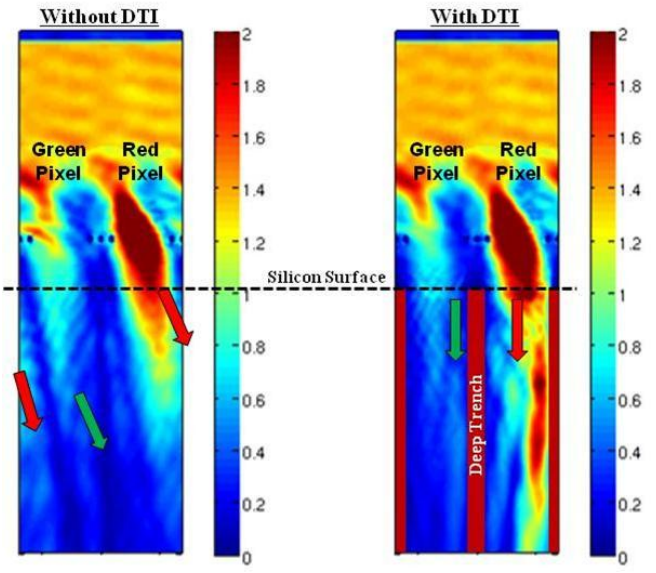


Fig. 7. *Off-axis optical Simulation @633nm of 1.4µ pixel in FSI : Comparison between pixel with isolation by implantation and isolation by Deep Trench*

4. Pixel Dark Current Optimization

Deep Trench Isolation technology involves a large increase of the total Si/SiO_2 interface area into the pixel. This may cause a degradation of the pixel dark current, due to the thermal generation of minority carriers by the oxide interface states. However, this parasitic effect can be prevented when using a carefull DTI sidewalls passivation process, as demonstrated on figure 8.

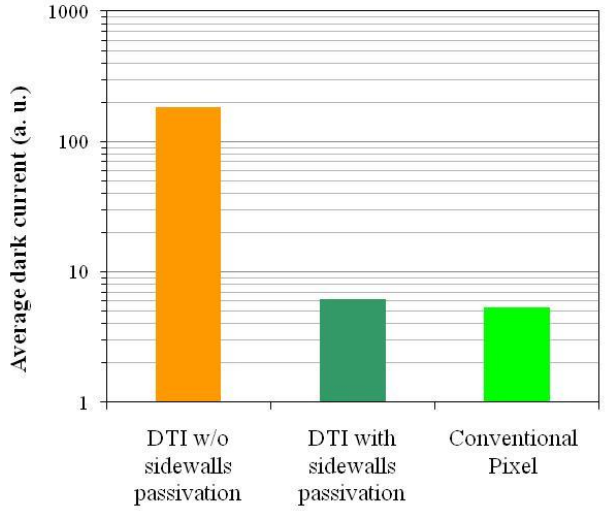


Fig. 8. *Average Dark Current with DTI process optimisation*

Indeed, the SRH theory [7] shows that the generation due to interface defects can be decreased when (i) the interface states density is reduced, and (ii) the remaining mid-gap interface states are permanently filled with the majority carriers. This last condition may be achieved by increasing the silicon doping at the interface. Moreover, the interfaces states density should be minimized using a forming gas anneal process, and the post anneal plasma processes have to be optimized to avoid new damage [8].

Finally, these carefull DTI sidewalls passivation optimizations allow to reach a dark current level lower than 25e-/s at 60°C.

5. Conclusion

Deep Trench technology for CMOS image sensor was successfully developed and industrialized for best-in-class 1.4µm pixel Front-Side Illumination (FSI) technology.

This technology also permits improvement in performance of bigger pixels and will be key for 1.1µm or smaller pixels either in Front-Side or Back-side Illumination (FSI / BSI) technologies.

Acknowledgment

The authors would like to thank the Front-End Manufacturing group of STMicroelectronics for wafers processing. Thanks are extended to all members of the Technology R&D group for their dedicated effort in design, test and process development.

References

[1] J. Ahn et al., "Advanced image sensor technology for pixel scaling down toward 1.0µm", *in IEEE International Electron Devices Meeting (IEDM) Dig. Tech. Papers*, San Francisco, 2008

[2] S.G. Wuu et al., "A Leading-Edge 0.9µm Pixel CMOS Image Sensor Technology with Backside Illumination: Future Challenges for Pixel Scaling", *in IEEE International Electron Devices Meeting (IEDM) Dig. Tech. Papers*, Baltimore, 2009

[3] G. Agranov et al., "Optical-electrical characteristics of small, sub-4µm and sub-3µm pixels for modern CMOS Image Sensors", *in Proc. IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Nagano, 2005

[4] M. Cohen et al., "Fully Optimized Cu based process with dedicated cavity etch for 1.75µm and 1.45µm pixel pitch CMOS Image Sensors", *in IEEE International Electron Devices Meeting (IEDM) Dig. Tech. Papers*, San Francisco, 2006

[5] J. Prima et al., "Improved colour separation for a backside illuminated image sensor with 1.4 µm pixel pitch", *in Proc. International Image Sensor Workshop (IISW)*, Bergen, 2009

[6] B.J. Park et al., "Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7µm Pixel Pitch", *in Japanese Journal of Applied Physics, Vol. 46, No. 4B, pp. 2454-5457*, 2007

[7] W. Shockley & W. T. Read, Jr: "Statistics of the Recombinations of Holes and Electrons," *in Phys. Rev. Volume 87, Issue 5, 1952, pp: 835 – 842*

[8] JP Carrère et al. "New Mechanism of Plasma induced Damage on CMOS Image Sensor: Analysis and Process Optimization", *in Proc. of the 40th European Solid-State Device Research Conferrence (ESSDERC), pp. 106-109*, 2010.