A Review of the 1.4 µm Pixel Generation

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Abstract – **The first 1.4 µm pixel generation CMOS image sensors (CIS) began appearing in consumer-grade downstream products in early 2009 with the majority of small pixel CIS innovators mass producing 1.4 µm pixel devices by the end of 2010. As 1.1 µm pixel generation devices have entered mass production in early 2011, it is worth reviewing the enabling technologies found in real world examples of 1.4 µm pixel devices.**

CIS developers faced a fundamental decision when scaling down from the 1.75 µm pixel generation: whether to extend front-illuminated (FI) technology or to develop back-illuminated (BI, or BSI) sensors. In both cases, the trend for small pixel CIS devices has been the use of more advanced silicon wafer foundries, and a remarkable increase in materials integration and packaging innovation.

Chipworks, as a supplier of competitive intelligence to the semiconductor and electronics industries, monitors the evolution of image sensor technologies as they come into production. Chipworks has obtained charge-coupled device (CCD) and CMOS image sensor (CIS) chips from leading manufacturers and performed structural, compositional, and design analyses to benchmark the technology of the market leaders.

Keywords: CMOS Image Sensors; 1.4 µm Pixels; Back-Illuminated (Backside Illumination); Light Pipes; Pixel Sharing

I. INTRODUCTION

Commercially available 1.4 µm pixel CIS devices from Sony, Toshiba, Aptina, OmniVision, Panasonic, Samsung, and STMicroelectronics have been analyzed [1-8]. These devices are used in mobile (camera phone), digital still camera (DSC) and digital video camera (DVC) applications. Innovation in the areas of pixel architecture, silicon substrate engineering, substrate isolation, light pipes, and wafer fabrication processes will be highlighted.

II. PIXEL ARCHITECTURES AND LAYOUT

A. Pixel Sharing

The migration from 1.75 µm to 1.4 µm generation pixels included updated pixel sharing architectures for most companies. Table I lists the architecture of choice by company and application with an even split between 2-shared and 4-shared pixels. For 2-shared pixel architectures, variants were found with and without row select transistors. OmniVision and Toshiba chose to connect the in-pixel amplifier transistor source diffusion directly to column out busses.

For 4-shared pixel architectures, again variants were found with and without row select transistors. Aptina employed a version of its internal reset control (IRC) pixels to reduce the number of interconnect lines in its FI pixels [9].

TABLE I. PIXEL ARCHITECTURE BY COMPANY

1.4 µm Pixel Device Manufacturer	Pixel Sharing	Architecture	Application
Aptina	4-shared	1.75T effective, IRC	Mobile phone
OmniVision/TSMC (BI[a])	2-shared	2T effective	Mobile phone
Panasonic	4-shared	1.5T effective	DSC
Samsung	2-shared	2.5T effective	Mobile phone
Samsung (BI[a])	2-shared	2.5T effective	DVC
Sony	4-shared	1.75T effective	Mobile phone
STMicroelectronics	4-shared	1.75T effective	Mobile phone
Fujifilm/Toshiba (BI[a])	2-shared	2T effective	DSC

a. BI denotes back-illuminated CIS

B. Pixel Transistor Layout

The inherent competition between pixel transistor footprint and active silicon area in FI devices was somewhat alleviated by the clever use of shared gate poly and clustered transfer gates [10]. Fig. 1 shows the FI device that uses gate fingers which are common to the neighboring shared pixels.

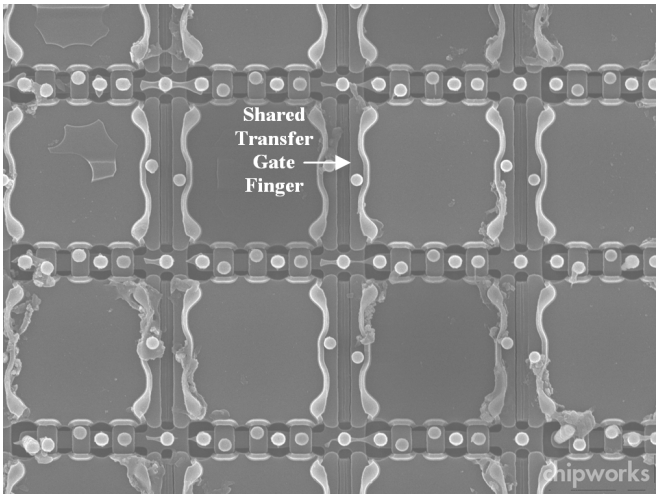

Figure 1. Front Illuminated Pixel Transistor Layout (Aptina)

This approach effectively reduces the number of transfer lines implemented in the back-end-of-line (BEOL) metal interconnect. The efficient arrangement of the gate fingers in long vertical stripes also maximizes the large unobstructed region corresponding to the photocathodes.

Fig. 2 shows a comparatively relaxed pixel transistor arrangement used by a BI device. The BI device scheme enables flexibility in pixel transistor placement and eliminates light obstruction from the pixel BEOL metallization.

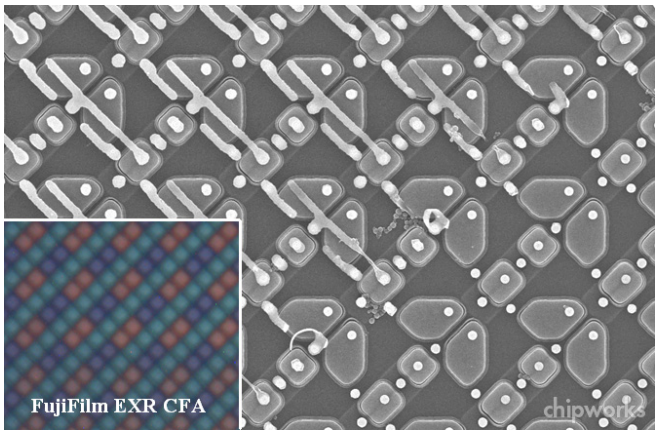

Figure 2. Back Illuminated Pixel Transistor Layout (Fujifilm/Toshiba)

III. Substrate Engineering and Isolation

A. *Front Illuminated Substrates*

While N-substrates have been shown experimentally to improve sensitivity for small pixels [11], both N-type and P-type bulk substrates were used for FI pixels. In both cases, the use of an epitaxial silicon layer was preferred (although not ubiquitous). Beyond the subtle variations of pixel transistor isolation schemes used by each company, the novel use of high aspect ratio, oxide-filled deep trench isolation (DTI) was observed for the first time. This innovation, borrowed from trench DRAM manufacturing, effectively isolates neighboring photocathodes.

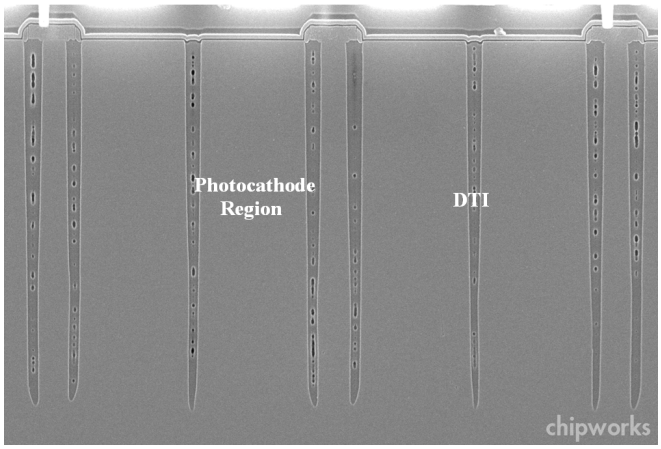

Figure 3. Oxide-Filled DTI for Pixel Isolation (STMicroelectronics)

B. *Back Illuminated Substrates*

Silicon-on-insulator (SOI) and thinned bulk/epi substrates were used for 1.4 µm generation BI devices. The first observed implementation of through-silicon-vias (TSVs) with a BI substrate served to redistribute a back bond pad metallization through the substrate to the front metallization.

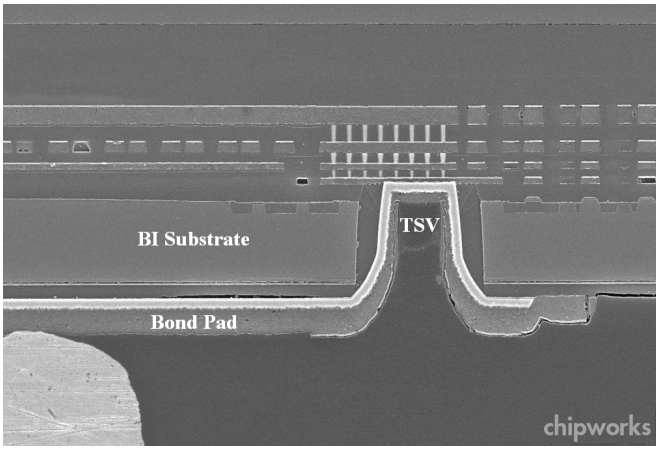

Figure 4. Back Illuminated Substrate with TSV (Samsung)

BI devices continue to evolve with seemingly no consensus on optimal silicon substrate thickness for the 1.4 µm generation. Each manufacturer uses markedly different fabrication processes for the pixel front-end-of-line (FEOL) and BEOL structures. A wide selection of BI specific processes was also noted, including back anti-reflective (AR) layers and metallization. Fig. 5 shows an example of a BI substrate AR layer comprising hafnium and tantalum oxide films.

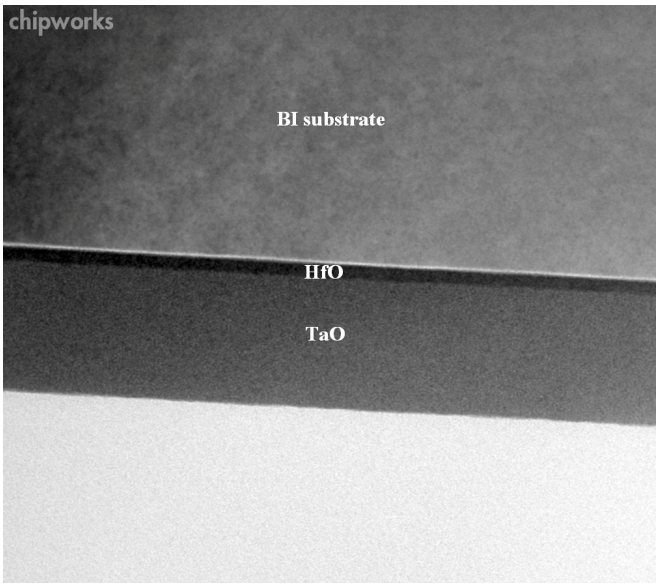

Figure 5. BI Device – Back AR Layer (Sony 1.55 µm Pixel Device)

IV. SELECTED PIXEL BEOL STRUCTURES

Even as BI technology emerges as an enabling technology for future scaling, as of the end of 2010, FI devices dominated socket wins for high-volume mobile phone applications [12]. The practice of optimizing the interconnect for symmetrical layout, which gained momentum at the 1.75 µm pixel generation, was prevalent in all of the observed FI 1.4 µm pixel devices.

Coinciding with the 1.4 µm generation was the use of even more advanced wafer fabs for CIS production. Table II lists the technology generation and back end metallization type by company, and use of light pipes in some FI devices.

TABLE II. BEOL PROCESS FEATURES BY COMPANY

1.4 µm Pixel Device Manufacturer	BEOL Technology Generation	BEOL Interconnect Metallization	Light Pipes
Aptina	90 nm	Al	Yes
OmniVision/TSMC (BI)	110 nm[b]	Al[b]	No (BI)
Panasonic	65 nm	Al/Cu	Yes
Samsung	90 nm	Al	No
Samsung (BI)	90 nm	Al	No (BI)
Sony	90 nm	Al/Cu	Yes
STMicroelectronics	65 nm	Al/Cu	No
Fujifilm/Toshiba (BI)	65 nm	Cu	No (BI)

b. 1st generation device; OmniBSI2 available in 65 nm Cu Process

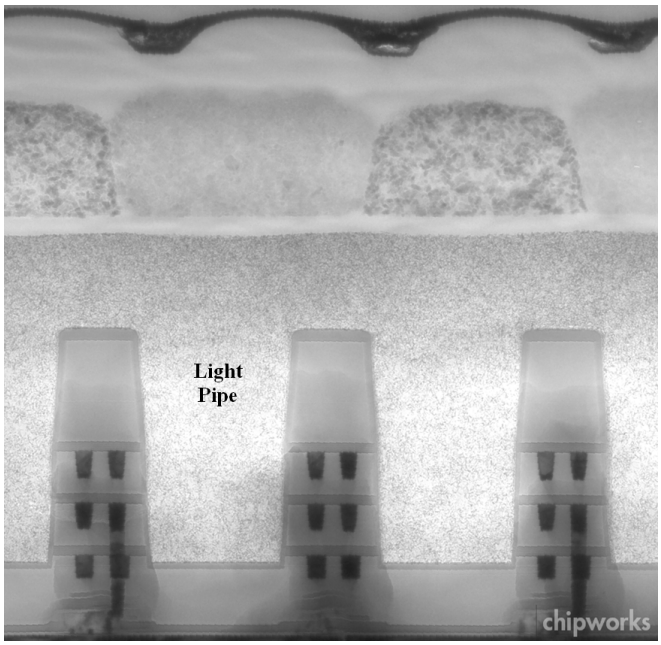

Figure 6. Light Pipe With 65 nm BEOL Cu Interconnect Lines (Panasonic)

The addition of light pipe technology [13] to the pixel BEOL has proven to be an enabling technology for the extension of FI devices for most manufactures. Fig. 6 shows a typical FI device with a fully symmetrical pixel BEOL and a titanium-based light pipe fill. The copper metallization, utilizing 65 nm design rules, introduces minimal obstruction in the pixel BEOL. The narrow lines also facilitate a large light pipe diameter thereby minimizing photon loss through the pixel BEOL.

Another approach continued from the 1.75 µm generation is the practice of thinning the pixel BEOL to improve the pixel angular response. The use of a tungsten local interconnect metal has been discussed as a means of thinning the overall pixel BEOL [14]. Fig. 7 shows an example of a tungsten "metal 0" serving as a floating diffusion interconnect strap beneath the metal 1 interconnect. Even at this lower level, the tungsten metal itself displays some degree of symmetrical layout.

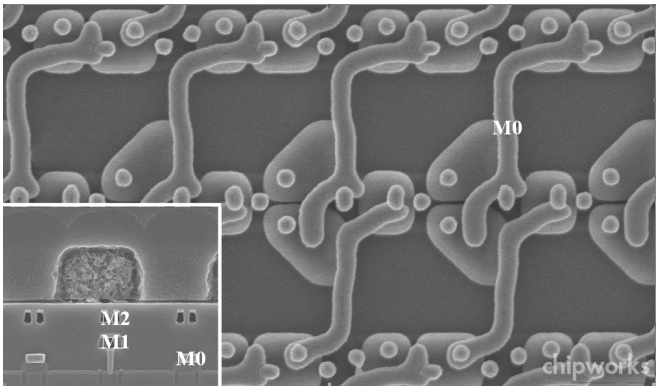

Figure 7. Tungsten Local Pixel Interconnect (Samsung)

Of the two FI devices not employing light pipe technology, one device, shown in Fig. 8, was found to use color filter films to fill the cavities common in the dielectric stacks of devices using copper metallization.

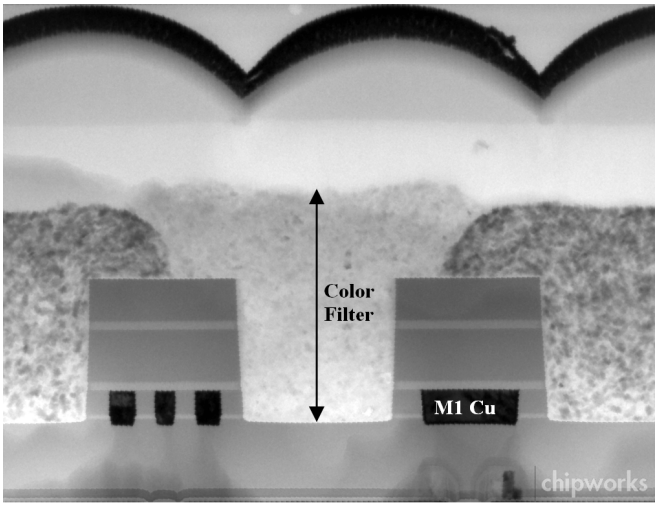

Figure 8. Color Filter Cavity Fill (STMicroelectronics)

V. PRESENT AND NEAR FUTURE TRENDS

Many novel CMOS process technologies have entered production for the recent 1.4 µm pixel devices, and companies continue to incrementally refine this generation of pixel technology. The use of advanced technology generation, high-volume 300 mm wafer fabs seems to be a requirement for future generations of small pixels.

The 1.1 µm pixel generation will almost certainly see the universal adoption of BI technology. The single device of this generation analyzed to date [15] features a 14.6 Mp resolution, 1.12 µm pixel size, and was fabricated using 90 nm design rules. A new, eight-shared pixel architecture (1.375T effective) was employed to facilitate the ultra-compact pixel layout.

Development continues for 0.9 µm pixel generation devices, which are expected to use 65 nm or below design rules [16]. While the BI small pixel scaling trend will continue for the near future, device manufacturers will at some point make another fundamental shift to other approaches including sub-diffraction limit pixels [17]. Beyond silicon, experimentation with quantum dot based image sensors puts forth another option for future innovation. Progress in these and other areas suggests that the acceleration of pixel design and manufacturing innovations will continue for the near future.

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