Low Noise High Dynamic Range 2.3Mpixel CMOS Image Sensor Capable of 100Hz Frame Rate at Full HD Resolution

Paul Vu, Boyd Fowler, Steve Mims, Chiao Liu, Janusz Balicki, Hung Do, Wang Li, Jeff Appelbaum

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, California, USA
Tel: (1)-408-433-2500, Fax: (1)-408-433-2604, e-mail: paul.vu@fcimg.com

Abstract - This paper describes a low noise high dynamic range 1/1.2" CMOS image sensor capable of delivering 100 frames per second in full 1080p HD format. We present the sensor architecture and its measured performance. The sensor features an active area of 2048(H) x 1144(V) 5T pixels with pinned photodiodes, on 6.5µm pixel pitch. The sensor supports both rolling shutter and global shutter readout operations. The maximum frame rate is 100Hz in rolling shutter mode and 50Hz in global shutter mode. In rolling shutter readout, at 100 frames/sec, the read noise is 1.1e- RMS in high gain and 9.7 e- RMS in low gain. The dark current is less than 3pA/cm2 at 25°C, and the MTF at Nyquist frequency (77 lp/mm) is > 0.5 at 450nm. The sensor achieves an intra-scene linear dynamic range of 92dB (41000:1) at room temperature.

I. INTRODUCTION

We have developed a new high-performance full HD format CMOS image sensor featuring a number of enhancements over the sCMOS sensor [1] we introduced in 2009. The sensor supports fully programmable region of interest (ROI) operation. A new function called 'anti-bleed' was also added to improve the overall image quality of the sensor: Anti-bleed works with the row decoder to dump any charge that is accumulated in the rows outside of the ROI, without this function, the extra charge build-up may 'bleed' into the outer rows of the ROI window and degrade the image quality. The image sensor is particularly well suited for demanding low light scientific imaging and night vision applications such as security and surveillance. The design of the sensor was optimized to deliver wide dynamic range, low readout noise at high frame rates, and low power dissipation. In addition, global shutter readout is also supported. The sensor features a 5T pixel architecture with a pinned photodiode coupled with a transfer gate (TX1) to shift signal charge from the photodiode to the floating diffusion sense node, and a 2nd transfer gate (TX2) to dump charge to the antiblooming drain to reset the photodiode. The device supports on-chip correlated double sampling (CDS) in rolling shutter and features high-speed column parallel dual-gain amplifiers coupled with 11-bit single-slope analog-to-digital (ADC) converters. The sensor supports external trigger mode where the sensor internal operation is synchronized to an external trigger signal. The sensor operation is programmable and controlled through a 4-pin SPI control interface. The peak QE is better than 55% at 600nm.

The sensor is mounted in a custom designed ceramic 101-pin PGA package as shown in Figure 1.

The remainder of the paper is organized as follows: in Section II the sensor operation, architecture, and circuitry are described, in Section III the measurement methods and results are presented, and finally in Section IV we conclude the paper.

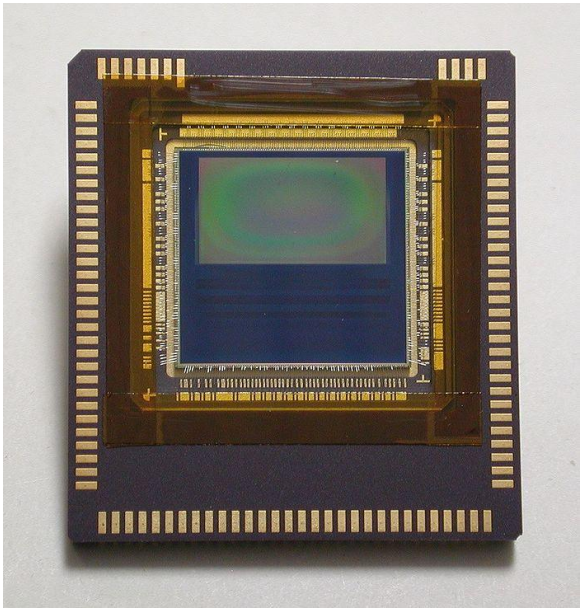

Figure 1. Image sensor in ceramic LCC package

II. SENSOR DESCRIPTION

Figure 2 shows the image sensor block diagram. The image sensor consists of an array of 1920 (H) x 1080(V) 6.5µm pixels, row and column decoders, column parallel high gain and low gain column level amplifiers and 11-bit single slope ADCs, a high speed 22-bit digital readout multiplexer, bias generators, and a bandgap based proportional to absolute temperature (PTAT) sensor. The imager operates at pixel rates up to 282MHz (100fps) and uses standard 1.8V HSTL I/Os for clock and data signals.

The sensor array contains 2.34 million active pixels. Figure 3 shows a simplified schematic of the 5T pinned photodiode pixel. The charge transfer transistor connected to TX1 is used to transfer charge from the pinned photodiode to the floating diffusion node. To optimize high speed performance, the rise/fall times of TX1 can be selected between the default setting of 500ns to a fast setting of 300ns. The source follower transistor size was optimized to minimize read out noise [3]. The reset transistor forces the floating diffusion node to "VRST" when "reset" is high. When "word" is high the source

follower is connected to the bit line and the voltage on the floating diffusion is read out. The transistor connected to TX2 functions as a voltage controlled anti-blooming drain and a global reset device [4].

In rolling shutter operation, the row decoder selects one row of pixels at a time by enabling the "Row select" line in a given row. During that time, the floating diffusion node in the selected pixel is reset, the reset voltage is read out then the transfer gate is turned on, via TX1, and the integrated charge on the pinned photo-diode is transferred to the floating diffusion node. The signal voltage on the floating diffusion node is read out again. The reset and signal voltages are initially stored on the sampling capacitors of both column level amplifiers (high gain and low gain); then the analog data is transferred to a double buffered analog memory (capacitor bank). Then the analog data (stored in the capacitor bank) is digitized using dual 11-bit single slope ADCs. Using the column decoder the double buffered digital data is read out of the sensor. Afterward, the next row is selected and the readout process continues in a similar fashion. The photodiode inside each pixel starts integration once the TX1 transfer gate is turned off. In rolling shutter mode, each row of pixels will have the same integration time, and the time delay between a row being reset and the row being read out defines the integration time. The sensor also supports global shutter readout operation where the active pixel array is first reset and read out, row by row; any residual charge accumulated in the photodiode of each pixel is next discarded using the global TX2 gate; signal charge integration follows next; then at the end of the integration time, TX1 is pulsed globally to transfer signal charge from the photodiode to the floating diffusion sense node of each pixel. The image data frame is then obtained by performing a CDS operation: subtraction of the reset frame from the data frame.

The sensor has a 22-bit digital output port operating at up to 282 MHz. The digital data at the column is transferred to the output pins using a 128:16:1 digital multiplexer. Note that each pixel is simultaneously read out through a high gain amplifier and a low gain amplifier. Both the high gain amplifier and the low gain amplifier outputs are digitized to 11 bits. The maximum frame rate of the sensor is limited by the settling time of the column amplifiers, i.e. 5.4µs. The maximum frame rate of the sensor is 100 frames per second.

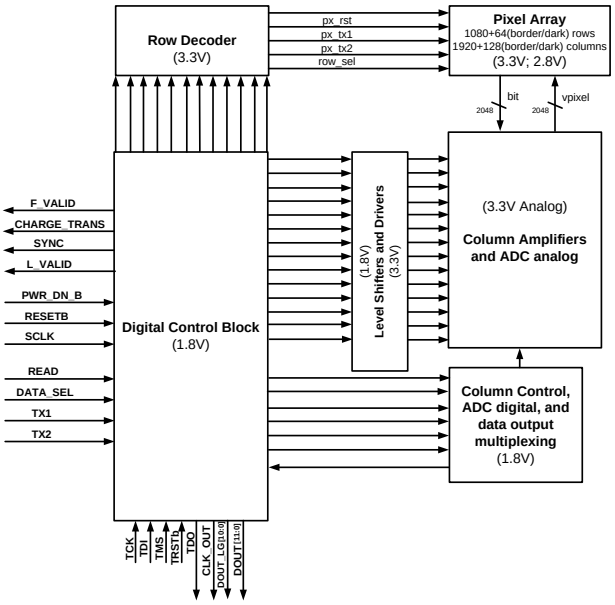

Figure 2. Sensor Block Diagram

Separate power supplies are used for the pixel core, analog amplifiers and ADC, pad ring, and digital circuitry. Common ground is used in the entire chip. A power down pin can be used to shut down all the bias and analog circuits. Internally, a bias reference circuit generates a 100uA bias current which in turn generates different bias voltages for column amplifiers and the pixel array.

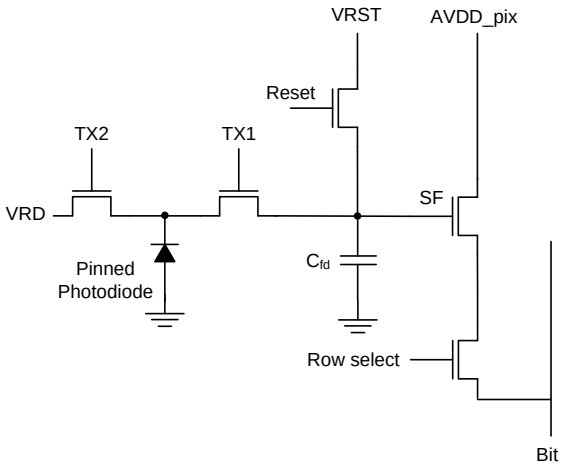

Figure 3. 5T Pixel Schematic

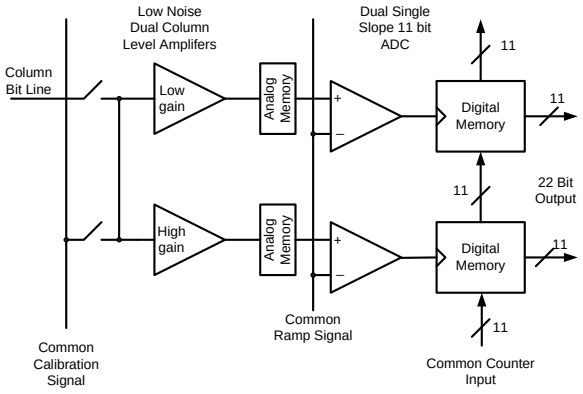

Figure 4. Column level amplifier and ADC block diagram

Figure 4 shows the amplifier and ADC architecture used in each column of the sensor. This architecture was selected to minimize the read noise and maximize the dynamic range simultaneously. There are two amplifiers per column with fixed gains of 30x and 1x respectively. These gain values were selected to minimizing the dip in the sensor SNR when the user switches between the high gain data and the low gain data. Each column also contains two 11-bit single slope ADCs. The amplifier outputs and the ADC outputs are double buffered to maximize the line rate of the sensor. Each column has a reference input that can be multiplexed into the circuit to aid in correcting column level gain and offset fixed pattern noise (FPN). The 22 bit data in each column is transmitted to the output using a 128:16:1 digital multiplexer. The final output data is registered at the output pins to minimize the clock to data skew for high speed operation.

The image sensor supports region-of-interest (ROI) readout, where the ROI window width is programmable in blocks of 16 columns while any arbitrary number of rows can be programmed for the ROI window height. At a particular clock frequency, the output frame rate is inversely proportional to the number of rows in the ROI, and overall power consumption is further reduced when the ROI includes fewer columns.

III. Results

Most of the performance parameters were estimated using a pixel level photon transfer based method [5]. These performance metrics include conversion gain, read noise, full well capacity, linearity, pixel response non-uniformity, dark current, dark current non-uniformity and fixed pattern noise. The QE was estimated using the method described in [6], and the MTF was estimated using the ISO12233 standard. All of the data was collected using a line time of 17.5µs, and integration time was varied based on the measurement. The sensor temperature was not controlled, but it was measured for each data set. The measured sensor parameters are shown in Table 1. A captured image frame is shown in Figure 5.

The high gain channel total noise (read noise plus dark current shot noise) distribution measured at 141MHz (50fps) is shown in Figure 6, the mean value is 1.3 e- RMS and the median value is 1.1 e- RMS. The read noise median and mean values are 0.909 e- and 1.204 e- respectively. The high gain read noise distribution is dominated by pixel level noise sources. These include source follower white 1/f and RTS noise, and transfer gate/coupling noise. The low gain channel read noise median value is 7.35 e-, the mean value is 7.70 e-, and its distribution is dominated by the column level amplifier and ADCs. At the maximum supported clock frequency, 282 MHz (100fps) the median total noise is 1.08 e- with a mean value of 1.35 e- in the high gain channel, and 9.72 e- (median) 10.8 e- (mean) in the low gain channel. Image lag measured at 282 MHz is about 1 e-.

The measured dark current is approximately 5 pA/cm^2 at 25.8°C, and the dark current doubling rate is about 7°C at room temperature.

The quantum efficiency (QE) of the sensor, defined as the number of electrons collected divided by the number of incident photons, is shown in Figure 7. The number of incident photons was calculated based on 6.5µm x 6.5µm pixel area. The peak QE at 600nm is approximately 56% after compensation for reflection loss. Note that all of the QE measurements were performed with a plain window glass cover on the sensor.

The modulation transfer function (MTF) of the sensor is shown in Figure 8. Note that the horizontal MTF is slightly lower than the vertical MTF. The pixel has a metal aperture to protect the readout electronics which results in a slight difference in the vertical MTF and the horizontal MTF. The MTF was measured with a 0.26 NA diffraction limited microscope lens. The sensor MTF was determined by de-convolving the lens MTF from the measured system MTF.

The dynamic range of the sensor, defined as the low gain full well capacity divided by the high gain read noise, is greater than 92dB (41000:1).

Power consumption at the maximum frame rate (100 fps) is 0.8W with both high-gain and low-gain channels operating, while at 50 fps, with a single output channel operating, the power consumption drops to 0.3W.

TABLE I
Sensor Performance
Rolling Shutter Read out at 141MHz

Parameters	High gain channel (30X)	Low gain channel (1X)
Conversion gain (DN/e-)	1.4325	0.0475
Read noise (e- RMS)	0.909 (median) 1.204 (mean)	7.35 (median) 7.70 (mean)
Dark Current (e-/pixel/sec) @ 26C	14.9	9
Full well capacity (e-)	1.3K	37K
Non-linearity (% FWC RMS)	0.4	0.2
Dynamic range (dB)	64 (median)	74 (median)
Max pixel clock (MHz)	282	282
Gain FPN (DN/e-RMS)	0.084	3.9e-5
DSNU (e-/pixel/sec RMS) @ 20C	3.5	3.5
Offset FPN (e- RMS)	13	210

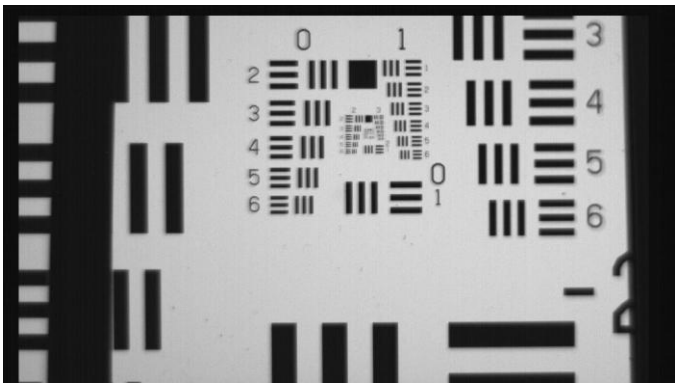

Figure 5. Full frame test image taken at 100fps (282MHz)

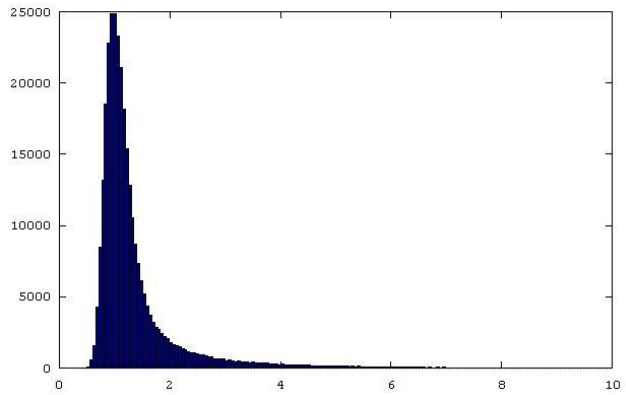

Figure 6. Total noise distribution in high gain channel measured at 141 MHz (50fps)

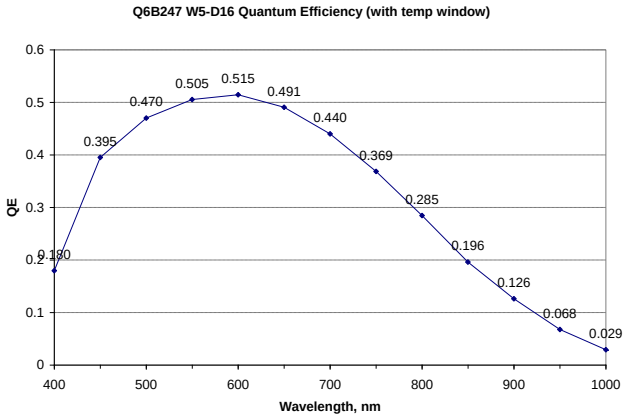

Figure 7. Measured QE of image sensor

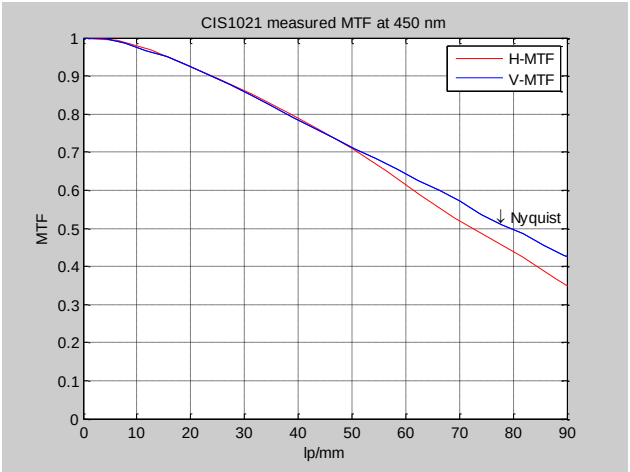

Figure 8. MTF measured at 450nm

IV. CONCLUSIONS

We have presented a high performance 1080p/100fps CMOS image sensor capable of high flexibility in operational modes with very high dynamic range making it suitable for a variety of demanding low light level imaging applications. At 50 fps, the sensor achieves a median read noise of 0.9 e- rms, a dynamic range greater than 92dB, the peak QE is greater than 55% at 600nm, and the measured MTF at 450nm is better than 50%.

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