Backside Illuminated CMOS Snapshot Shutter Imager on 50µm Thick High Resistivity Silicon

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Abstract – Presented is a monolithic 5T backside illuminated snapshot shutter imaging array with 10um pixel pitch. Test structures were integrated in a modified deep submicron CMOS process on high resistivity silicon. Fully processed wafers were thinned to 50um thickness and the backside was passivated and AR coated to provide high quantum efficiency over a wide wavelength range from 400 – 1000nm. Room temperature dark current of 1nA/cm^2 and a peak quantum efficiency of 80% was achieved. The extinction ratio, η_{ext}, was characterized as a function of wavelength. At 640nm, η_{ext} = 120dB could be demonstrated. An analytical model was developed, predicting, in agreement with our measurement results, significant further extinction ratio improvement towards shorter wavelength and degradation to ~60dB towards the silicon cutoff wavelength of 1100 nm. To our knowledge these results are among the best ever reported for a monolithic snapshot shutter pixel.

Index Terms – Backside Illumination, Integrate While Read Snapshot Shutter, Extinction ratio, CMOS Image Sensor, 5T Pixel, Quantum Efficiency

1. Introduction

In order to avoid image artifacts, electronic exposure time control using a global shutter instead of a conventional rolling line shutter is preferred in applications where the time, characterizing the scene or camera motion is comparable to the frame readout time. The ideal performance of a monolithically integrated snapshot shutter pixel is, however, often not achieved. Limitations associated with the operating principle of the underlying devices and the IC manufacturing process may cause light leakage and image lag. Standard front side illuminated CMOS imagers with 3T, 4T or 5T pixel architecture, only achieve a shutter efficiency of 1% to 0.1% [1, 2] which is not sufficient for many practical applications. For example in HDR cameras, low noise readout at high speed and shutter isolation better than 100dB are required to extend the dynamic range using multi exposure time techniques. The shutter efficiency in monolithic imagers can be improved by design [3] or modifications to the baseline CIS (CMOS Image Sensor) process. Design solutions tend to increase the transistor count and therefore the minimum achievable pixel pitch. Small, high performance snapshot shutter pixels will therefore require CIS process modifications, including 3D chip integration. An extinction ratio of 106dB has been achieved for a front side illuminated monolithic imager with a 6T pixel architecture on 14um pitch [3].

Over the past few years, backside illumination technology has been introduced to commercial [4] and scientific [5] CMOS image sensors. In BSI imagers the snapshot shutter leakage mechanisms are different from those in FSI sensors. In particular there are no interlayer dielectrics in the optical path and the silicon sensor membrane is so thin, that multiple path reflections inside the detector must be taken into account. Commercial processes are optimized for very small pixels of 1.4 micron and below and use standard low resistivity Czochralski type silicon wafers. In order to maintain a good MTF in these pixels, the photo sensitive low resistivity silicon membrane must be thinned to less than d=5 micron. However, such a thin silicon layer will only absorb part of the incoming light, especially for wavelengths longer than ~500nm. A BSI snapshot shutter pixel with a storage node on the front side of such a thin silicon layer will therefore suffer high shutter leakage, especially in the red and NIR region. In this operating region most charge carriers are created deeper in the silicon detector which in this case is close to the sense or storage node. In this paper we present results for a backside illuminated 5T (Figure 1) snapshot shutter pixel array with 10 micron pitch, integrated on 50um thick high resistivity silicon in a modified deep submicron CMOS process.

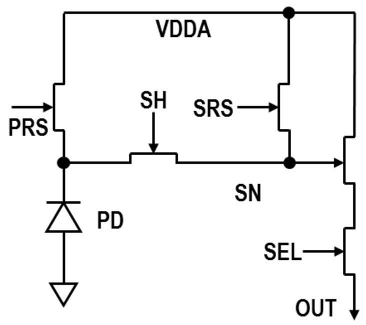

Figure 1 *Schematic of the characterized 5T snapshot shutter pixel. The signal is stored on the sense node, SN, while the signal for the next frame is integrated on the photodiode, PD.*

1. Extinction Ratio Modeling

The extinction ratio of a snapshot shutter pixel is defined as the ratio of pixel responsivity [A/W] in the shutter open versus shutter closed state. Although only the pixel output voltage [V] per incoming illumination power [W] can be measured, the ratio of leakage versus signal charge is estimated in the following analysis. Assuming constant illumination, the photocurrent onto SN and PD will be calculated. In this simplification the difference in conversion capacitance between the shutter open and closed state is neglected. This can be justified considering that the photodiode in our case is of the PIN type and adds very little additional capacitance to the integration node. Nevertheless it should be kept in mind that this simplification will lead to a better extinction ratio in the model than what should be expected in the measurement. In Figure 2 a simplified view of the cross section and layout of our pixel is shown, identifying the leakage and signal currents, $i_{leakage}$ and i_{signal}, respectively. The ratio of leakage charge q_{SN}, integrated on SN during the hold time t_{SN}, to the charge q_{PD}, integrated on PD during the integration time t_{PD} is the extinction ratio, η_{ext}.

$$\eta_{ext} = \frac{q_{SN}}{q_{PD}} = \frac{i_{SN} t_{SN}}{i_{PD} t_{PD}} \qquad (1)$$

The leakage and signal current under constant illumination are determined by the wavelength dependent absorption coefficient $\alpha(\lambda)$, the layout as characterized by the lateral charge collection area A_{SN} and A_{PD} for SN and PD, respectively and the vertical junction depth for SN and PD, parameterized by w and d as shown in Figure **2**. The extinction ratio, $\eta_{ext}(\lambda)$, can then be estimated with the following equation (2):

$$\eta_{ext}(\lambda) = \frac{A_{SN}}{A_{PD}} \frac{exp[-\alpha(d-w)] - exp[-\alpha(d+w)]}{1 - exp[-2\alpha(d-w)]}$$

In this expression, it is assumed, that all photons reaching the front side are reflected and pass through the silicon membrane a second time. Higher order reflections are considered to be negligible, since the detector is 50um thick in our case.

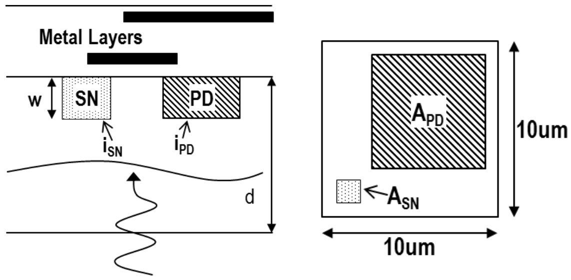

Figure 2 *Cross section (left) of backside illuminated snapshot shutter pixel with sense node SN and photodiode PD. In the conceptual layout view (right), the different size of photodiode, A_{PD}, and sense node area, A_{SN}, is shown. Charges integrated on SN after the shutter is closed, contribute to shutter leakage. The ratio of pixel sensitivity in the shutter closed to open position is the extinction ratio.*

In Figure 3 the simulated extinction ratio is shown as a function of detector thickness, d, for 3 different wavelengths. The extinction ratio, η_{ext}, quickly improves with increasing detector thickness, d, demonstrating the benefit of using a thick silicon detector for snapshot shutter pixels. In the visible domain below 630nm wavelength, extinction ratios up to 160dB should be achievable for 50 micron thick Si detectors.

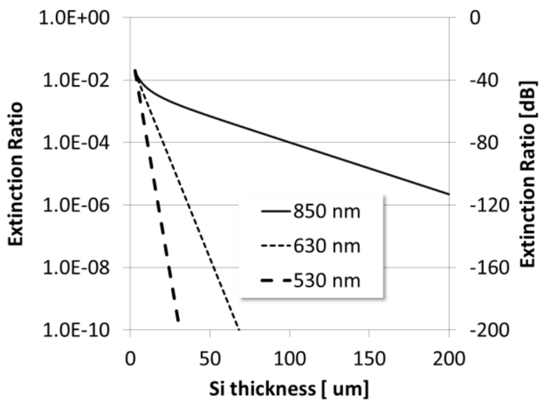

Figure 3 *Simulated extinction ratio, η_{ext}, as a function of detector thickness. In the visible domain up to 630nm, extinction ratios >160dB should be achievable for a 50um thick silicon detector.*

2. BSI Process

The pixels were integrated in a deep sub-micron process with custom modifications using high resistivity silicon. The fully processed CMOS wafers were then thinned to 50um. Next, the backside was passivated and finally an AR coating was deposited to minimize dark current and maximize quantum efficiency over a wide wavelength range. Using large on chip process control photodiodes (PCP) of 1x1mm^2, an average specific dark current of 1nA/cm^2 was measured on wafer at 1V reverse bias and room temperature. A representative IV curve is shown in Figure 4.

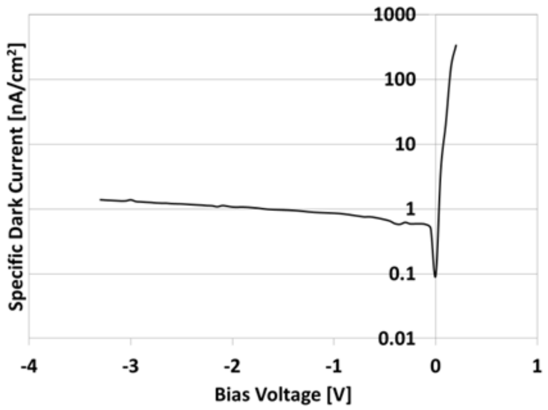

Figure 4 *Dark current measurement of the presented backside illuminated CMOS pixel array. At room temperature and a reverse bias of 1V, the dark current density of our 50micron thick detectors is 1nA/cm^2.*

In order to measure the optical characteristics of our BSI process, single devices were packaged. Because the detectors are thicker than commercial BSI sensors, no handling wafer is required and conventional wire bonding can be used for small devices. A conceptual cross section of our PCP test board is shown in Figure 5. This setup offers to characterize devices with illumination from the front- or backside without the need for any optical window.

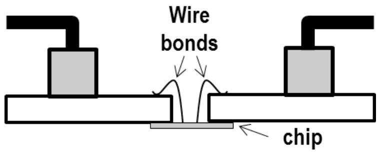

Figure 5 *BSI test chip package using conventional wire bonding. A hole in the board allows illumination from the front- or backside*

These packaged devices were illuminated using a wavelength tunable light spot with a size smaller than 1mm^2. Correct spot alignment was verified through signal response maximization as a function of x and y coordinates. Using a NIST traceable calibration photodiode the power in the light spot was measured as a function of wavelength over a range of 360 – 1100nm. The output signal current of our BSI photodiode was then measured over the same wavelength range and converted into quantum efficiency using the previously recorded calibration data. The result is shown in Figure 6. The photodiodes exhibit high NIR quantum efficiency as a result of the detector thickness and good blue response, indicating the successful passivation of the backside surface.

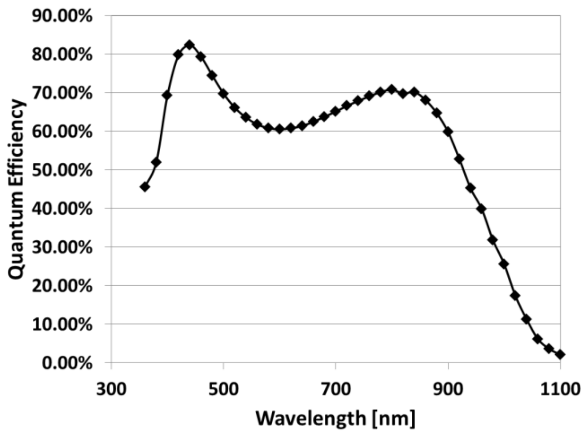

Figure 6 *Measured quantum efficiency of our backside illuminated CMOS technology. High quantum efficiency is maintained over a broad wavelength range from 360 – 1000nm.*

3. Extinction Ratio Measurements

For extinction ratio characterization, a pixel array with 64x80 pixels was packaged on a board similar to the one shown in Figure 5. In this test array, each output and control signal of all pixels is shorted together in order to magnify the effects to be investigated, thereby simplifying the measurements. The schematic of this test array is identical to the one shown in Figure 1.

The extinction ratio is measured by clocking the signals PRS and SH according to the timing diagram shown in Figure 7. The signal SRS is permanently held at the logic low level, SEL at the logic high level. During the t_{PD} phase, the pixel integrates photo generated charge carriers on PD and SN. Our measurements therefore correspond to an Integrate Then Read (ITR) shutter operation. In Integrate While Read (IWR) operation, signal charge would only be integrated on PD, not SN. The extinction ratio in IWR mode will be very similar but the PD capacitance must be increased to achieve good pixel sensitivity.

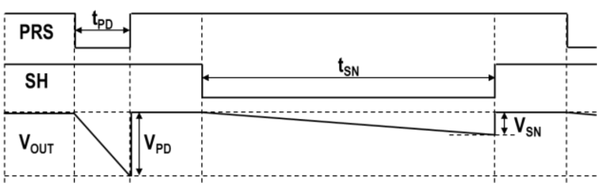

Figure 7 *Timing diagram for extinction ratio characterization. The extinction ratio, η_{ext}, is defined as the ratio in pixel sensitivity during hold time, t_{SN}, and signal integration time, t_{PD}. For constant illumination $\eta_{ext}=(V_{SN}/t_{SN})/(V_{PD}/t_{PD})$.*

With the available flux levels from our spectrometer, t_{PD} was chosen to be ~100usec, t_{SN} was 1sec. The memory hold time t_{SN} of 1sec is limited by our data acquisition system. This is, however, not enough time to create a V_{SN} swing above the noise floor with short wavelength illumination in our present measurement setup. The same illumination creates, however, very fast rise times on V_{out} during the t_{PD} phase with slew rates that can ultimately not be supported by our present test structure. These limitations will be removed in the future.

Programmable timing control, low noise voltage supplies, biases and digital data acquisition was provided to the test array from a separate imager evaluation board shown in Figure 8. This board is prepared to test our imaging arrays with illumination from the front- or backside.

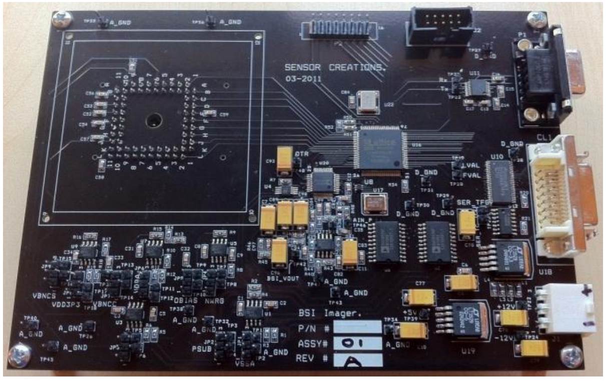

Figure 8 *BSI Imager evaluation board. All biases are digitally controlled via serial interface. Data download is via Camera Link.*

The measured extinction ratio together with simulation results from the presented model is shown in Figure 9. We do not know the exact depth, w, of the SN collection region and a value of 3 micron was chosen to match the measurement results. This is a reasonable distance but may not be accurate. Sense node and photodiode area A_{SN} and A_{PD} for equation (2) were directly extracted from the layout. As can be seen, there is good agreement between simulated and measured extinction ratio results for wavelengths above 700nm. For shorter wavelengths the extinction ratio could not be measured accurately due to constraints in the test structure and our measurement setup as described above.

4. Conclusion

A backside illuminated snapshot shutter pixel on 50um thick, high resistivity silicon was developed, modeled and characterized. The pixel has 100% fill factor, a peak quantum efficiency (QE) of 80% and maintains ~50% QE over a

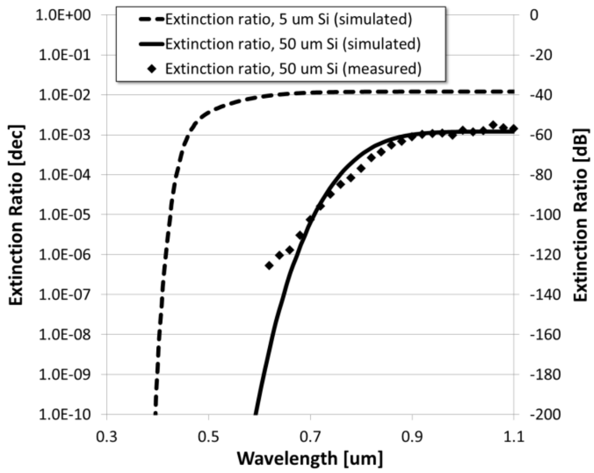

Figure 9 *Measured and simulated extinction ratio of the presented backside illuminated CMOS snapshot shutter pixel. At 700nm the extinction ratio η_{ext} is 100dB. Comparison with the simulated extinction ratio for a 5um thick silicon detector demonstrates the benefit of using a thick silicon membrane in a backside illuminated snapshot shutter imager.*

wavelength range from 400 – 950nm. Our model indicates that the remaining shutter leakage is caused by absorption of photons within a small region around the sense node. Extinction ratios of better than 120dB were measured in the visible domain, establishing one of the best results ever reported for monolithic snapshot shutter pixels.

5. References

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