# Analysis of Front-end Multiplexing for Column Parallel Image Sensors 

Daniel Van Blerkom, Steve Huang, Loc Truong, and Barmak Mansoorian<br>Forza Silicon Corporation, 48 S. Chester Avenue, Suite 200, Pasadena, CA 91106, USA<br>tel: 626-796-1182, email: dvb@forzasilicon.com


#### Abstract

This paper analyzes the scaling of column parallel signal chains for varying degrees of parallelism. As pixel pitches continue to shrink, it has become increasingly difficult to fit the read-out column circuitry in a single column pitch. One approach is to implement a sample and hold in each column after the PGA, and multiplex the gained pixel values into an ADC that is shared across multiple columns. To investigate the trade-offs for different choices of parallelism, we present an analytical model that predicts the layout area, buffer noise and power of designs with different amounts of multiplexing, given a fixed row time. We apply the results of this model to the design optimization of an endoscopic sensor.


## Introduction

CMOS image sensor pixels continue to shrink, with pitches below 1 um now available. This has forced the pitch of the analog signal chain in each column to shrink along with the pixel. When evaluating the impact of reducing the pixel pitch, concerns typically center on the degradation of the QE and crosstalk. A different set of concerns, however, is involved in shrinking the analog column pitch. The values of the sample and hold capacitors used in the column are dictated primarily by the noise requirement. As the column pitch shrinks, the column height must expand in order to keep the total capacitor area the same. For successive approximation ADCs, in addition to kTC noise, the physical size of the smallest unit capacitor also sets a floor to the total area needed by the ADC capacitors, since each successive bit's capacitor is ratioed to the unit capacitor.

If the design rules preclude an efficient layout at the column pitch, the readout can be split between top and bottom banks to allow for a factor of 2 in the column pitch, or the layout can be done on a multiple column pitch and stacked. Neither one of these approaches reduce the total area consumed by the column circuitry, however.

Another approach is to implement a sample and hold in each column after the PGA, and multiplex the gained pixel values into the ADC by means of a switched-capacitor buffer amplifier. In this paper, the parameter M defines the degree of multiplexing in the column, as shown in Figure 1 and 2. As M ranges from 1 to the C , where C is the number of column output lines, the readout architecture spans the range from fully parallel $(\mathrm{M}=1)$ to a serial readout with only one ADC in the design ( $\mathrm{M}=\mathrm{C}$ ). To investigate the trade-offs for different choices of parallelism, we present an analytical model that predicts the layout area, buffer amplifier noise and power of designs with different values of $M$, given a fixed row time.


Figure 1 \& 2: Floor-plan and signal chain for multiplexed front-end.

## Model Description

The first critical input parameter for the model is the row time. Larger values of M require higher speeds from the buffer amplifier. The breakdown of the row time for different values of M is shown in Figure 3. One interesting aspect of multiplexing is the opportunity to overlap timing sequences. The sample and hold stage allows the last ADC conversion within a row time to overlap with the following row's pixel read sequence. Small values of $M$ give the greatest overlap benefit, since the ADC conversion takes a larger portion of the row time. The amount of timing overlap can be found to be:

$$
\begin{align*}
& t_{o}=\frac{a\left(t_{r}-t_{p}\right)}{M-a} \text { for } M>\frac{a t_{r}}{t_{p}}  \tag{1}\\
& t_{o}=t_{p} \quad \text { for } M<\frac{a t_{r}}{t_{p}}
\end{align*}
$$

where $t_{r}$ is the row time, $t_{p}$ is the pixel read time, and $a$ is the percent of the time allotted to the buffer plus ADC conversion that is used for the ADC conversion. The choice of $a$ shifts the settling demands from the buffer amp to the ADC reference driver and the comparator; in practice we have used a value of $80 \%$ to $90 \%$. The time available for the buffer to drive into the ADC is then:

$$
\begin{equation*}
t_{b u f}=(1-a)\left(\frac{t_{r}-t_{p}+t_{o}}{M}\right) \tag{2}
\end{equation*}
$$

We next derive a simplified buffer-amplifier model that determines the noise, power and area of the buffer amp from the settling time allowed. The circuit implementation of the buffer amp is shown in Figure 4, and the key parameters are described in Table 1. The resulting model equations are given in Table 2.


| Name | Description |
| :--- | :--- |
| $C_{i n}$ | Amplifier input parasitic |
| $C_{p}$ | Parasitic capacitance from <br> each multiplexing switch |
| $M$ | Degree of Multiplexing |
| $C_{f b}$ | Feedback \& S/H capacitance |
| $C_{\text {adc }}$ | ADC input capacitance |
| $C_{\text {out }}$ | Amplifier output parasitic |
| n | Time constants for settling |
| m | Time constants for slewing <br> plus settling |

Table 1: Model parameters
Figure 3: Row time breakdown

| Feedback Factor | $\beta=\frac{C_{f b}}{2 C_{f b}+M \cdot C_{p}+C_{i n}}$ | (3) |
| :--- | :---: | :--- |
| Load Capacitance | $C_{L 1}=C_{a d c}+C_{o u t}+C_{i n}+M \cdot C_{p}$ |  |
| Total Settling Time | $C_{L 2}=C_{a d c}+C_{o u t}+\beta\left(C_{i n}+M \cdot C_{p}+C_{f b}\right)$ | (4) $\frac{C_{L 1}}{g_{m}}+(n+m) \frac{C_{L 2}}{\beta g_{m}}$ |
| Input Referred Noise | $v_{n, i n}^{2}=\frac{8 k T}{3}\left(\frac{1}{\beta C_{L 2}}+\frac{\left(C_{i n}+M \cdot C_{p}\right)^{2}}{C_{f b}^{2} C_{L 1}}\right)$ | (5) |

Table 2: Buffer amplifier model equations


Figure 4: Buffer-amp circuit model
The buffer amplifier must drive two voltages into the ADC; first the reset level, followed by the signal level. We assume that driving the reset level requires only linear settling, whereas driving the signal level requires maximum slewing plus settling. The slewing time is found in the manner described in [1].

Making additional assumptions about the capacitances, technology and device lengths, the $g_{m}$, $C_{i n}$, and $C_{\text {out }}$ of the amplifier can be written in terms of the amplifier input device width. The amplifier area and power are also approximated to be linearly proportional to the input device width. The buffer settling time can then be plotted as a function of the device width and the parameter M, as shown in Figure 5. The parameter values used for this example are listed in Table 3.


| Parameter | Value |
| :--- | :--- |
| Technology | 0.18 um CIS |
| $C_{a d c}$ | 2 pF |
| $C_{f b}$ | 400 fF |
| $C_{p}$ | 80 fF |
| n | 7.6 (0.05\% settling) |

Table 3: Parameter values

Figure 5: Buffer settling vs. device width

## Model Application

Applying this model to endoscopic sensor requirements, we were able to identify a value of M that met the area, noise and power constraints while maintaining the sensor frame rate. The model results are plotted in Figure 6, and resulting layout in Figure 7. As M increases, initially the power per column drops as the ADC comparator is shared by more PGAs; but then the settling speed requirement of the buffer amp becomes faster, requiring a larger amplifier with more power. The larger bandwidth, along with the reduced feedback factor of the buffer stage due to increased switch parasitics, leads to higher noise as M increases. The area decreases as the ADC is shared over more and more columns; until, at large values of $M$, the size of the buffer amplifier starts to increase the area per column slightly.


Figure 6: Model results for an endoscopic image sensor


| Description | Model | Device | Unit |
| :--- | :--- | :--- | :--- |
| Total settling time | 100 | 100 | nsec |
| Buffer Power | 2.5 | 2.3 | mW |
| Buffer Area | 18750 | 15000 | $\mathrm{um}^{2}$ |
| Buffer Noise | 400 | 450 | $\mathrm{uV} \mathrm{rms}^{\text {ra }}$ |

Table 4: Model vs. actual device parameters

Figure 7: Layout of area optimized sensor, $M=50$
By optimizing the column area, we were able to fit the digital block and reference generation circuitry in a region under the sample and hold capacitors that would normally be filled with the column parallel ADCs. The buffer amplifier was designed to be fully-differential instead of single-ended; however, the fabricated sensor performance matched the model predictions when adjusted to account for this, as shown in Table 4.

## Conclusion

The human body imposes strict limits on the cross-section of endoscopic instruments, limiting the electrical and optical energy that can be transmitted to the sensor, thus requiring careful tradeoffs between area, power and read noise. The model presented here allows for signal chain multiplexing tradeoffs to be analyzed, and an optimum degree of multiplexing to be chosen given the sensor performance requirements.

## References:

[1] P. J. Quinn, A. H. M. van Roermund, Switched-Capacitor Techniques for High-Accuracy Filter and ADC Design, Springer, 2007.
[2] M. Gustavsson, J. Wikner, N. Tan, CMOS Data Converters for Communications, Kluwer Academic Publishers, 2002.

