

# Prototype line-scan device with 12-bit charge domain column-parallel Successive Approximation ADC

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## Introduction

Different market segments, including industrial vision, demand higher resolution and higher frame-rate imaging devices. The speed limitations of serial ADCs has lead to the development of a diversity of column-parallel ADC architectures.

The Successive Approximation Register (SAR) architecture is one of the concepts used to create high-speed column-parallel ADCs. Typical SAR implementations are equipped with a bank of binary weighted capacitors to generate the comparator reference levels. However, process limitations on capacitor matching can introduce Differential Non Linearity (DNL) errors in the SAR performance characteristics.

In this work a new column-parallel SAR ADC concept, based on a combination of charge redistribution and charge transfer, is investigated. Six equal size capacitors are used to subtract or add accurately binary weighted charge levels from the sampled pixel signal level.

A test-chip was designed in 0.35 $\mu$ m 2P4M technology with column-pitch of 7.4  $\mu$ m. The column-pitch was limited by the design rules of the vertical metal wiring.

The test-chip is equipped with a single line of 3-transistor pixels (7.4 x 149  $\mu$ m<sup>2</sup>) for ADC evaluation purposes.

The ADC circuit performs 12-bit quantization in 1.5  $\mu$ sec and has an input referred noise level of  $\sim$ 400 $\mu$ V.

## Device Architecture

Figure 1 depicts the device column architecture. The OTA stage has a double functionality. First it is used to perform the CDS operation during the pixel signal read-out and secondly it is used during AD conversion to add or subtract charges from the sampled net pixel signal level.

The OTA is equipped with an option for input offset cancellation to secure accurate charge additions or subtractions during the conversion cycles. The offset cancelation circuit is activated by pulsing "Calibrate" high. Pixel and comparator offset cancellation is performed by switching both "SHS" and "SHR" high after the pixel "Reset" has lapsed. By doing so, the OTA is switched in follower mode making the voltage level on its inverting input and output equal to "Vref\_2". This way the offset voltage levels are projected over  $C_9$  and  $C_{10}$  and are stored when "SHR" is switched low.

The net pixel signal is measured by switching "SHS" on during the pixel read-out. The amount of charge transferred to  $C_{7,8}$  during pixel read-out equals the net pixel swing times the capacitance of  $C_{10}$ . A switchable signal-gain can be introduced by making capacitor  $C_{10}$  programmable. When "SHS" is switched off, the signal charges on  $C_{7,8}$  are frozen and the AD conversion can start.

The AD Conversion is performed by measuring the amount of charges stored on  $C_{7,8}$  by subtracting or adding charges via a binary search algorithm. The binary weighted charges for this AD Conversion process are delivered by the Capacitor Bank connected with the inverting OTA input.

Figure 2 depicts the detailed schematic of the Capacitor Bank together with the connected OTA stage. Basically there are three sets of equal size capacitors  $C_{1,2}$ ,  $C_{3,4}$  and  $C_{5,6}$ . The capacitors  $C_{1,2}$  and  $C_{5,6}$  are charged, during pixel read-out (SHS=on), with opposite polarity to the voltage difference between "Vref\_1" and "Vref\_3". Capacitor  $C_{3,4}$  is discharged to "Vref\_2" during this period of time.

Figure 3 depicts the required timing waveforms for read-out of the line-scan device and Figure 4 shows the charge levels on the capacitors in the Capacitor Bank together with the OTA output signal at the end of the successive conversion cycles. The different timing moments are marked (a) to (e) and are indicated in the figures:

- Switches "Charge" and "Parallel" are closed. Capacitors  $C_{1,2}$  and  $C_{5,6}$  are charged to the differential voltage between "Vref\_1" and "Vref\_3". Capacitor  $C_{3,4}$  is completely discharged. The comparator output is initialized by pulsing "Init" high, to secure a correct start of the Successive Approximation algorithm.
- Switch "Equalize" is closed to connect the bottom plates of  $C_{1,2}$ ,  $C_{3,4}$  and  $C_{5,6}$  with "Vref\_2".
- Switches "Parallel" and "Share\_P" or "Share\_N" are closed. The comparator output level decides whether the "Share\_P" or "Share\_N" switch is closed. The comparator output is initialized at the start of the AD conversion to secure that "Share\_P" is closed for the first conversion cycle (MSB). Charges as initially stored on  $C_{1,2}$  are redistributed between  $C_{1,2}$  and  $C_{3,4}$ . Since both capacitors have equal size, each capacitor carries 50% of the initial charges.

- d. Switches “Transfer” and “Discharge\_P” or “Discharge\_N” are closed. The comparator output level decides whether the “Discharge\_P” or “Discharge\_N” switch is closed. The comparator output is initialized at start of AD conversion to secure that “Discharge\_N” is closed for the first conversion cycle (MSB). MSB charges on  $C_{3,4}$  are transferred to  $C_{7,8}$  resulting in a negative going swing at the OTA output. By closing “Discharge\_N”, 50% of the charge on  $C_{5,6}$  is drained to “Vref\_2” to balance the remaining charges with the charges on  $C_{1,2}$ .
- e. Rising edge on “Clk\_bit” to latch the comparator output. A slightly delayed version of “Clk\_bit” is applied to the shift register to secure proper data capture.

Steps (c) to (e) are repeated for the successive conversion cycles. Depending on the previous comparison result, charge redistribution to  $C_{3,4}$  happens from  $C_{1,2}$  or  $C_{5,6}$ .

Figure 4 (g) shows that for this example the MSB conversion cycle was resulting in a too high voltage swing at the OTA output. As a result charges from  $C_{5,6}$  are distributed with  $C_{3,4}$  for the next conversions cycle. The 12-bit conversion is performed via 12 successive cycles.

After the conversion is lapsed the quantized pixel data is copied to a shadow register by clocking “Clk\_db” high.

Figure 5 depicts a photograph of the test-chip on the wafer.

## Conclusion

A 12-bit column-parallel SAR ADC architecture was implemented using six equally sized capacitors. The architecture is based on a charge transfer concept and enables easy integration of the CDS functionality, signal gain and AD Conversion around a single OTA stage. The column-pitch is limited by the metal layer design rules of the 0.35 $\mu$ m 2P4M process.

## Performance Summary Test device

Parameter	Specifications
Technology	0.35 $\mu$ m 2P4M
Column pitch	7.4 $\mu$ m
Number of columns	192
Pixel dimensions	7.4 x 149 $\mu$ m <sup>2</sup>
Conversion depth	12-bit
ADC input swing	1.2 V
ADC input referred Noise	400uV
Conversion time	1.5 usec
Power Consumption	80 uA / 3.3 V
DNL	< 2 DN
INL	< 1%

## References

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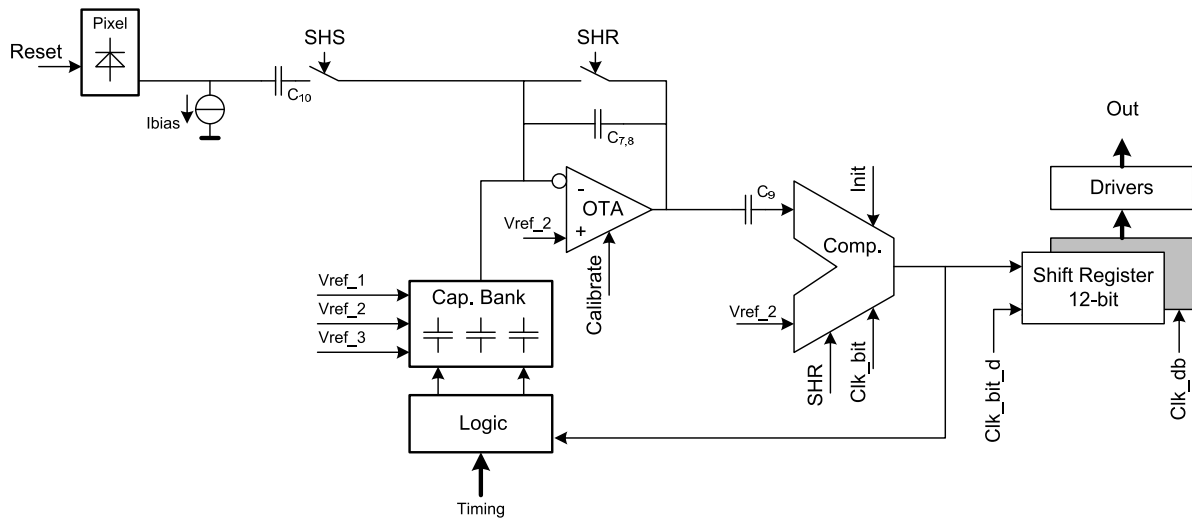


Figure 1 Column architecture

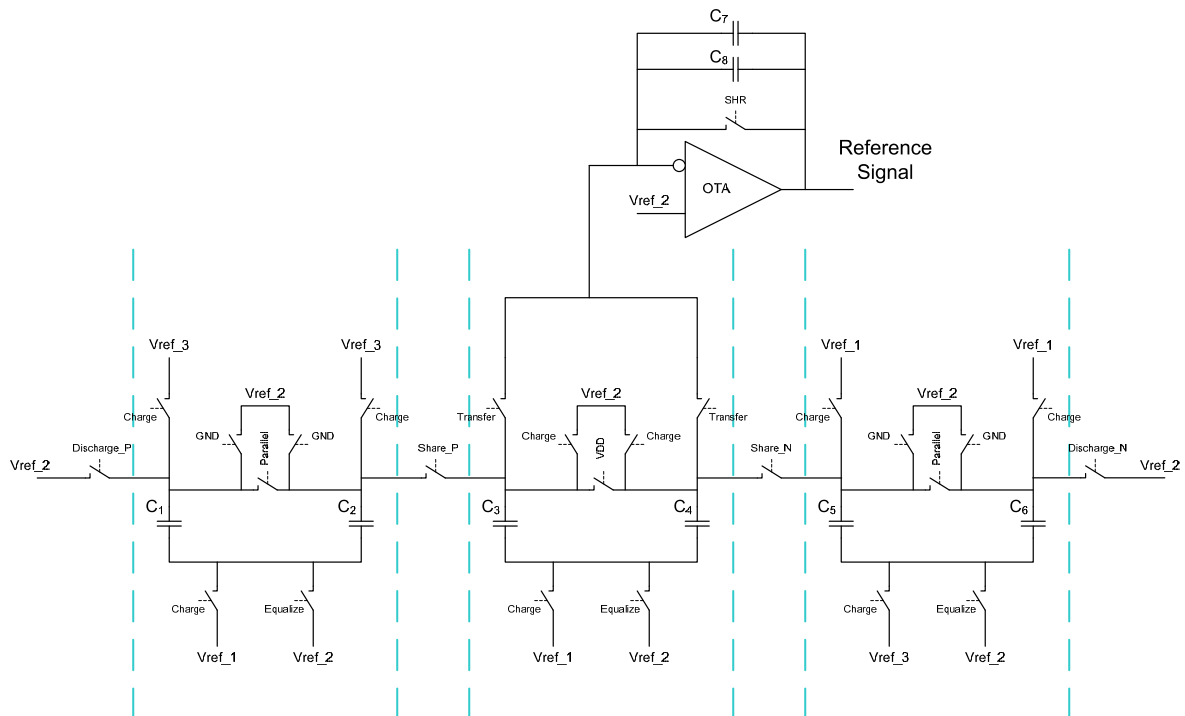


Figure 2 Capacitor Bank details

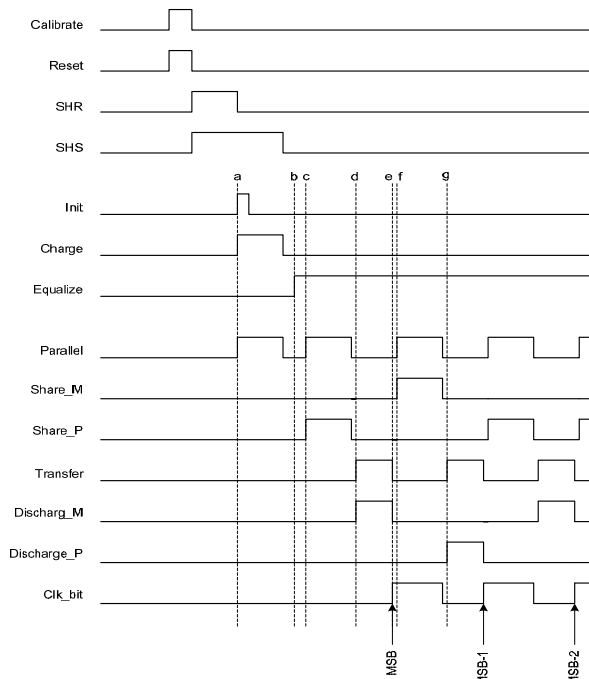


Figure 3 Timing waveforms

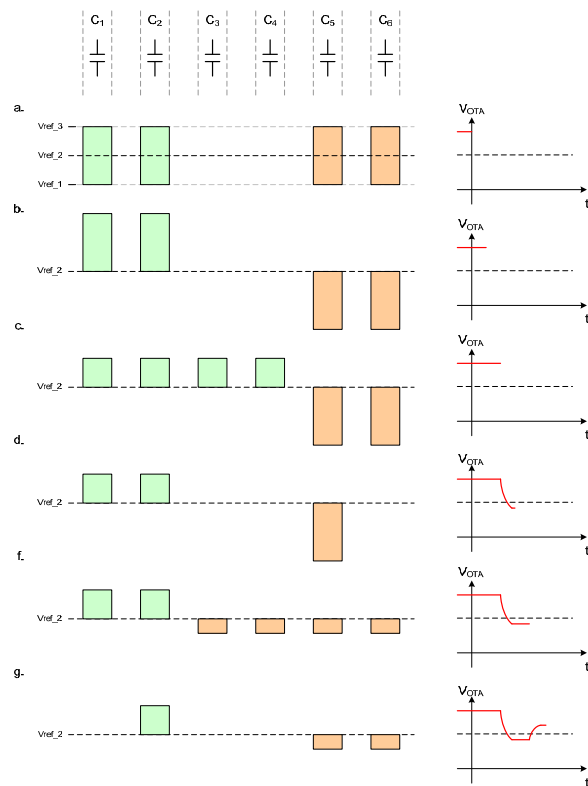


Figure 4 Capacitor charge levels and OTA output signal

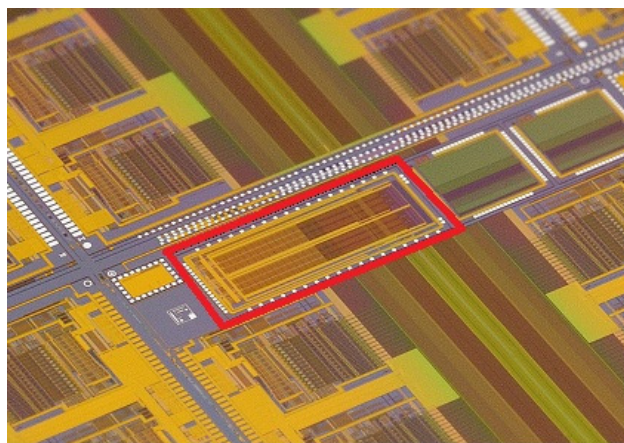


Figure 5 Photograph of chip on the wafer