[P10] Post-ADC Digital Filtering in the CIS with the Column Single Slope ADC

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ABSTRACT

This paper presents a post-ADC digital filtering technique to reduce the temporal noise by exploiting the comparator transition patterns in the column single slope ADC in the CIS. The de-noising schemes do not impose additional conversion time. A simulation was conducted to analyze the effectiveness of the schemes. A test element has been fabricated using CMOS 0.18-μm single-poly five-metal (1P5M) process as a part of 4K-pixel 3T photodiode CMOS image sensor. The comparator transition patterns are digitally processed and the de-noising performances are compared. The measurement results from the test element shows that the suppression of the signal to noise ratio effectively improves by 0.57-bit of accuracy.

Keywords: Column single slope ADC, Post-ADC processing, De-noise, CMOS image sensor.

1. INTRODUCTION

The single slope ADC architecture is widely used in commercial CISs from small size [1], [2] to very large number of pixels for the professional cameras [3]. One of reasons for the wide variety of application is due to the inherent simple column circuit structure that is indeed scalable as the pixel pitch becomes smaller [4]. However, because of its simplicity, the column single slope ADC is sensitive to the temporal noise caused by the power/ground bounce, the intrinsic noise such as thermal, shot and 1/f of the reference ramp driver and comparator, and the clock jitter [5]-[7]. It is because any input voltage fluctuation close to its threshold voltage of the comparator affects directly and yields false ADC codes. Assuming sampled photodiode signal is to be compared with the ramp signal and no fluctuation; all temporal noise is aggregated to the ramp reference signal, the noise presented at the comparator input converts the noise amplitude and frequency characteristics to various comparator output transition patterns. Thus if the noise probability density function (PDF) of the aggregated noise is known, the dynamic signal to noise ratio can be improved by estimating the true value. Fig. 1 shows the correction model, in which the sampled photodiode signal (regard as the true value), V_{IN}, is compared with the ramp signal, V_{RAMP}, affected by the aggregated noise, δ, and the comparator output is input to the ADC code memory to store the first or last comparator transition (regarded as a DC offset) and the noise estimator, $E(*)$. Then the true value estimation, $\hat{D}_{OUT}$, is calculated by subtracting the estimated noise from the non-filtered ADC code. This estimated noise value provides the average difference between the non-filtered ADC code that is affected by the noise, and the true value. As explained in the section 2, it is equivalent to have the photodiode signal be affected by the noise, ε, and removing the ramp signal for simplicity. Then a formula can be found by the representing it in the symbolic expression.

$$\hat{D}_{OUT} = g(V_{IN} + \varepsilon) - E(g(\varepsilon)) = g(V_{IN}) + g(\varepsilon) - \hat{g}(\varepsilon) \approx g(V_{IN}) \tag{1}$$

Note that $g(*)$ represents the comparator transfer function; the function is assumed linear time invariant. D_{OUT} and $\hat{g}(\varepsilon)$ indicate the non-filtered ADC code and the estimated noise, respectively. The first or last comparator transition ADC code is affected by the noise greatly and stored as D_{OUT}. This noise itself can not be estimated with a simple circuit and an algorithm, however the noise average that is the center of the random noise can be estimated by processing the noise-affected comparator outputs. Since the noise average can be regarded as the true value without the DC offset as explained in the section 2, by subtracting it from the DC offset; pushes back the final transition ADC code close to the true value. So the key point is how to estimate the noise average precisely using a small number of the comparator transition patterns which are stored in the noise estimator.

We propose the de-noising scheme using the arithmetic operation with the comparator transition patterns and the circuit structure that sustains the simple column layout and stringent area constraints without increasing the conversion time.

2. NOISE ESTIMATION ALGORITHM

The comparator output pattern reflects the temporal noise introduced at the inputs of the comparator, which are traditionally discarded. Closer to the sampled photodiode signal voltage, more frequent comparator output transitions are likely to occur. It is because that the noise of the ramp reference signal has the PDF of the white Gaussian distribution, the total noise PDF around the comparator threshold would be, due to its additive property, also the sum of the white Gaussian distribution among

each ramp steps of those cross the threshold as shown in Fig. 2. In case of the column single slope ADC, the ramp reference signal is constantly changing, thus a number of available samples are inevitably little. The simplest estimation method is an average of the first and last transition ADC codes, $g(V_{IN}(0))$ and $g(V_{IN}(N\text{-}1))$, respectively as described in (2).

$$\hat{g}(\varepsilon) = g\left(V_{IN}(N-1) - V_{IN}(0)\right)/2 \tag{2}$$

To keep the column circuit simple, the formula that uses only two samples are chosen. Although the arithmetic average is the best estimator in case of abundant observed data, the centroid as described in (3) is expected to give less estimation error, as it uses all the observed samples, which are usually more than two.

$$\hat{g}(\varepsilon) = \sum_{k=0}^{N-1} W(k) \cdot g\left(V_{IN}(k) - V_{IN}(0)\right) \Big/ \sum_{k=0}^{N-1} W(k) \tag{3}$$

Note that $W(k)$ is the displacement number from the first transition ADC code. From the aforementioned analysis, it is considered that the true value lies around the center of the transition patterns; that is the average of the noise. Using this a-priori information, a roughly defined weight function such as a triangle-shaped, can be applied to honor the transitions near the center so that the estimation error becomes less in a situation where only limited number of samples is available.

3. SIMULATION RESULT

To verify the proposed de-noising performance, an image simulation has been conducted using the white Gaussian noise generator. The 8-bit standard image of 256x256 in size was used as the true value image and the single slope operation (8-bit ramp mode) was emulated to re-digitize the original image, in which 16-comparator outputs are kept and used for the correction operation. The PSNRs of the two proposed schemes and non-filtered are plotted in Fig. 3 along with added noise of standard deviations in LSB. A few important observations can be derived from the plot. As the superpositioned white Gaussian noise becomes larger, the drooping of the non-filtered PSNR becomes more prominent compared to the proposed correction schemes. However, the PSNR difference becomes saturated around 5-dB as the deviation increases; this indicates that if the noise deviation is more than the length of the transition memory, the correction performance degrades in similar fashion. Secondly, there is almost no PSNR difference in case where the deviation is less than 1-LSB. Lastly, the performance differences among two schemes are almost negligible but slightly the centroid scheme shows better performance.

4. COLUMN CIRCUIT STRUCTURE

We have developed a test chip to verify the performance of the de-noising scheme. The test structure was designed to measure the comparator output transitions of the two schemes; thus not full circuitry including the correction logic has been implemented. Fig. 4 shows the column circuit structure implemented as a part of the CIS. The D Flip Flop (DFF) -base 16-bit column First-In-First-Out (FIFO) memory resides on each column to capture the comparator transitions up to 16-sample. The number of sixteen may or may not be appropriate depending on the expected noise variance, as described in previous section that if the noise is much larger than the FIFO length, the correction operation starts to degrade the performance. The clock to the column FIFO memory is synchronized to the ramp reference generator circuit clock so that it can capture all comparator output transitions up to 16-cycle starting from the first transition. The clock gating circuit is implemented to automatically hold the shifting operation when the first transition is detected after 15-cycle later. This will ensure no-loss of the transition patterns. The FIFO memory is read out in parallel to reduce the readout time. The correction circuit itself is to be implemented, for example, at the forefront of the digital data path. Along with the column FIFO memory, the latch circuit for the normal ADC code is implemented to store the first or last transition code.

The algorithm test circuit structure used to characterize the de-noising performance only consists of the comparator shown in Fig. 4; this is to measure all output transitions using the evaluation board and avoid column-to-column FPN.

5. MEASUREMENT RESULTS

The measurement procedure is as follows. The DC input voltage and ramp reference signal from the external DAC are presented at the inputs of the comparator. The comparator operation is about 100K samples per second and all outputs are captured. 2048-conversion results are gathered and applied each correction method on a test bench PC. The noise is intentionally added at the ramp reference signal to see the effect of the de-noising more clearly. Fig. 5 shows the results of the correction schemes. The first and last non-filtered indicate the first and last transition codes, respectively. They show widely-spread tail distributions. Its standard deviation is 7.78-LSB. On the contrary, the average and centroid schemes have sharp peak occurrence and small tail distributions. Their standard deviations are 5.23-LSB and 3.69-LSB, respectively. As expected, larger temporal noise is suppressed most by the centroid scheme.

The different ramp step voltages have been applied to see how the correction performance changes and the results are shown in. Fig. 6. As predicted by the simulation, when the temporal noise deviation is within a ramp step voltage, there is no additional improvement observed. Within 1-LSB deviation range, the average and centroid schemes stays low whereas the non-filtered goes up quickly. After 1-LSB deviation range, the difference becomes more severe. The centroid scheme is tolerant to the temporal noise than the average scheme. The maximum performance obtained is 1/1.48 times in deviation; thus it corresponds to 0.57-bit of accuracy improvement.

The DNL and INL (not shown) have also been measured using the histogram testing method with 48K samples to see any effect is occurring by the de-noising scheme. The DNL and INL have no noticeable difference between Non-Filtered and the two schemes. The peak DNL is 0.46/-0.49-LSB and the peak INL is 1.72/-3.02-LSB. A sample image obtained by the column ADC output is depicted in Fig. 7 for a reference.

6. SUMMARY

The two de-noise schemes using the arithmetic operation for the column single slope ADC in the CIS have been presented. The image simulation and the measurement results agree each other and it clearly shows that the improvement of the dynamic noise suppression by 0.57-bit of accuracy. These schemes require additional FIFO memory in a case of the test chip on each column to observe the comparator transitions along with the ordinary ADC code latch circuits. Future work will be oriented to combine it with the digital correlated double sampling circuit to realize more practical solution for the single slope ADC in the CIS and the theoretical approach to boost more correction efficacy.

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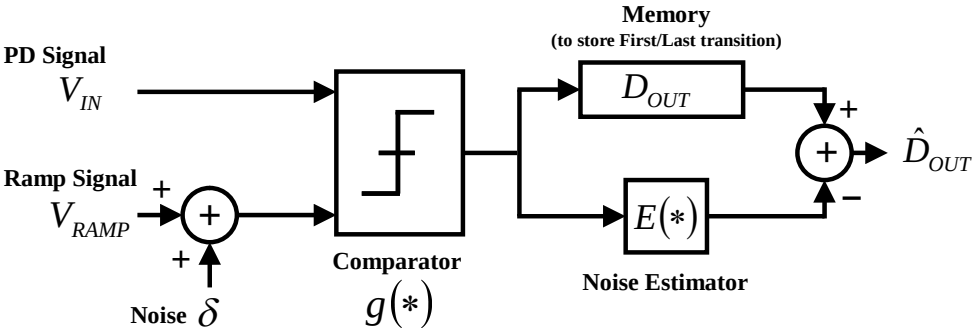


Fig. 1. Correction model used to build the algorithm.

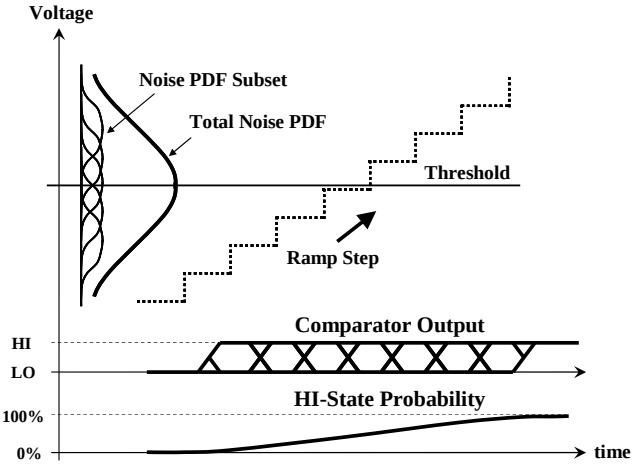


Fig. 2. An illustration of he total noise PDF around the threshold and the comparator output transition period.

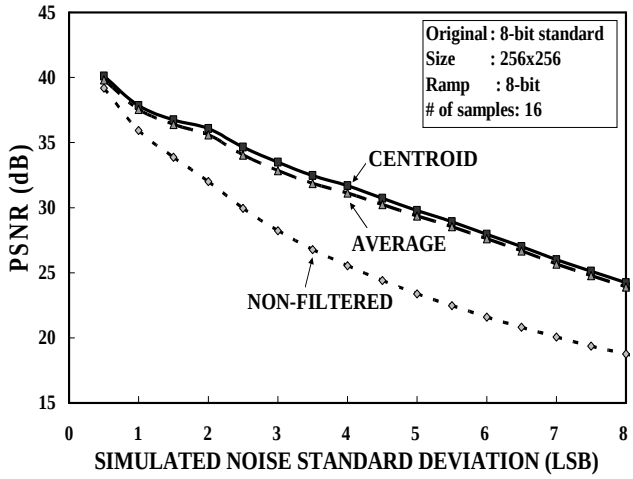
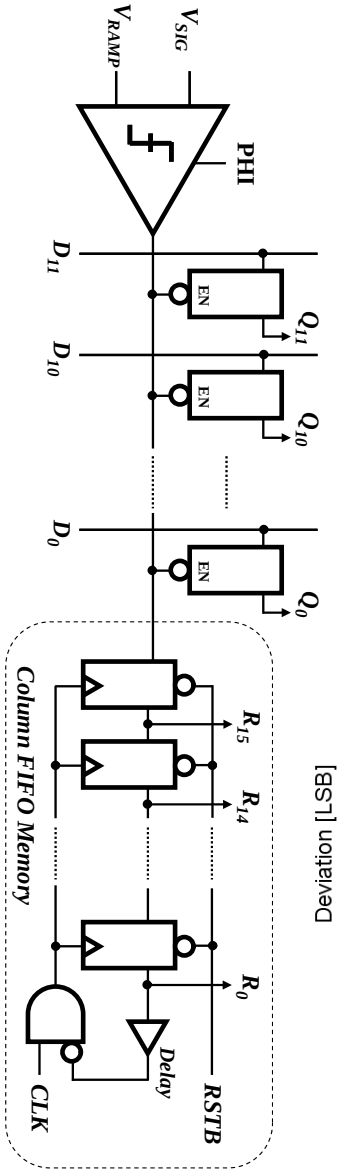


Fig. 3. De-noising simulation result.



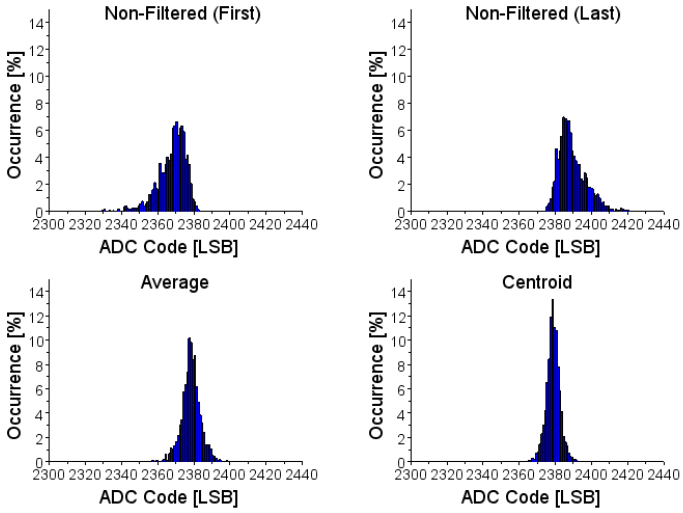


Fig. 5. Transition codes histograms (noise is intentionally added to the ramp signal to see the differences more clearly).

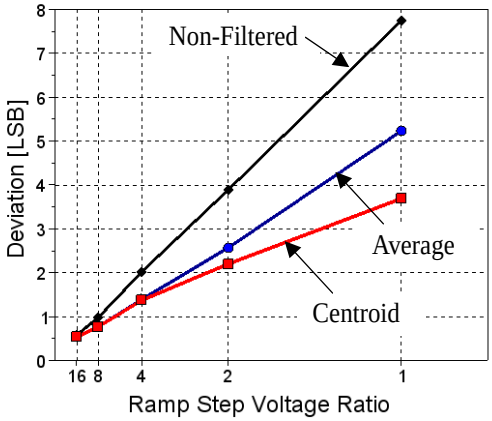


Fig. 6. De-noising performance change along with the ramp step voltage ratio.

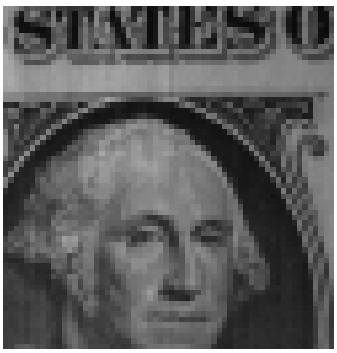


Fig. 7. Sample output image. (4K-pixel, 200% magnified.)

Fig. 4. Implemented column structure.