P9

Column-Parallel Circuits with Digital Correlated Multiple Sampling for Low Noise CMOS Image Sensors

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ABSTRACT:

This paper presents a low noise CMOS image sensor using column-parallel high-gain signal readout and digital correlated multiple sampling (CMS). The sensor used is a conventional 4T active pixel architecture with a pinned-photodiode as detector. The test sensor has been fabricated in a 0.18μm CMOS image sensor process from TSMC. The random noise from the pixel readout chain is reduced in two stages, first using a high gain column parallel amplifier and second by using the digital CMS technique. The dark random noise measurement results show that the proposed column-parallel circuit with digital CMS technique is able to achieve 127 μV_{rms} (2.8 e^-) input referred noise. The significant reduction in the sensor read noise enhances the sensor's SNR with 10.4 dB. Such sensors are very attractive for low light imaging applications which demand high SNR values.

DESIGN AND OPERATION PRINCIPLE:

Fig. 1 shows the simplified schematic diagram of the 4T pixel with a pinned-photodiode and the proposed column readout circuits, including a gain amplifier and a single slope A/D converter (SS-ADC). The use of the column gain amplifier can reduce the noise by amplifying the signal which will narrow the bandwidth due to the conservation product of gain and bandwidth, before the rest read noise is added. The gain here is defined by the capacitance ratio of C_{in}/C_{fb}, where C_{in} is the input capacitor, and C_{fb} is the feedback capacitor of column gain amplifier, respectively. The output of the column gain amplifier is connected to the column SS-ADC using an auto-zero capacitor C_{az}. The column SS-ADC consists of a comparator, driven by a ramp voltage and a bit-wise inversion (BWI) counter [1]. The BWI counter shows 32% reduction in power consumption and 2.4 times improvement in maximum speed over the conventional up/down counter [1]. After the ADC, the digital output of the sensor is ready to be readout. The column-parallel gain amplifier is implemented using a folded-cascode architecture at 3.3 V power supply. The specifications and simulated performance of the column-parallel gain amplifier are summarized in Table I.

Fig. 2 shows the readout timing diagram of the pixel and column readout chain. Initially, the floating diffusion (FD) node of the pixel is reset, and then the column gain amplifier and the comparator are reset sequentially as well. The pixel reset transistor (RT), the amplifier reset switch T_{op}, and the comparator reset switch T_{az} are closed sequentially. This sequential closing of the reset switches produces a "cascaded noise cancelling" process [2] which isolates the reset noise and offset noise of every previous stage by storing it in a subsequent capacitor and thus be cancelled by the analog correlated double sampling (CDS) later on [2], [3]. The digital CMS sequence is as follows. After the FD node is reset, the reset level is compared with the ramp voltage V_{ramp} and the BWI counter is set to synchronously count up. When V_{ramp} is equal to the reset level, the comparator output toggles from digital "high" to digital "low" and this stops the BWI counter from counting. The BWI counter value directly corresponds to the reset level in the column. For m-times sampling of the reset level, the reference ramp voltage V_{ramp} for the comparator will be up and down ramping for m-times while the BWI counter will count m-times up. The latched counter output thus corresponds to m-times sampling of the reset level available on the column. After the signal charge transferred to the FD node, V_C as the input voltage of the comparator goes up to the amplified signal level voltage accordingly.

During the signal charge transfer, every bit of the BWI counter is inverted to perform 1's complement operation by applying the control pulse B_1 and B_2. The BWI counter then is set to up counting for m-times again during pixel signal level sampling. Eventually the counters will digitally subtract the conversion of the sum of m-times sampling of reset signal from the sensor signal, and then do the averaging the output in digital domain. When m is 1, only the digital CDS is performed by the column readout chain. The advantage of this CMS technique is the high thermal noise suppression capability in readout chain circuits which can be reduced by a factor of √m, where m is the number of samples. According to [4-6], CMS technique is also useful in reducing the random telegraph signal (RTS) noise when large number of m is applied.

MEASUREMENT RESULTS

Fig. 3(a) & (b) show the measured differential nonlinearity (DNL) and integral nonlinearity (INL) plot of the column-parallel SS-ADC. The histogram test approach is used to measure the non-linearity of the SS-ADC. A 1.5 Hz sinusoidal wave signal is applied to the ADC after low-pass filtering. From the measured results, the worst DNL is within -0.8/+0.6 LSB and the worst INL is within -2.0/+4.0 LSB, which corresponds to a 0.58% nonlinearity. The non-linearity of the ADC is well below the nonlinearity of the pixel (pinned-photodiode and source follower) [7].

Fig. 4(a) & (b) show the dark random noise measurement results. It shows that the proposed column-parallel circuits with digital CMS technique is able to achieve 127 μV_{rms} input referred noise at the column amplifier gain of 12 with 16 times digital CMS in 10bit ADC mode. The significant reduction in the sensor read noise enhances the sensor's SNR with 10.4 dB. As a conclusion, such image sensors with the proposed column-parallel circuits are very attractive for low-light imaging applications which demand high SNR values.

CONCLUSIONS

A prototype CMOS image sensor with a new type of column readout chain is presented. The test sensor achieves a low noise performance by using the column-parallel gain amplifier together with a digital CMS algorithm. The measurement results show that the proposed column-parallel circuits achieve 0.58% nonlinearity. The dark random noise measurement results still show that the use of the proposed column-parallel circuit with digital CMS technique is able to achieve a drastically reduction of the random noise, i.e. nearly 70% reduction. This is an attractive benefit to use this proposed column-parallel circuit to enhance the SNR of imagers with 10.4 dB for low light imaging application.

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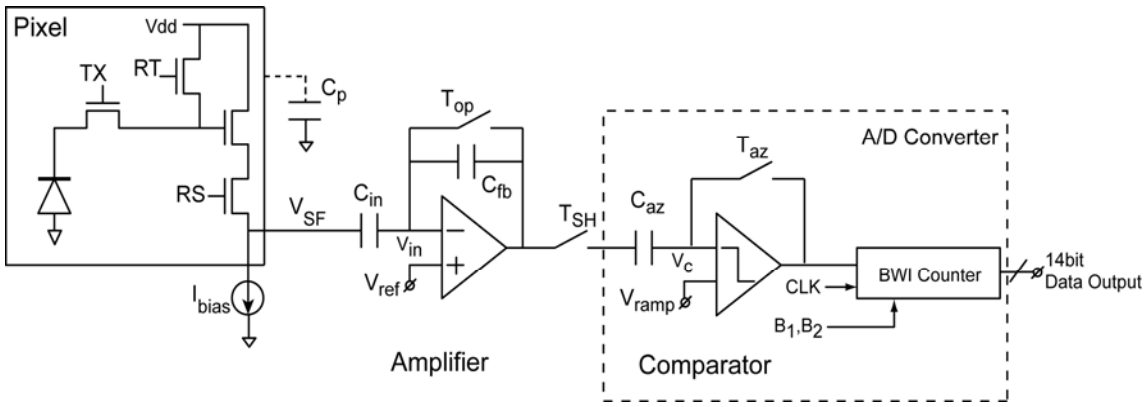


Fig.1 Schematic diagram of pixel and the proposed column readout circuits

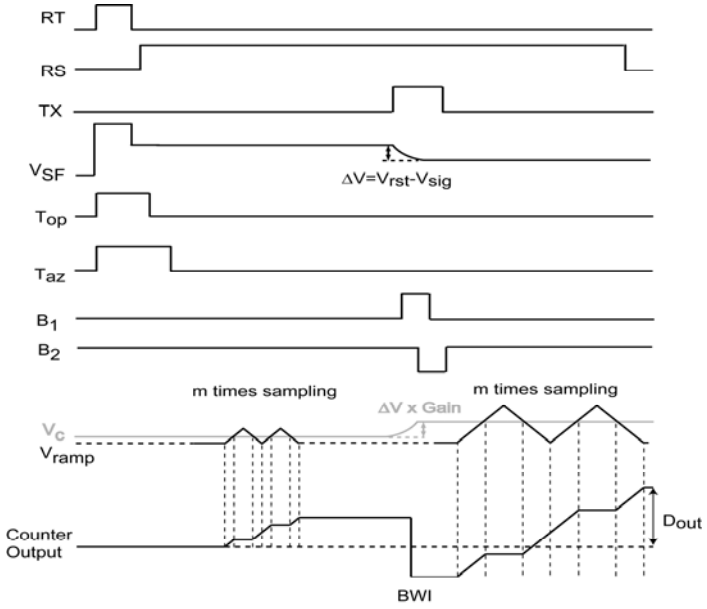
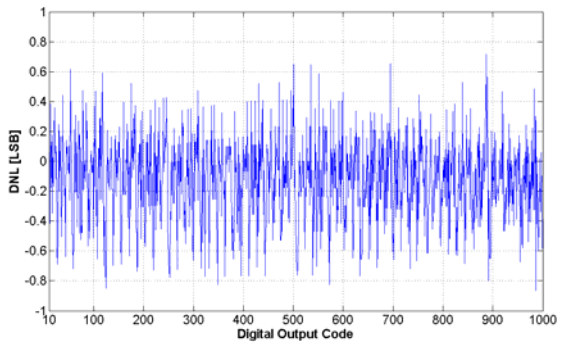


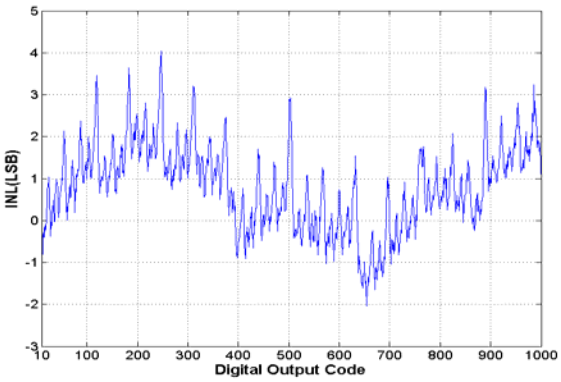
Fig.2 Readout timing diagram of the pixel and column readout chain

TABLE I
COLUMN-PARALLEL GAIN AMPLIFIER SPECIFICATIONS

Parameters	Value
Power Supply	3.3 V
Gain Stage	×2, ×4, ×8, ×12
Output Swing	1.35V
Open loop Gain	81.6 dB
-3dB Bandwidth	3 Hz ~ 11 MHz (Gain=12)
Phase margin	>62.68°
SNR	65~70 dB
Total Summarized Noise	129 μV_{rms} (Gain=1)
Power Dissipation	0.39 mW
Settling time	<160 ns
Slew rate	>25 V/μs

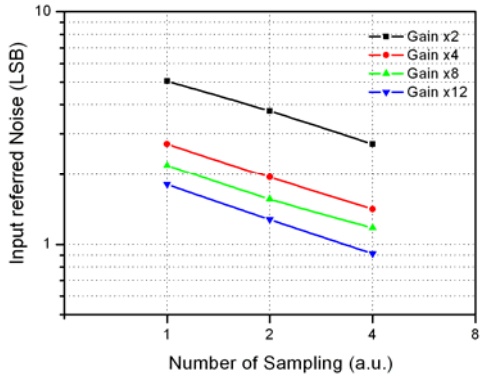


(a)

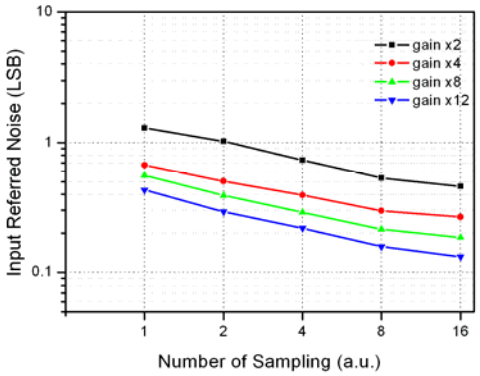


(b)

Fig.3 Measured column ADC nonlinearity: (a) DNL and (b) INL in 10b resolution mode



(a)



(b)

Fig. 4 Measured input referred dark random noise of the sensor in: (a) 12b, and (b) 10bit ADC resolution mode