Study of Image Artefacts caused by the single-ended CTA column comparator used in CMOS imagers

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The singled ended CTA architecture presented by [1], offers a simple, low noise, low power and compact comparator solution for CMOS imagers is shown in Fig1. Although this architecture is very well suited for small resolutions; it starts introducing image artefacts as resolution and conversion speed increase. This paper discusses these artefacts and some solutions implemented to extent the suitability of the single –ended architecture. The image artefacts considered are:

- Image dependant X-Droop,
- Smearing,
- Ground congestion pixel noise,
- Line noise.

Image dependant Droop:

When the image is flat, all the first stage inverters discharge the charge on their output, to ground. The ground plane at the centre of the array rises the most and the column comparators in that area fire later, leading to droop, as shown in Fig 2. If the ground plane resistance cannot be reduced, a pseudo-differential front-end architecture can be used to improve the rejection of the first stage to ground modulation (see Fig 3).

Smearing:

Smearing is one of the image artefacts, which causes a lot of problems once colorization and gamma correction is applied to the image (Fig 4). Smearing in single ended architectures has four main analogue origins:

- IR smearing,
- DAC smearing,
- Bias coupling smearing,
- Ground coupling smearing.

IR smearing is the simplest, as it is basically caused by a shift in the DC current consumption of the column comparator from auto zero to end of the conversion. It is therefore important to ensure that the current sources do not go linear, by using clamping structures (Fig 5).

DAC smearing is caused by the Miller effect of the first stage of the column comparator, which changes the load seen by the DAC and renders it dependant on the image content. A buffer behind the DAC can help extend the region of operation of the comparator, but only by so much as track resistances soon become an issue for larger arrays.

Bias coupling induced smearing is caused by the capacitance between the bias lines and the output of the inverters, as shown in Fig 7. This leads to the bias line becoming dependent on when the comparators fire. As the delay in the column comparator is directly linked to its bias current, this leads to the delay of one comparator being dependant on the state of its neighbours.

Ground coupling only really affects sensors when the speed of the DAC increases. As the output of the inverters increases, so does the amount of charge injected into the ground. These glitches, if they do not lead to x-droop, then potentially lead to smearing as they depend on the resistance from the column comparator to the pad. This is illustrated in Fig 8.

Ground congestion pixel noise:

The formula for the noise contribution of the CTA column comparator is $\sqrt{(comp\_noise^2 + dac\_noise^2 + quantisation\ noise^2)}$. Now in some cases the noise does not obey this formula and is higher. Often this problem is due again to ground plane congestion. The first pixel to fire actually prevents his neighbour from firing, making noise look bigger. A way to confirm this is to introduce droop in the image and see whether the noise decreases.

Line noise:

Line noise is critical in an image as it is so visible in an image sensor. Line noise caused by the column comparator can be subdivided into three categories: thermal line noise, supply rejection and finally substrate noise. Thermal line noise is random by nature and is usually caused by the bias transistors, which are common to all the comparators; and the bias currents provided to the column comparator. This is shown in Fig 9. One must take care in ensuring the noise caused by these bias elements leads to a line noise, which is kept well below 1 code. Supply rejection more often than not, has a beat to it and is caused by limitations of the power supply rejection of the column comparator. The only viable solution is a regulator for the column comparator. Finally substrate line noise is the

most difficult to eradicate as it is linked to digital activity or charge pump activity. Both influences can be minimised by careful layout. However keeping the digital current as constant as possible and image independent, helps a lot. Fig 10 describes the influence of digital current on line noise. By reducing the dark pedestal, we clipped the image to 0, this lead to a decrease in current if the image was near black and the line noise increased in the parts of the image above black.

[1] G.G. Storm et al, "Continuous time column parallel architecture for CMOS imagers", IISW 2007, June 2007, pp58

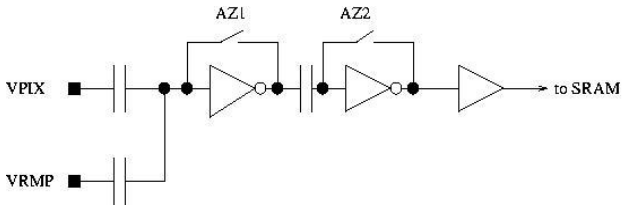

Fig 1: Single ended CTA system.

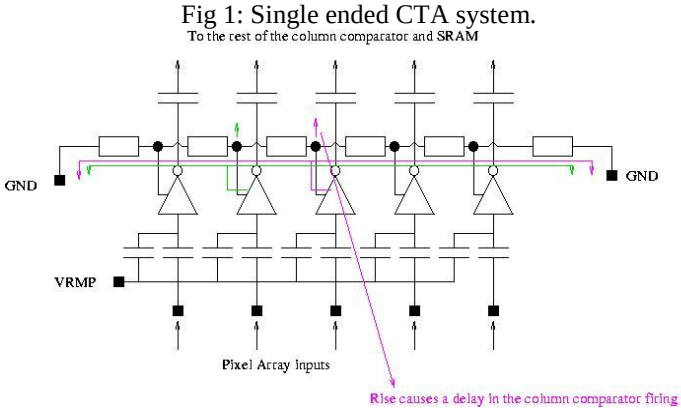

Fig 2: Mechanism for X-droop

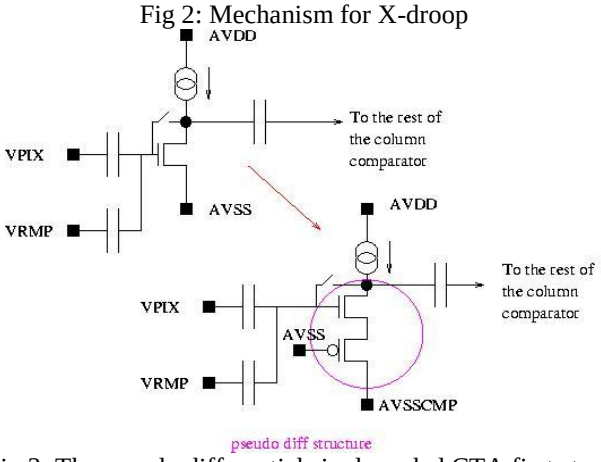

Fig 3: The pseudo differential single ended CTA first stage.

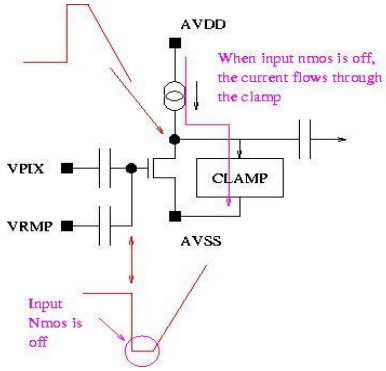

Fig 4: The Clamps

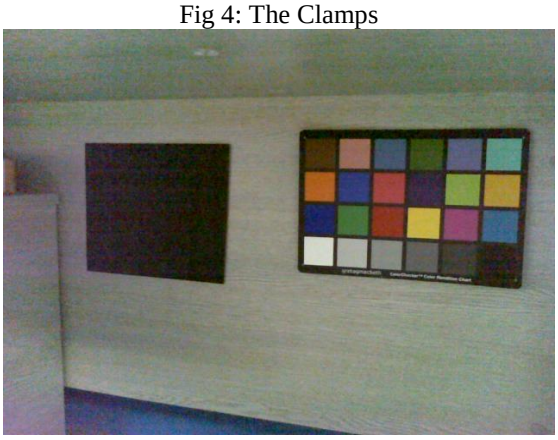

Fig 5: Smearing

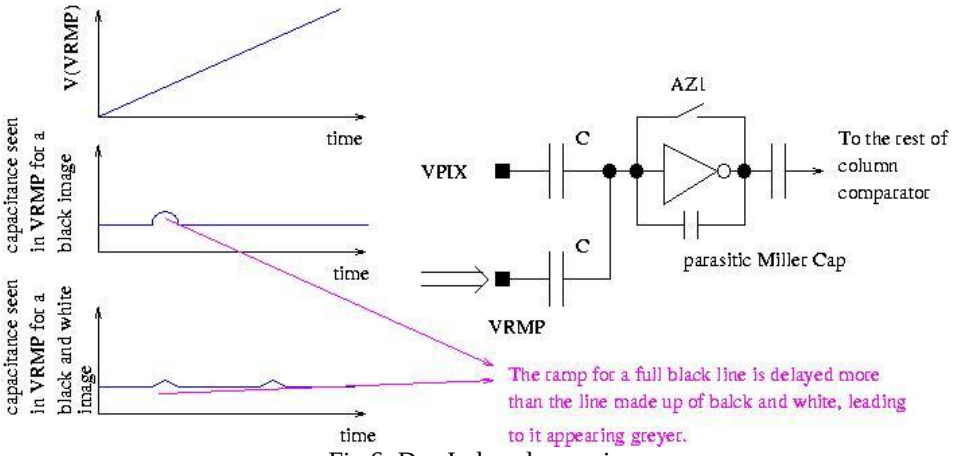

Fig 6: Dac Induced smearing

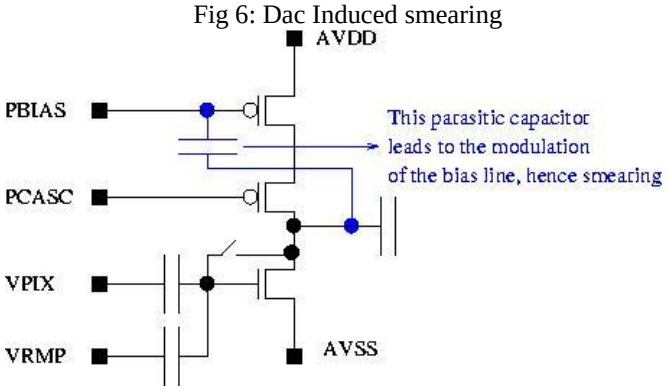

Fig 7: Bias line smearing

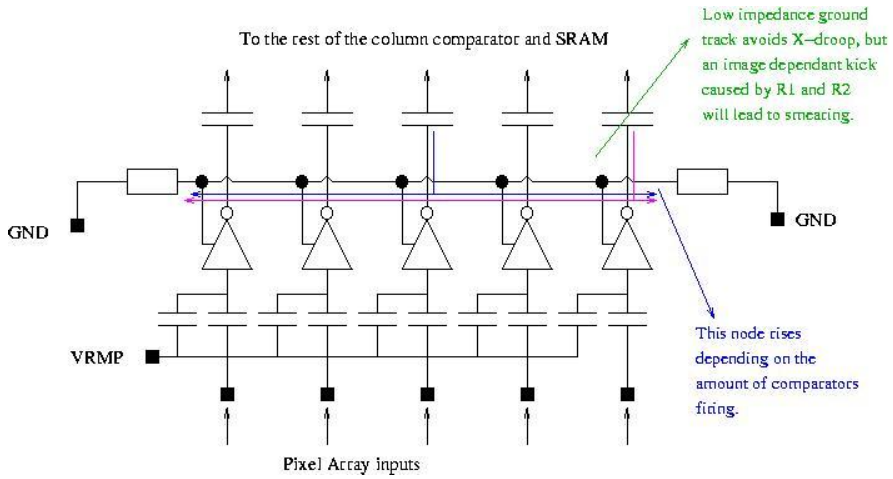

Fig 8: Ground induced smearing

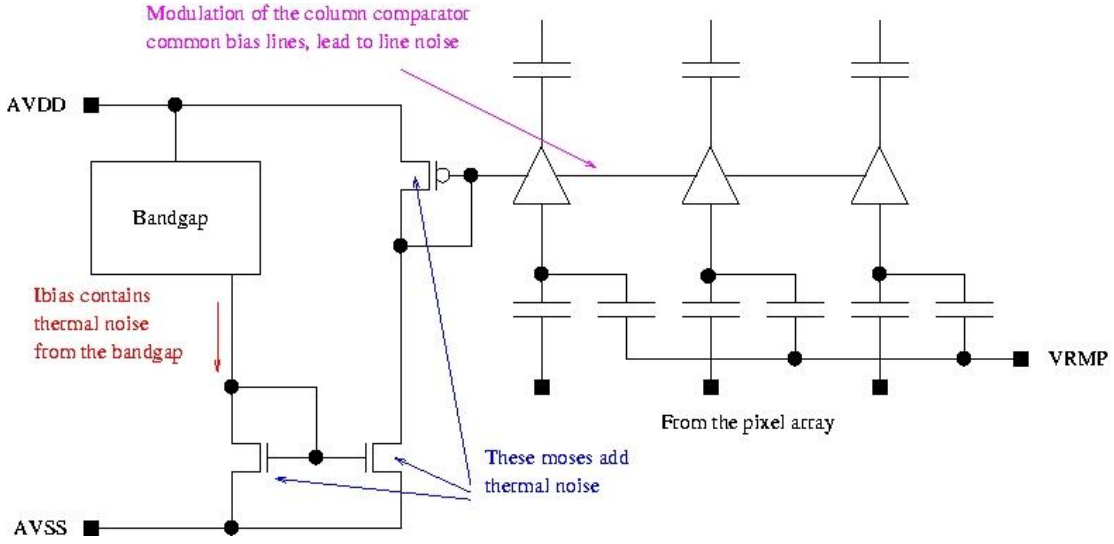

Fig 9: Thermal line noise due to the column comparator bias lines and currents

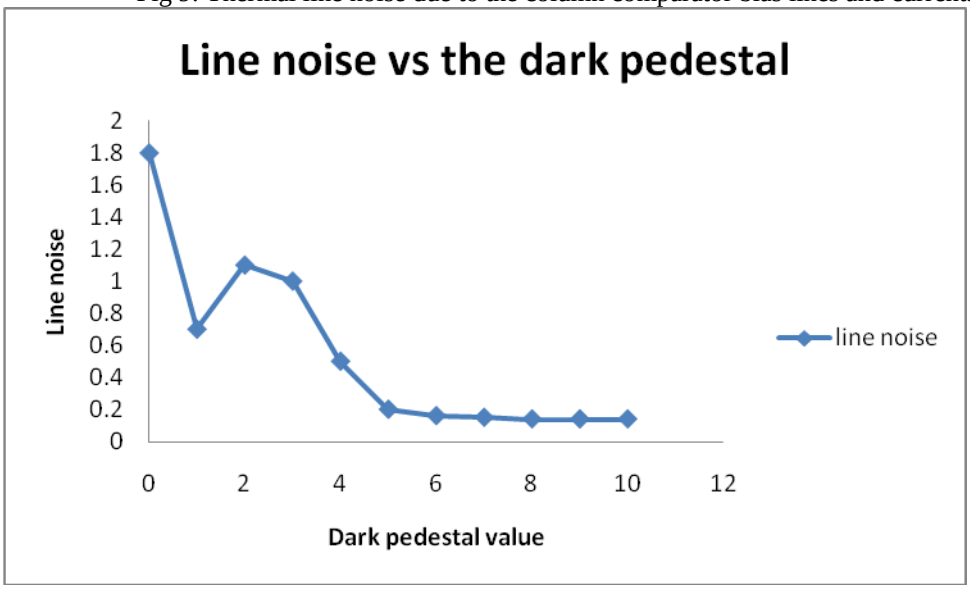

Fig 10: Influence of digital activity on line noise.
For low dark pedestal values, the image starts getting clipped, which leads to a decrease in digital current consumption, which in turn affects the unclipped pixels.