A High Speed CMOS Dual Line Scan Imager For Industrial Applications

P. Donegan, L. Korthout, M. Moser, V. Bommu, Y. Lin, A. Kumar, F. Feng, D. Marchesan, D.Verbugt, P. Albertini, W.de Haan, S. Xie, D. Atos, W. Maes, J. de Meulmeester, M. Sonder, E. Fox

Teledyne DALSA Inc.

605 McMurray Road, Waterloo, ON, Canada

Phone 519 886 6000, Fax 519 886 5767; e-mail paul.donegan@teledynedalsa.com

<u>Abstract</u>

This paper presents an ultra-high resolution, high speed linear image sensor for high speed industrial imaging. Two versions of the device have been fabricated and evaluated: a single line version with 16k pixels on a 3.5 um pixel pitch; and a high sensitivity dual line version with 8k pixels on a 7 um pixel pitch. Both devices are capable of a line rate of 70kHz. The CMOS imager design and evaluation results are presented.

Introduction

Machine vision applications continue to demand higher spatial resolutions and higher line rates in order to achieve both higher inspection precision and higher inspection throughput [1,2,3]. Smaller pixel pitches improve spatial resolution, but negatively impact line rate and sensitivity [4]. Sensitivity can be increased in linescan applications by increasing the number of pixel rows that are integrating signal. High speed can be addressed through a combination of high speed circuits and additional parallelism. When such approaches have been used in the past uniformity has often been impacted. Novel solutions have been used in the present work to achieve high speed and high resolution without sacrificing image uniformity.

Image Sensor Development

Figure 1 shows the block diagram for an individual design slice. Each slice contains 2k pixels in the 7 um implementation and 4k pixels in the 16k implementation. These slices are stitched lithographically at the wafer level to produce the final device.



The pixel was implemented using a modified 3T architecture with a partly pinned photodiode. The surface of the photosite is pinned via a shallow p-implant everywhere except the single metal contact to the reset drain and source follower gate [5]. Photocharge drains from the pinned region to the contact region during integration. Adjacent to each pixel is a dedicated source-follower readout circuit as illustrated in Figure 2. This architecture supports fully correlated double sampling (CDS) readout for suppression of photosite kTC noise and fixed pattern noise. Compared with a traditional 4T pixel, this 3T design also offers the advantages of a

higher voltage swing, no issues related to incomplete charge transfer, and negligible image lag when a hard reset is used. Compared with a pixel that uses a charge transimpedance amplifier (CTIA), this architecture operates at a lower power and can be realized with a more compact layout.

One of the major limitations of the pixel architecture is that integration and readout are inherently sequential operations. In order to allow for simultaneous integration and readout, and thereby maximize total light collection efficiency and scene throughput, the pixel output is directed to a serial readout chain by way of two banks of column-parallel sample and hold (S&H) circuits. When the pixel output is being sampled with one S&H cell, the other holds the output from the previous scan and is available for read out. The capacitors in the two banks are sufficiently large to eliminate mismatch between "even" and "odd" rows. The timing diagram is illustrated in Figure 2.



Figure 2. Pixel architecture and sample and hold circuits.

The sampled data from the column circuits are sequentially read from the column stages via a single unity gain buffer per column and a set of read rails. A shift register controls this serial read-out process (Figure 1). S&H stages in front of the CDS stage sample the reference level and the signal level from the read-rails. Successively the CDS stage performs the subtraction and the net video signal is applied to the succeeding 12-bit pipelined ADC (1.5bit/stage) for digitization to true 12 bit code. Four such serial processing chains are used per 2k pixels, each running at a 40 MHz data rate.

To minimize power dissipation and to reduce the number of pins, the data from the ADC is serialized at six times the ADC sampling frequency before transmission off chip via LVDS. Additionally, the line valid signal that is used for synchronization is eliminated by injecting a unique start of line sequence just prior to active video.

This highly parallel readout circuitry allows the sensor to achieve high line rates, however such architectures can be susceptible to image non-uniformities from mismatch between signal processing chains. External calibration for fixed pattern noise as well as offset and gain mismatch can be accomplished at the camera or image processing level using relatively simple algorithms as part of a factory or an initial in-field calibration. However these correction algorithms could fail if a change in environmental or operating conditions results in appreciable output drift of the sensor. At the same time, many line scan machine vision applications rely on continuous operation and cannot afford to perform repetitive calibration steps that interrupt the inspection process.

A circuit was implemented to facilitate dynamic auto-calibration of offset and gain across output channels. During the line blanking period, the serial portion of the analog processing chain is normally idle. At this time, the connection between the column circuits and the CDS stage can be interrupted, and in its place, two external DC signals can be fed into the serial processing chain to provide a measure of the offset and gain of the CDS and ADC circuits. Figure 3 shows a block diagram of the circuit implementation. To simulate a black pixel, the CDS circuit is clocked such that it samples the VREF rail twice; to simulate a white pixel, the CDS circuit alternatively samples the VSIG rail and the VREF rail to create a differenced output.



Figure 3 Black and White Reference circuit architecture for dynamic calibration of offset and gain mismatch.

By outputting black and white reference "pixels" that are independent of the scene, changes in the offset and gain that are related to the serial analog processing chain can be monitored by the camera and digitally corrected.

The implementation of black and white reference pixels relies on two DC reference inputs provided by the camera. It is critical that the DC references are directly sent to all taps without internal buffering in order to avoid tracking changes that are not part of the normal signal chain. This requirement dictates that the DC voltages supplied by the camera have a low output resistance in order to drive the high capacitive load on chip.

Evaluation Results

A sample image acquired from a rotating drum using the 8k version of the sensor is shown in Figure 4.

2	3	4	5	6	7	
С	d	е	f	g	h	

Figure 4 Sample unprocessed image taken from an 8K dual line scan sensor (in single line mode)

The evaluation results summary for the 8K and 16K sensors is listed in Table 1. All data was taken at a sensor operating temperature of 40°C and correspond to measurements in single line operation. At the system level, improvements to SNR can be achieved by summing the outputs of the two lines together in the camera. As expected, offset mismatch between channels is a significant contributor to overall FPN and reached as high as 214 DN on some devices (Figure 5). The offset mismatch is easily corrected in the camera without resulting a significant loss in dynamic range.

Sensor Performance Parameter	8K Measured Results	16K Measured Results
Resolution	8240 (H) x 2 (V)	16480 (H) x 1 (V)
Pixel size	7.04 μm x 7.04 μm	3.52 μm x 3.52 μm
Fill factor	100 %	100 %
Full Well capacity	30 ke	30 ke ⁻
Broadband Responsivity	$120 \text{ DN/(nJ/cm}^2)$	30 DN/(nJ/cm^2)
Conversion Gain	0.126 DN/e ⁻ per line	0.126 DN/e ⁻ per line
Fixed Pattern Noise per channel	< 40 DN	< 40 DN
Offset Mismatch between Channels	214 DN	195 DN
Photo Response Non-Uniformity	<10%	<10%
Noise floor	1.7 DN	1.77 DN
Dynamic Range	66 dB	66 dB
Non-linearity, 10 to 90% saturation signal	< 2 %	< 2 %
Maximum Line Rate	> 70kHz	> 70kHz

Fable 1	Overview	of sensor	performance



Figure 5 Dark line profile showing tap to tap mismatch.

The sensors were also tested across temperature and only minor changes to performance parameters were observed. The largest parameter deviation seen over an operating temperature range from 30°C to 60°C was the offset mismatch. As shown in Figure 6, the black reference circuit was found to track the average offset level of the channel very well across all channels and temperatures. This result should contribute well towards for a dynamic, scene independent correction for channel to channel mismatch in the camera.



Figure 6 Tracking of black reference circuit against the average output level of the scene in dark.

Conclusions

An 8K dual line scan and a 16K single line CMOS image sensor were developed for use in machine vision applications. Operation at greater than 70kHz is possible by the use of several read out channels operating in parallel. The design features low noise structures, real 12 bit conversion, and pixels optimized for high sensitivity. The architecture suffers from high channel to channel mismatch, but additional circuitry included in the sensor design can facilitate for correction in the camera.

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