P4 A 2/3-type 2.3-Mega Pixel IT-CCD for HD 1080p60

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Abstract

This paper describes our new development of 2/3-type 2.3-Mega pixel IT-CCD for HD 1080p60. In order to realize this frame rate, we adopt dual channel output system at horizontal CCD (HCCD). Therefore, we can drive at HCCD frequency of 74.25MHz as same as conventional. And we adopt four-phase drive HCCD. It is effective for high transfer efficiency and low power consumption.

1. Introduction

In a lot of countries, the broadcast stations have adopted High Definition TV (HDTV) system and it mainly includes two format, 1080i60 and 720p60. However, it depends on each country's system which format is adopted, 1080i60 or 720p60.

Therefore, in the professional broadcast camera market, there is a demand for 1080p60 format cameras of HDTV [1]. It is possible to convert 1080p60 into both 1080i60 and 720p60 without the image degradation.

By the way, image sensor is mainly divided into two types, a CCD image sensor (CCD) and a CMOS image sensor (CIS). The flagship cameras require global shutter of image sensor, which can avoid the image distortion or the flash band. On the other hand, they are caused by rolling shutter which is generally adopted in CIS. The image distortion is that a fast moving object appears to tilt. And the flash band is that a light band appears on the screen when a flash occurs such as that from a still camera or a strobe light. Now, there is a trade-off between keeping good pixel characteristics and adding global shutter function in CIS [2,3]. Therefore, CCD is suitable for the flagship cameras due to good pixel characteristics and global shutter function.

So, We have developed a new 2/3-type 2.3-Mega pixel IT-CCD for HD 1080p60. In order to realize 1080p60 frame rate which is doubled from 1080i60, we adopt dual channel output system at HCCD frequency of 74.25MHz.

2. Device structure

Figure 1 shows the schematic diagram of this device. The image area includes effective pixels which are arranged as 1952 (horizontal) × 1086 (vertical) and achieved a 16-to-9 aspect ratio. The pixel size is 5.0μm square. HCCD includes two channels in parallel. In order to realize high transfer efficiency from first HCCD to second HCCD, the transfer gate named HHT is arranged between first HCCD and second HCCD.

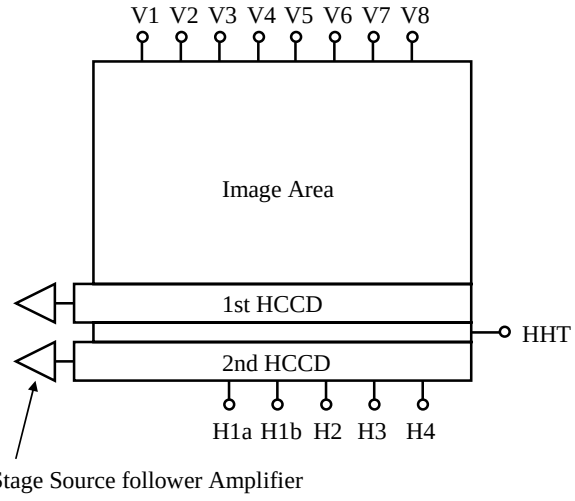

Figure 1. ***Schematic diagram of this device***

3. Four-phase drive horizontal CCD

In general, the HCCD gate electrode width is likely to become longer than HCCD gate electrode length and vertical CCD (VCCD) gate electrode length. Therefore, in case of dual channel HCCD, it is difficult to transfer from VCCD to second HCCD with high transfer efficiency due to its long distant charge path. For that reason, dual channel HCCD frequently has fixed pattern noise caused by transfer inefficiency between channels. In addition, dual channel output system tends to consume higher amounts of power because gate-to-gate and gate-to-substrate capacitances of HCCD become about twice. To solve these problems, we adopt four-phase drive HCCD in this new device.

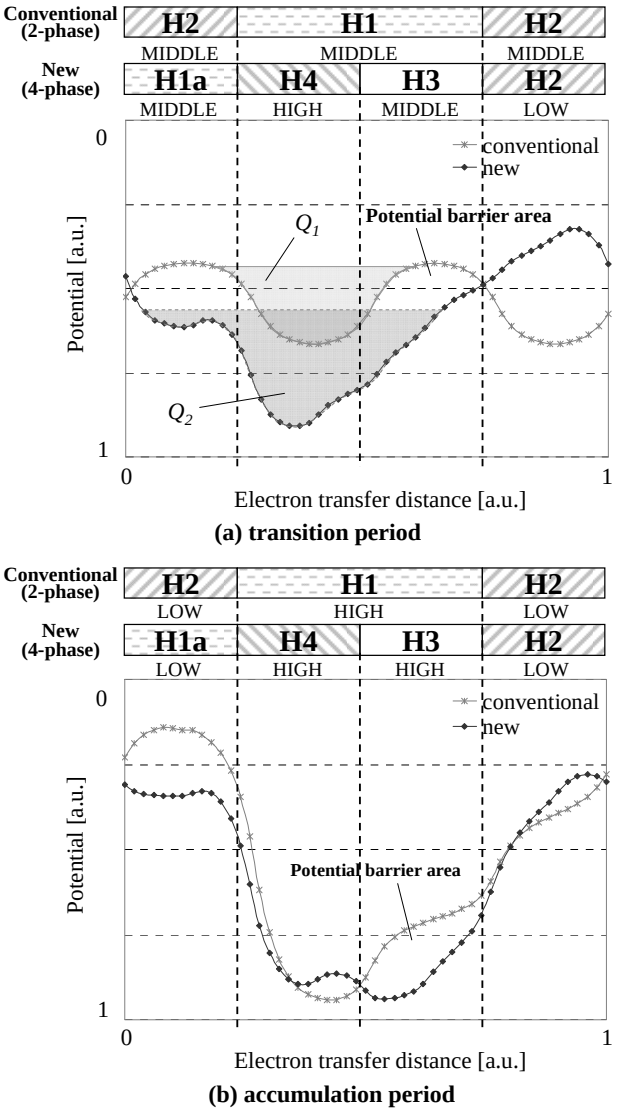

Figure 2. ***Simulation result of HCCD potential profile in a horizontal direction***

HIGH, MIDDLE and LOW mean 3V, 1.5V and 0V, respectively.

Figure 2 shows HCCD potential profile's comparison between this device's HCCD and conventional. One is at transition period and another is at accumulation period. As shown in figure 2, potential profile of four-phase drive HCCD at transition period is quite different from that of conventional HCCD even though they have similar potential profile at accumulation period. By comparison, the amount of accumulable charge at transition period is the smallest. Therefore, HCCD saturation signal depends on this transition period. In conventional two-phase drive HCCD, every gate must have potential barrier area to prevent signal back-streaming. Due to this potential barrier area, the amount of accumulable charge is small. On the other hand, in four-phase drive HCCD, every gate doesn't have to have anti-back-streaming potential barrier area by the difference of driving sequence. Therefore, saturation signal per unit area in four-phase drive HCCD (Q_2) becomes more than twice as much as conventional in two-phase drive HCCD (Q_1).

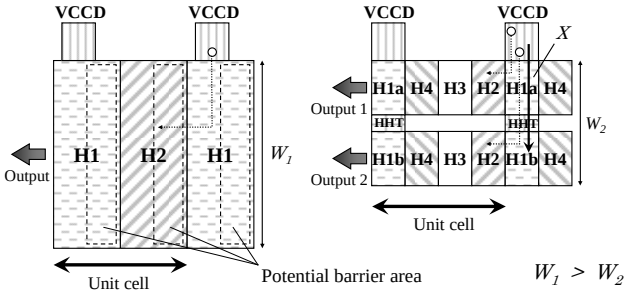

Figure 3. ***HCCD gate electrode configuration***

Figure 3 shows the gate electrode configuration. In this new device, we arrange six kinds of gate electrodes in HCCD which are named H1a, H1b, H2, H3, H4 and HHT for dual channel and four-phase drive HCCD. H1a is arranged in first HCCD and H1b is arranged in second HCCD. H2, H3 and H4 are arranged in both channels. HHT is arranged between channels. In case of horizontal direction transfer, H1a and H1b are driven by same phase pulse. Due to the four-phase drive HCCD, we can design HCCD gate electrode width of new CCD (W_2) to about thirty percent narrower than that of the conventional CCD (W_1), holding same HCCD saturation signal of unit

cell, even though the length W_2 includes dual channel. In addition, this narrow HCCD gate electrode width is effective for reducing power consumption because we can reduce gate-to-gate and gate-to-substrate capacitances of HCCD.

4. Transfer between channels

Figure 4 shows simulation result of HCCD potential profile in a vertical direction. This profile is along the electron path *X* in figure 3(b). In case of vertical direction transfer at HCCD, H1a and H1b are driven by different phase pulse for easy transfer between channels. For smooth transfer, the channel potential of second HCCD is deeper than HHT and HHT is deeper than first HCCD at each "high" state. Condition (i) is when H1a, HHT and H1b are high voltage level and last VCCD is low voltage level. In this period, signal charges are quickly transferred from last VCCD to H1a by the fringe electric field in the area *A* and drift to H1b by built-in electric field. Condition (ii) is when H1a is changed into low voltage level. In this period, signal charges transfer from H1a to H1b by the fringe electric field in the area *B*. Condition (iii) is when HHT is also changed into low voltage level for the separation between H1a and H1b. In this period, the signal charges which could not be transferred at the position such as gate interface by a potential dip or a potential barrier are completely transferred to H1b. In the area *C*, there is less affected by the fringe electric field *A* and *B* because this area is far from the gate interface. Therefore, when the first HCCD becomes wider, electric field in the area *C* gets smaller.

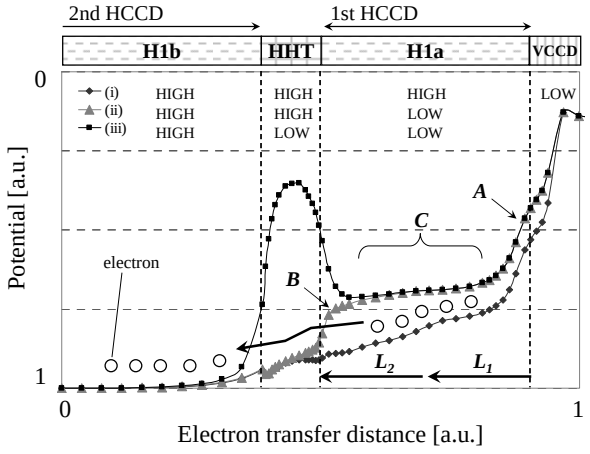

Figure 4. ***Simulation result of HCCD potential profile in a vertical direction***

At HCCD, HIGH and LOW mean 3V and 0V, respectively.

Figure 5 shows transfer time dependence from VCCD to H1b. This transfer time includes two steps corresponding to L_1 and L_2 (shown in figure 4). First step is the time when the voltage level of each gate is condition (i) and the electron path is from the interface between VCCD and H1a to the center of H1a. Second step is the time when the voltage level of each gate is condition (ii) and the electron path is from the center of H1a width to the interface between H1a and HHT.

In case of narrow HCCD width, the transfer time is very short due to the fringe electric field by the last VCCD gate and HHT. On the other hand, in case of wide HCCD width, the transfer time becomes much longer because the area *C* which has almost ten times smaller electric field than the area *A* and *B* is increased. That is disadvantage to prevent from fixed pattern noise peculiar to dual channel HCCD.

Therefore, we had better choose the first HCCD gate electrode width as narrow as possible. However, if first HCCD gate width is too narrow, H1a gate has less saturation signal. There is a trade-off between high vertical transfer efficiency and saturation signal in H1a. In this new device, by several-step impurity implantations under H1a gate, we could achieve enough saturation signal at H1a, keeping high transfer efficiency in both vertical and horizontal direction.

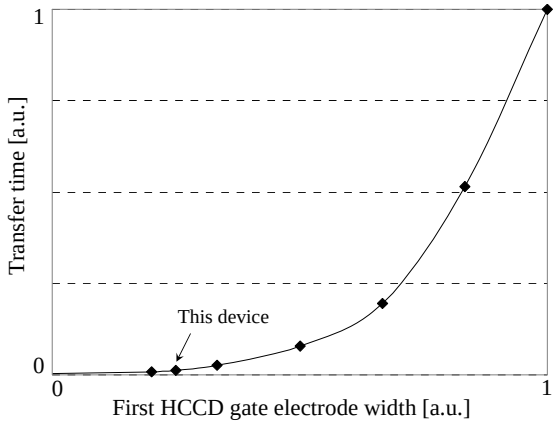

Figure 5. ***Transfer time dependence of first HCCD gate electrode width***

5. Fabrication

We apply newly developed process to fabricate this device. Sensitivity and smear level are improved by photodiode and micro lens optimization. Figure 6 shows the chip image of this device.

Figure 6. ***Chip image of this device***

6. Device characteristics

Table 1 and table 2 summarize the characteristics of this device and HCCD, respectively. By adopting four-phase drive HCCD structure, HCCD drive voltage is 3.0V as same as conventional. And also power consumption at 1080p60 isn't increased from conventional at 1080i60. Sensitivity and smear level are improved to 165mV and -130dB, respectively. It is possible to output 1080i60 signal chain using one channel output as same as conventional.

And it is possible to get not only 1080p60 but also 1080i120 signal at HCCD driving frequency of 74.25MHz. Furthermore, it is possible to get 1080p90 or 1080i180 signal for slow-motion recording at HCCD driving frequency of 111.375MHz. On the contrary, it is possible to get 1080i60 signal at HCCD driving frequency of 37.125MHz which is half of 74.25HMz.

7. Conclusion

A new 2/3-type 2.3-Mega pixel IT-CCD for HD 1080p60 has been developed by dual channel and four-phase drive HCCD. This device has not only high frame rate but also high sensitivity, low smear, large saturation signal. Therefore, it is suited for broadcast and cinema camera use.

8. Acknowledgement

The authors would like to thank the members of Image Sensor Business Unit for their support and valuable discussions.

9. References

[1] P. Centen et. al, "A 2/3-inch Low Noise HDTV FT CCD-Imager for 1080i180, 1080p90 and 720p120 Scanning at Constant Image Diagonal", IEEE 2009 International Image Sensor Workshop, June 2009.

[2] I. Takayanagi et. al, "A 600×600 Pixel, 500 fps CMOS Image Sensor with a 4.4mm Pinned Photodiode 5-Transistor Global Shutter Pixel", IEEE 2007 International Image Sensor Workshop, June 2007.

[3] S. Lauxtermann et. al, "Comparison of Global Shutter Pixels for CMOS Image Sensors", IEEE 2009 International Image Sensor Workshop, June 2009.

Table 1. ***Device Characteristics***

Optical format	2/3-type
Effective pixels	1952(H) × 1086(V)
Pixels size	5.0(H) × 5.0(V)μm
Color filter	Black and white
HCCD driving frequency	74.25MHz
HCCD driving voltage	3.0V
Sensitivity (1080p60) *	165mV
Saturation signal (1080p60)	910mV
Smear (V/10)	-130dB

** face plate illumination : 1.9lx*

Table 2. ***HCCD Characteristics***

	Conventional	**New**
Format	1080i60	1080p60
Channel number	Single	Dual
Driving frequency	74.25MHz	74.25MHz
Driving clock	2 phase	4 phase
Driving voltage	3.0V	3.0V