IISW-2009

BSI – technical challenges

Bergen. 25th June 2009

Outline

- BSI consumer vs BSI scientific
- BSI vs FSI
- Remaining challenges
  - Charges collection
  - BSI overlay challenges
  - BSI laser annealing
  - Thinning Process
- Starting material competition

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BSI consumer vs BSI scientific

- Consumer
  - Small pixel
    - AR<< 1, V shape
  - Colored Pixels
  - High Manuf. volume
  - Low cost
- Scientific
  - Large pixel
    - AR >> 1, H shape
  - Black & White Pixels
  - Low Manuf. volume
  - Not cost effective for consumer

BSI concept has been reused :

same motivation, driven by sensitivity improvement [1], but technical & production challenges are very different for consumer and scientific BSI sensors

FSI consumer vs BSI Consumer

- **FSI for Consumer : 1.4 µm Pixel**
  - ❖ **state of the art =>**
  - **Blue, Green & Red QE 50 to 55 %**
  - **Low Xtalk < 5 %**
    - ➔ **100 _ 130 Lux @ SNR10**
  - **Depletion zone & photons entrance :**
    - ➔ **Same side**
      - **Favorable for Electrical xtalk**

- **BSI for Consumer :**
  - ❖ **how to be ahead of FSI =>**
  - **RGB QE > 65 %**
  - **BSI Xtalk < FSI Xtalk < 5 %**
    - ➔ **better SNR**
  - **Depletion zone & photons entrance :**
    - ➔ **Opposite side**
      - **Not favorable for xtalk**

Lower Xtalk - Better QE with no added dark current or noise sources

➔**dedicated Back side diode optimization is mandatory**

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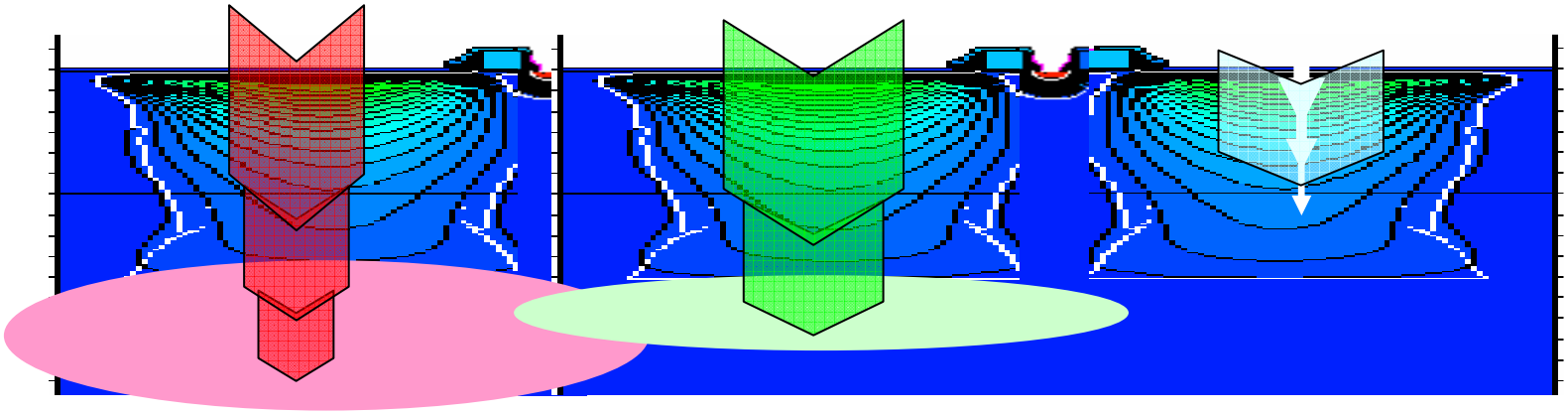
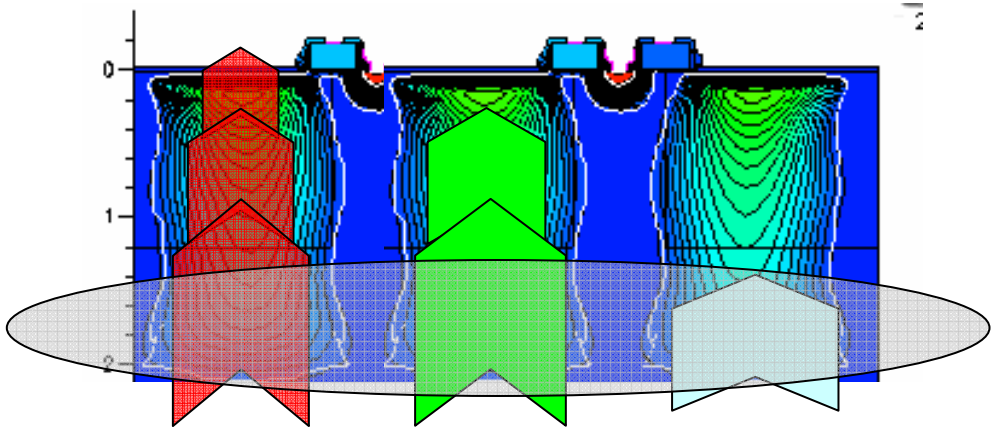
FSI pixels working schematic



No xtalk from diffusion for the Blue
Low level of xtalk for the Green
Medium level of xtalk for the Red

Even if we have low level of signal ➔ The poor collection on the rear side of the photodiode ➔ color xtalk which is already a concern for FSI …

Back side illumination + Smaller pixel



High level of photon absorption for the three colors on the rear side of the diode

➔ collection efficiency must be managed as first priority

- **High energy implant (800 keV, 1 MeV , even more) [2][3] with high resolution for space & width for thick photo resist**
- **Deep Trench [4] : Idark concern [5]**
- **Back side Graded Doping profile with built in Electrical field**
  - ✓ **what about laser anneal compatibility ?**
- **Microlens to concentrate light in the centre of the pixel [6]**

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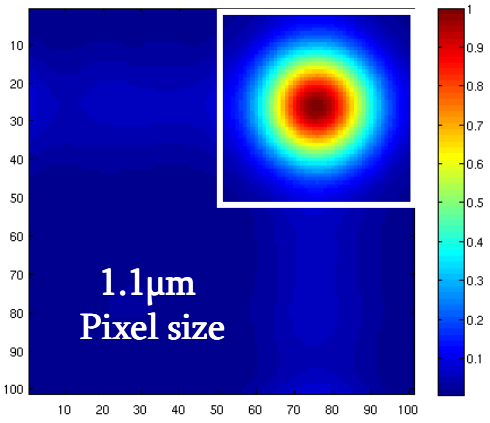
BSI overlay challenges

- Alignment Mark recognition
  - Mark created on front Side
    - Should be visible and right positioning through back side layer
- Comparable State of the Art
  - 3D interconnect, 3D wafer to wafer stacking [7]-[8]
    - Misalignment ranging from, best case : 0.6 to 2 µm
    - $E_{tot} = E_{wafer\text{-}wafer\text{-}misalignment} + E_{wafer\text{-}Deformation}$
- BSI overlay issue = Wafer deformation

BSI overlay requirements

- Overlay request for Pad
  - 100 * 100 µm²
    - 1 to 3 µm misalignment could be acceptable
- Overlay request for Colored filters
  - 1.4 * 1.4 µm² Bayer Pattern and below
    - Precise alignment is mandatory and should be better than 0.1 µm

Filters+ulens centered

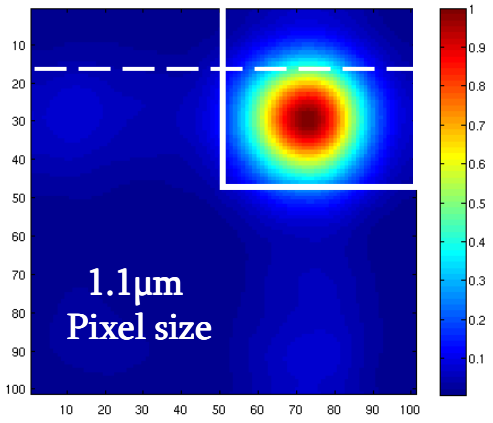


100nm

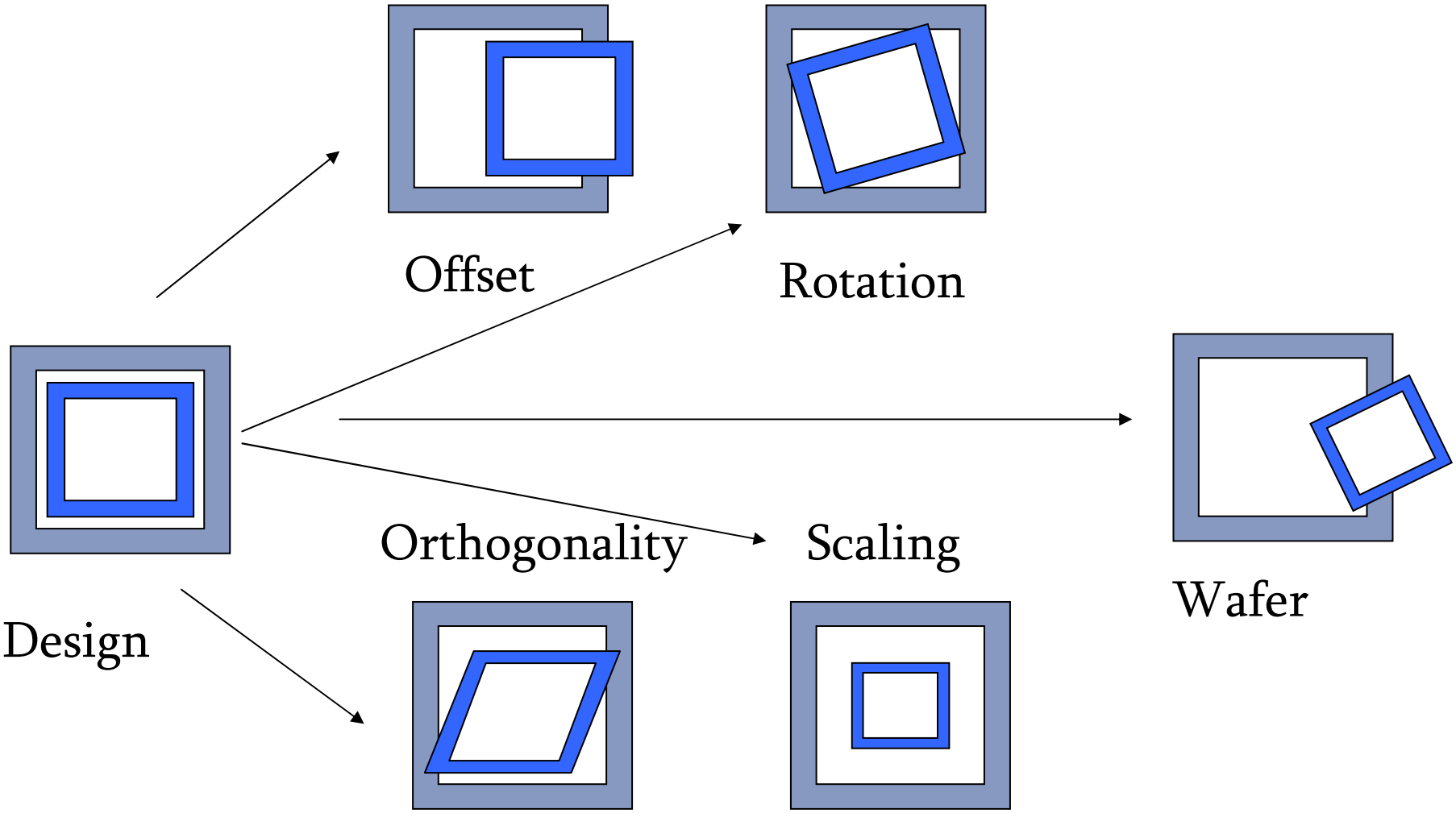
100nm

Spot size close to Pixel size

Filters+ulens shifted

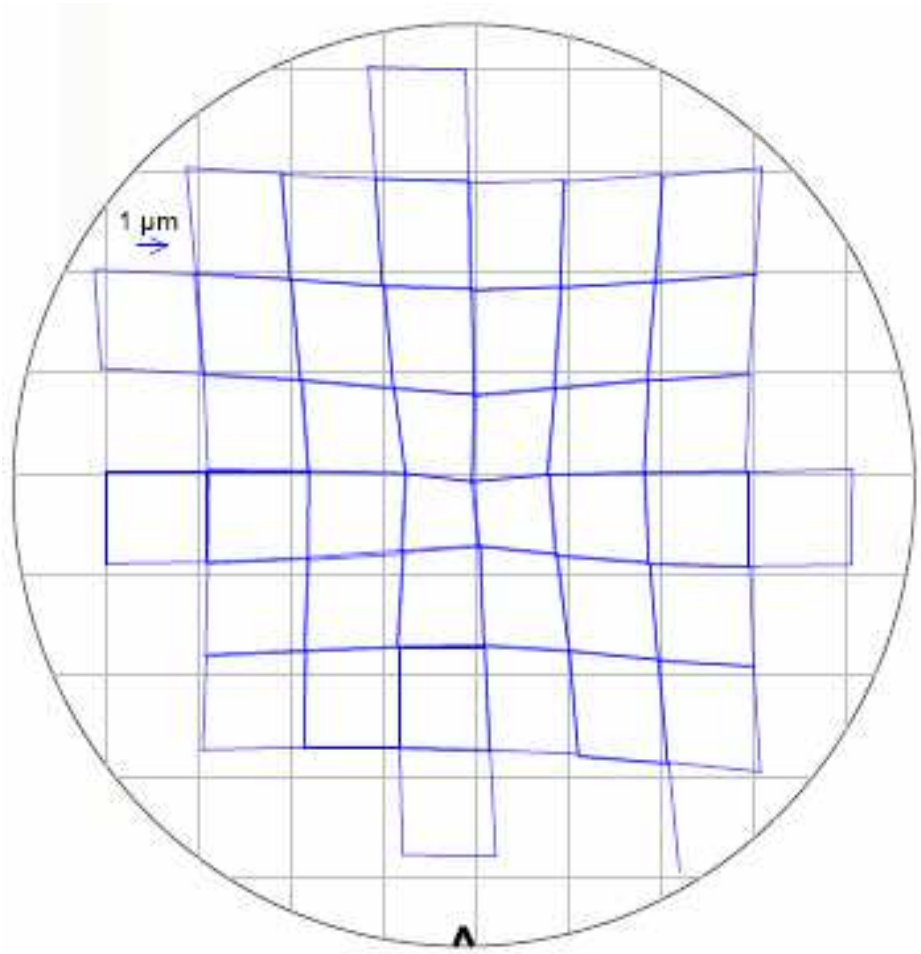


Root causes for alignment mark issue



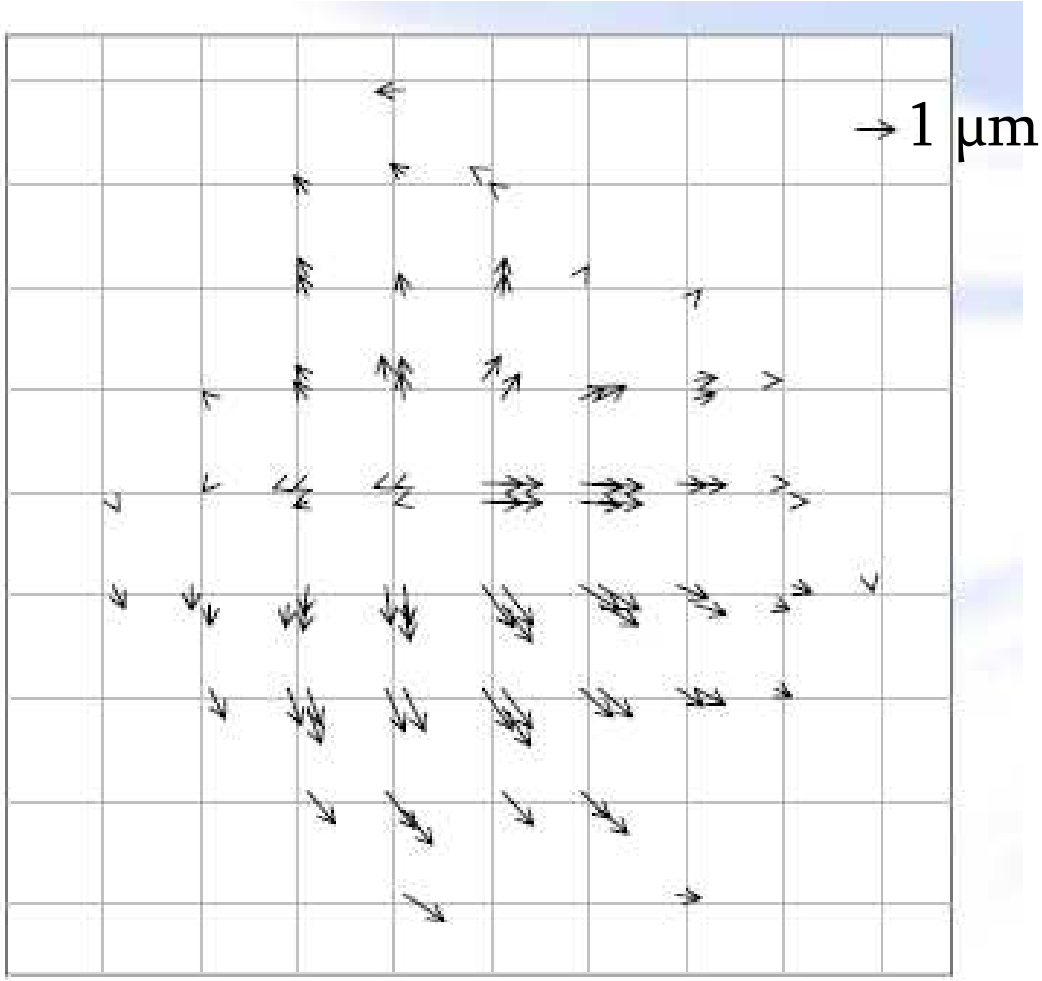
“Box in Box alignment control mark”

Wafer mapping result illustration



Wafer deformation should be 10 times better than 3D wafer to wafer bonding state of the art

Wafer mapping result illustration



Wafer deformation should be 10 times better than 3D wafer to wafer bonding state of the art

Backside to front side Alignment achievements

- Bonding Process :
  - Bond process control ➔ T°c
  - bonding interface preparation ➔ Bonding energy
  - mechanical constraints relaxation ➔ material choice
  - wafer curvature tuning ➔ mechanical stress management
- Thinning process :
  - mechanical (hard) & chemical (soft) process tuning
    ➔ mechanical stress management
- Alignment process :
  - Residual misalignment correction by photolithographic algorithm

3MPiX – 1.4 µm Pitch – Bayer pattern

2 µm deep depletion diode

Color alignment Below 50 nm

SOI starting Si
No Laser anneal

Courtesy of D.Herault ST

See [3] for electro optical characterization

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Laser annealing challenges

- Doping Activation process & implant defect curing

- High temperature gradient management
  - High temperature on back-side > 800℃ (Melting @145 0℃ under investigation)
  - Low temperature (< 400℃) at 4 µm far from anneal ing or melting zone (active Device integrity , interconnect temperature integrity in place before annealing process

- Photo response with good uniformity
  - No moiré pattern coming from scanning or overlapping beam
  - No PRNU due to beam energy non uniformity

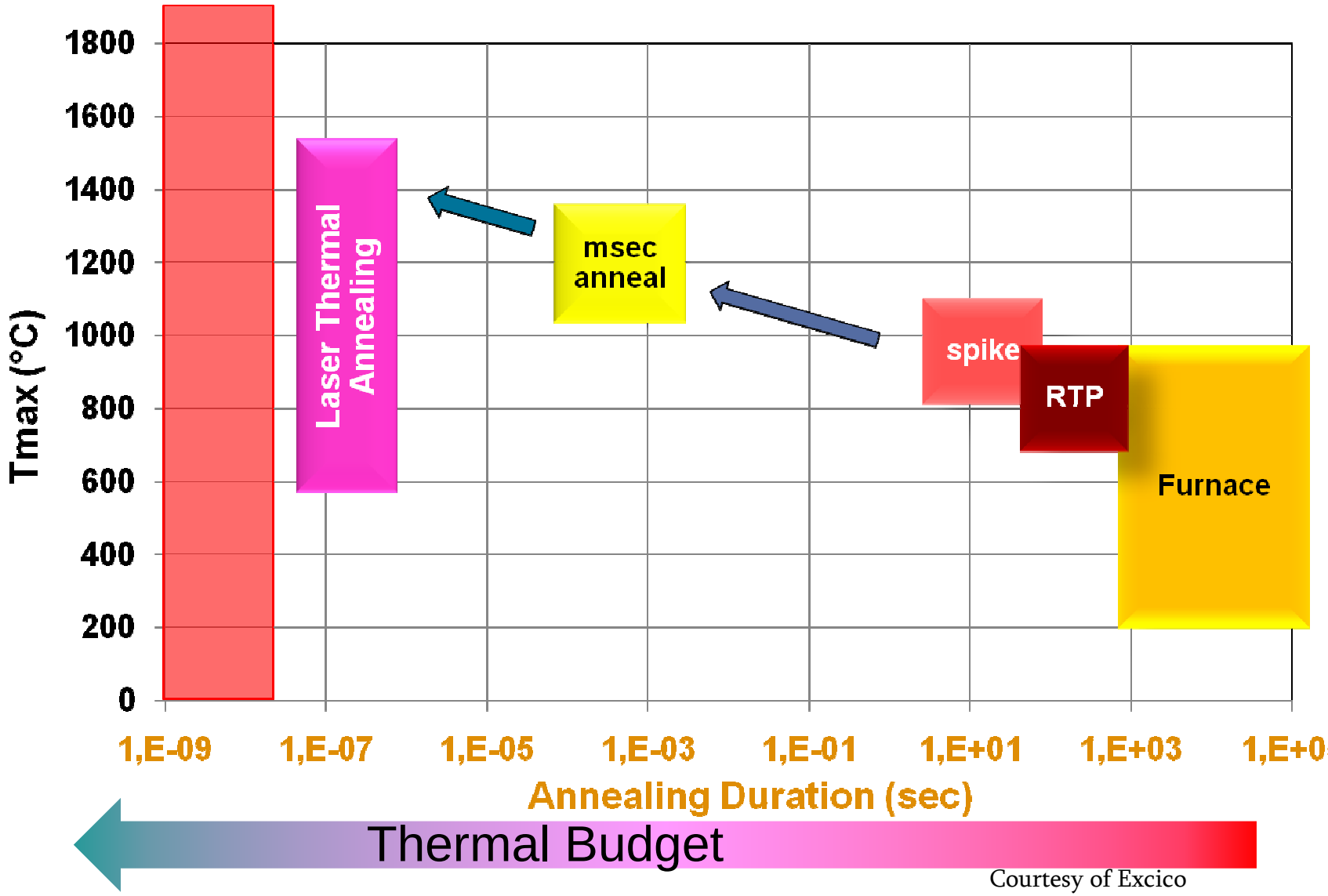
Doping activation road-map

- Know-how
  - Furnace : basic process, starting micro-electronic
  - RTP : introduced and driven by advanced CMOS
  - Spike : introduced and driven by advanced CMOS
  - Laser msec (IR) : introduced and driven by advanced CMOS

- objectives
  - Ultra low thermal budget
    - **UV excimer laser , nano sec pulse, liquid phase – Si melting phase [9]**
    - **imaging process ahead than the utmost advanced CMOS ?**
      - **No CMOS process leverage**

✓ Not yet well introduced Digital and for the time being driven by Imaging, LCD, Power Devices ?

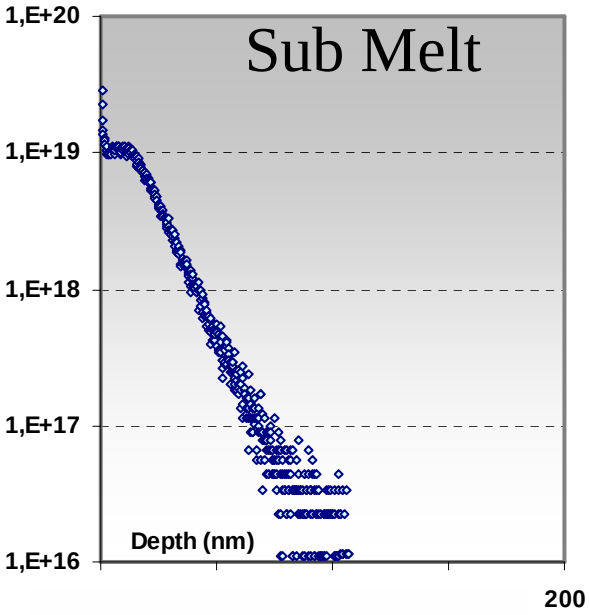
Hot Process for Semiconductor Doping activation



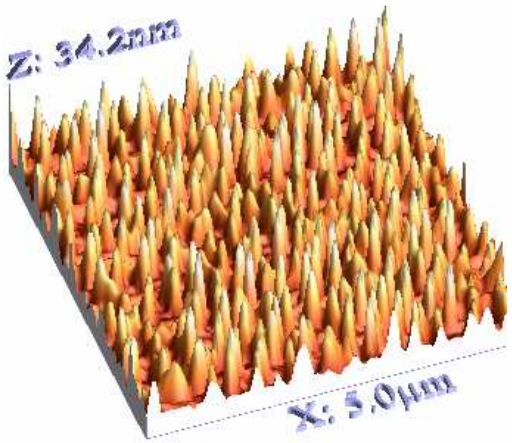
Courtesy of Excico

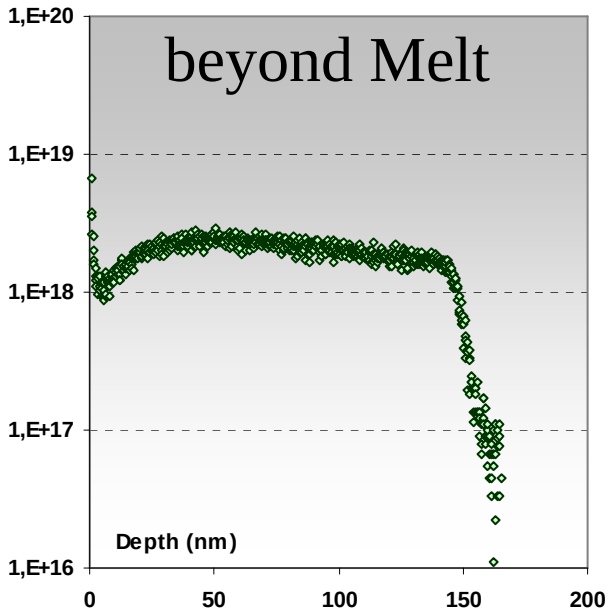
Requirement for Laser annealing

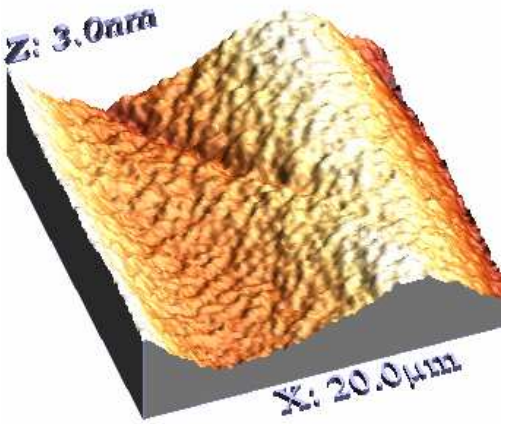
- Ultra low thermal budget
  - Excimer sub µsec pulse UV laser
- One Die – One shot
  - Full die exposure in one laser shot without overlap
    - No moiré pattern
- Single pulse or multi pulse
  - Sub-melt or beyond melt choice
- Ultra shallow junction
  - 7nm to 20 nm
- Manufacturing performances
  - Throughput (step and repeat), repeatability, reliability



@ threshold
Melting Point





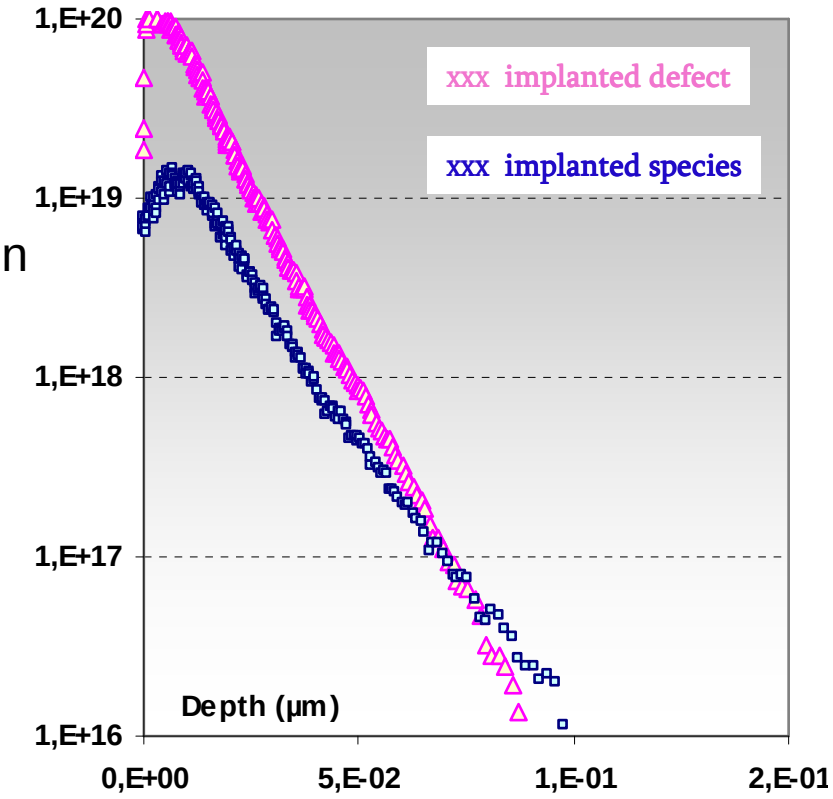


Sub Melt

beyond Melt

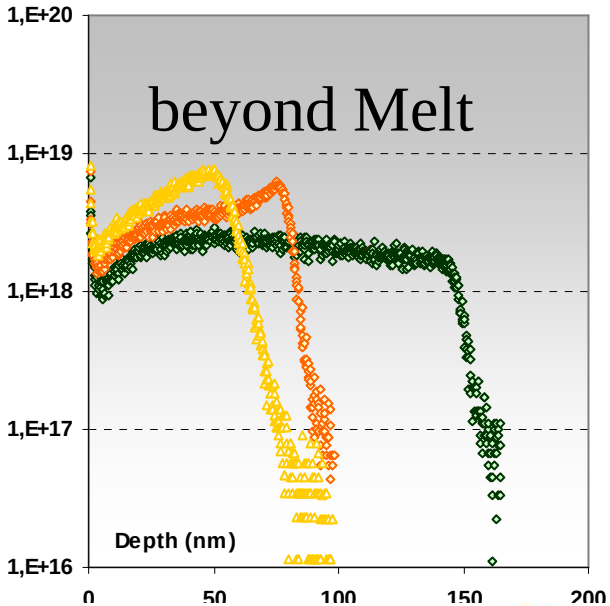
Sub Melt laser annealing

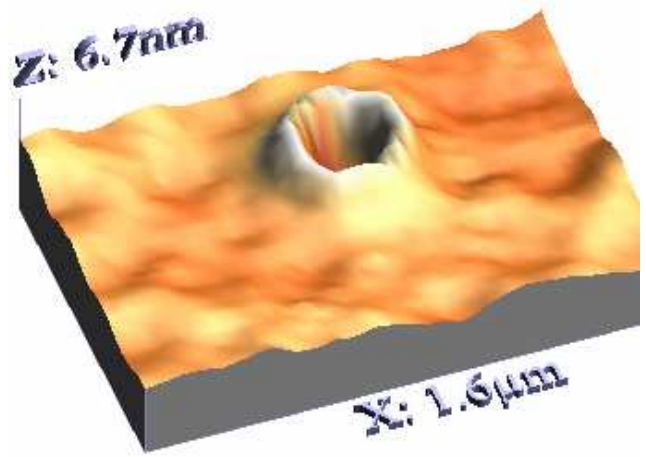
- Why sub-melt choice
  - Ultra thin Doping layer
  - Doping layer as implanted layer
    - Solid phase with no doping redistribution
  - Built-in electrical field
    - Better charge collection
    - Cross talk reduction
    - QE improvement
- Remaining challenges
  - Implantation defect curing efficiency
    - How to achieve Best in class dark current and white pixel count



Beyond Melt laser annealing

- Why beyond melt choice
  - High throughput step & repeat process
  - 100% Doping activation
    - Liquid phase with dose redistribution
  - Implantation defect cure efficiency
- Remaining challenges
  - Surface Particles induced Silicon layer defect during melting phase
  - Laser beam uniformity is critical
    - Melting layer thickness uniformity impact on PRNU





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Bulk starting material

Selective Wet etch on P+ Etch Stop Layer

- the challenge is to find the process window to manage properly
  - Precise Final layer thickness and uniformity
    - QE & cross talk optimization depend on layer thickness
  - Defect in the remaining Si bulk material
  - Defect at the surface of thinning layer

➔ P+ etch stop layer doping profile optimization [1]

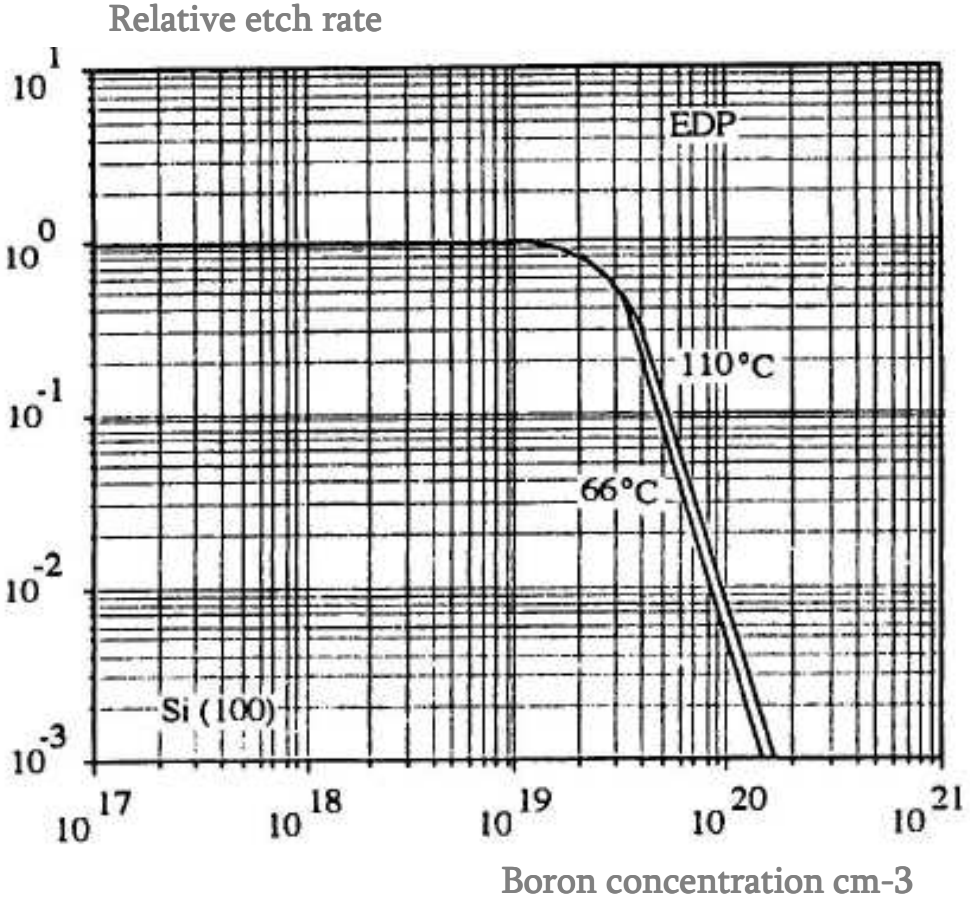
➔ chemistry recipe (KOH, TMAH, NDP, dilution, T°c, duration) [11]

Bulk starting material

Selective Wet etch on P+ Etch Stop Layer

- High Selectivity needed **[1] [10]**
  - Why
    - Layer thickness control
    - Surface non uniformity

    and defect removal thanks to over etch
  - How
    - P+ layer concentration at high level (# 1^E19 to # 1^E20 At/cm3)
  - Challenges
    - Avoid doping diffusion during CMOS process
    - Corse & fine grinding process step uniformity
    - P+ doping etch stop layer
    - Chemistry for thinning process

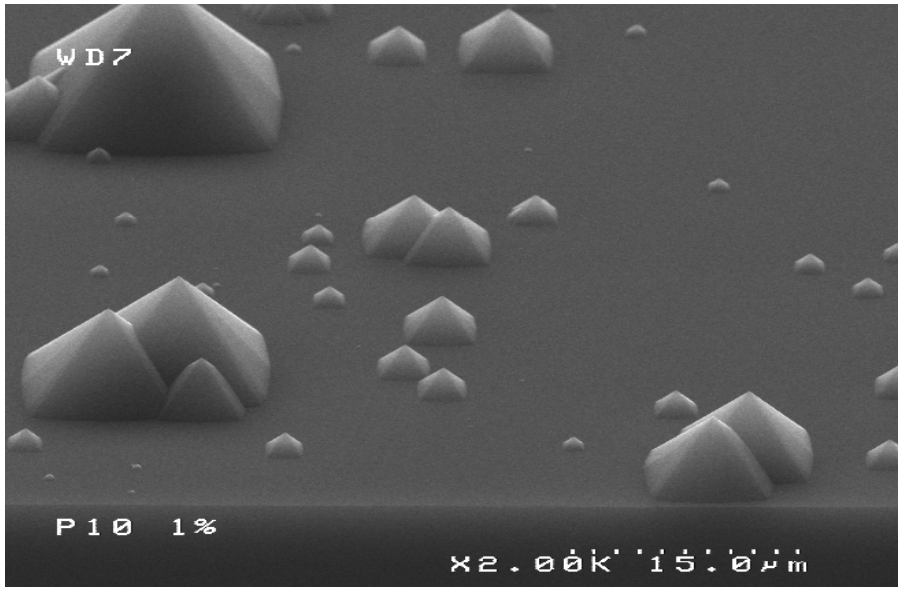


[10] Q.-Y. Tong & U. Gosele, Semiconductor Wafer Bonding

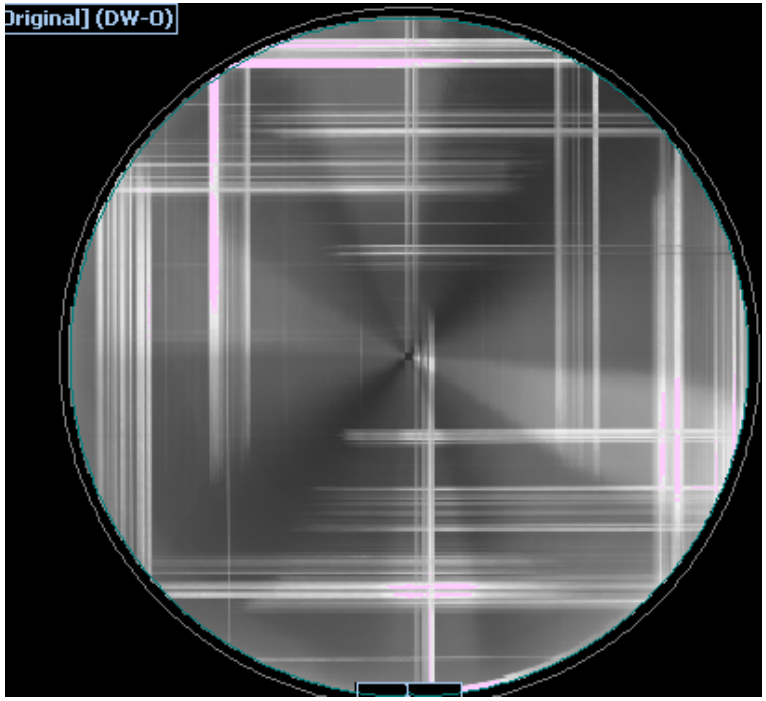
Bulk starting material

Selective Wet etch on P+ Etch Stop Layer

- low doping level
  - <111> Pyramid on the surface
- High doping level
  - Slip line in the Epi layer



Tradeoff has to be found



Courtesy of P.Besson ST, CEA

SOI Starting Material

Selective Wet etch on oxide layer

- Intrinsic High Selectivity for Si on SiO2
- Layer uniformity control by Epi process
- Back side BOX can be removed or kept if needed

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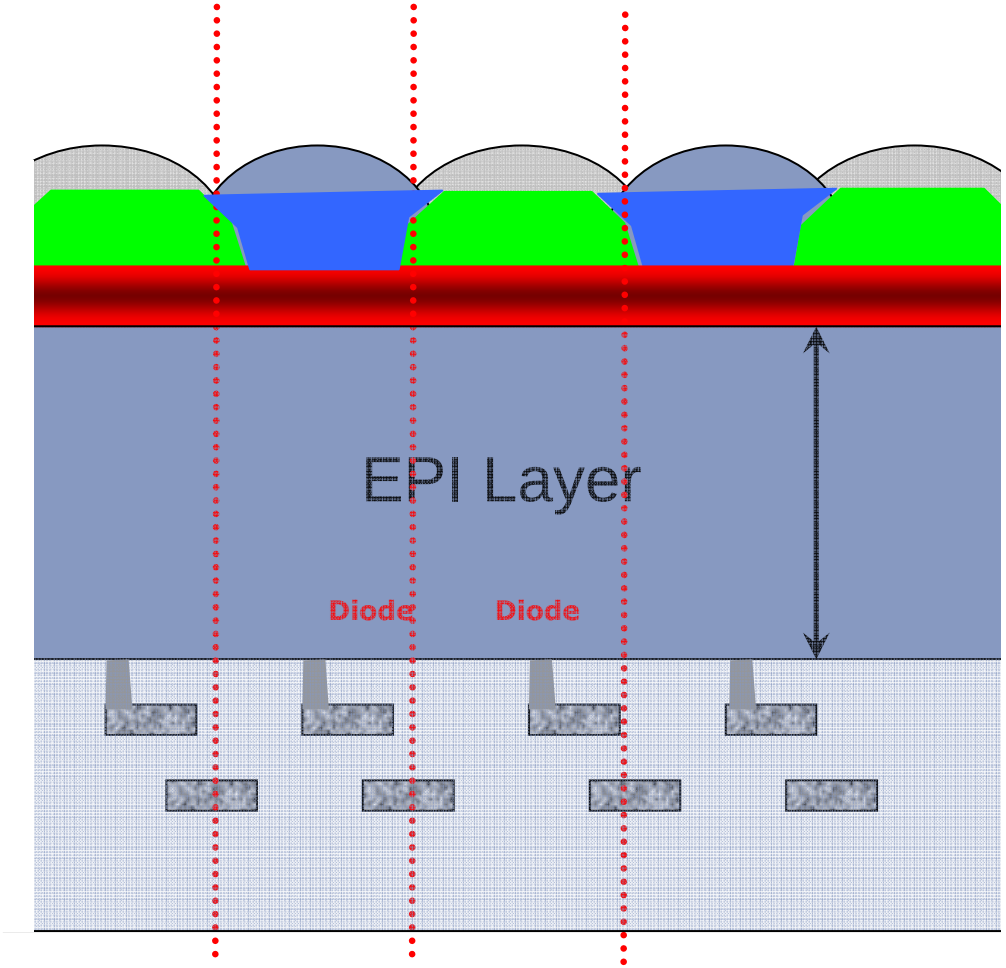
BSI starting Material : first issue



- Active Silicon thickness ?

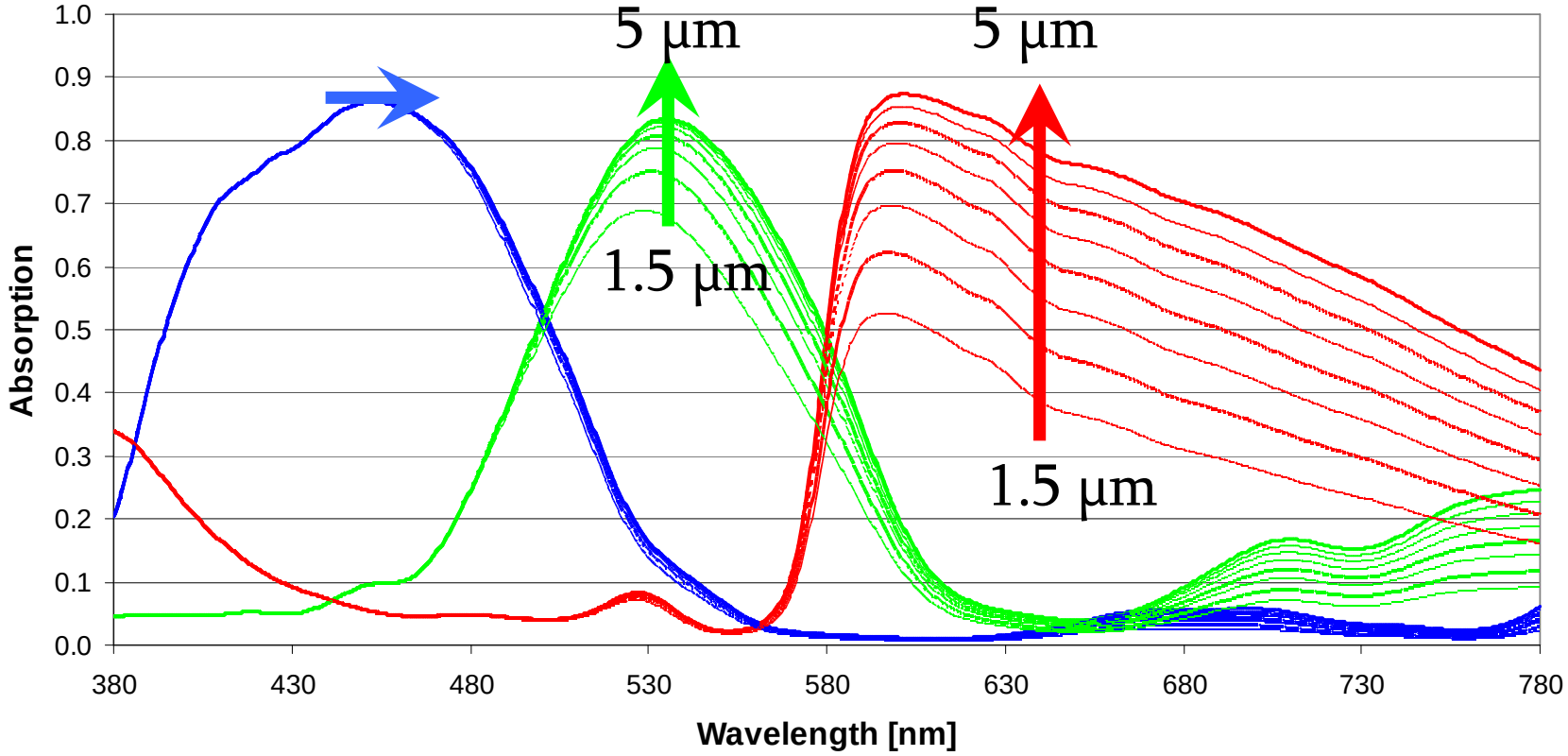
  - Epi thickness for SOI ?
  - Remaining Si layer thickness after thinning for bulk ?

Thin for cross talk improvement
Thick for Green and Red QE response

Signal absorbed in Silicon x Color Filter

Epi 1.5µm ➔ 5µm step 0.5 µm

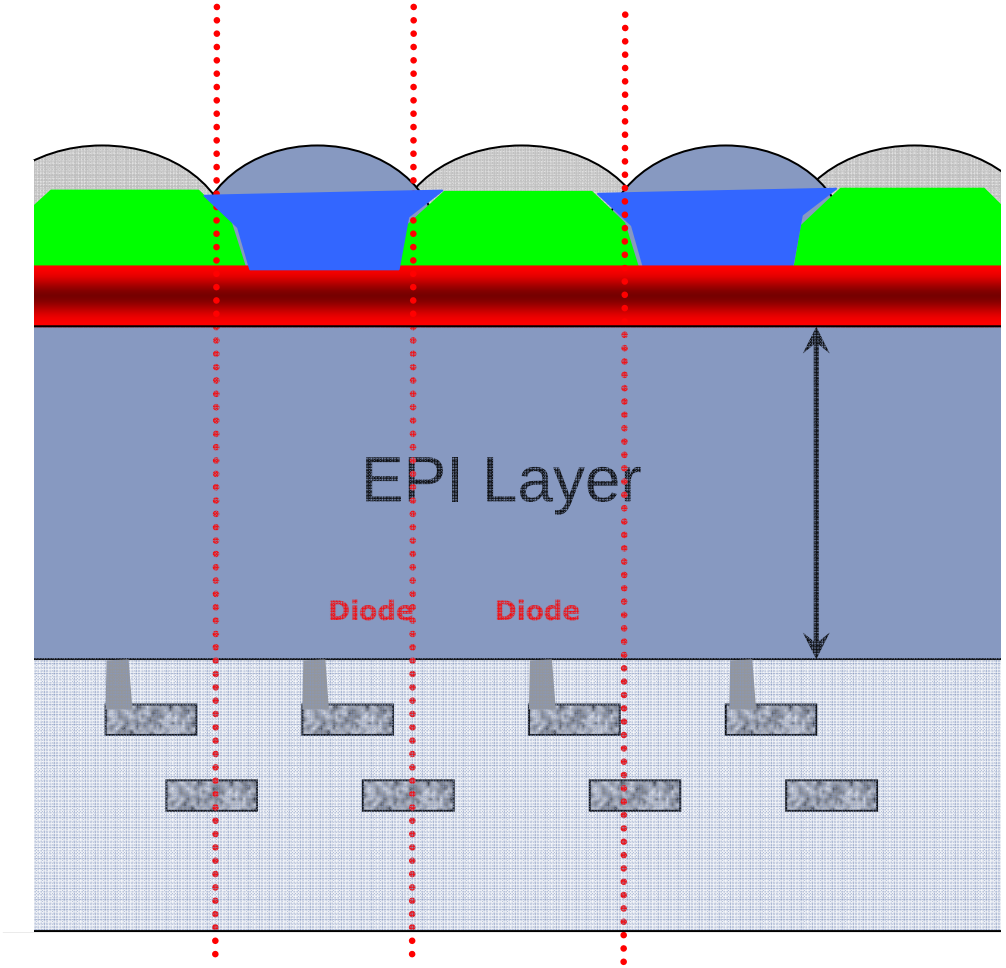
(Simulation Results)



Blue : xtalk care, Red : QE care, Green : xtalk and QE care

Courtesy of J.Vaillant ST

BSI starting Material : second issue



- Thinning Process

➢SOI with SiO2 etch stop layer ?

➢Bulk with P^{++} etch stop layer ?

Bulk thinning Process & challenges

- Bulk as starting material
  - Grinding
    - Coarse Grinding
    - Fine Grinding
  - CMP
    - Remaining Thickness control
    - Total Thickness Variation
  - Chemical thinning ➔ a critical point
    - P+ etch stop layer
    - Defect from P+ layer
    - Chemical Etching reveals defect
  - Implant and Laser annealing ➔ a critical point
    - Remaining defect from implant with Sub melt condition
    - Surface roughness defect for beyond melt condition
    - Melting layer thickness uniformity

SOI thinning Process & challenges

- SOI as starting material
  - Grinding
    - Coarse Grinding
    - Fine Grinding
  - Chemical thinning
    - Box etch stop layer — yield detractor << P+ layer
  - One option could be
    - No Laser annealing — no yield detractor
  - Other one option could be
    - BOX removal + laser annealing

Bulk – SOI competition

- SOI Starting material
  - The easiest process flow set-up
  - The concern is the wafer starting material cost
- Bulk Starting material
  - The process looks to be less robust (Si layer uniformity & Defect)
    - Etch stop layer and thinning process are the key process steps to be mastered
- Remaining questions
  - What will be the time to market for the Bulk versus SOI ?
  - Will ultimate performances be the same for Bulk and SOI ?

References

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