

Backside Illumination Technology For SOI-CMOS Image Sensors

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Backside Illumination of Solid-State Image Sensors**

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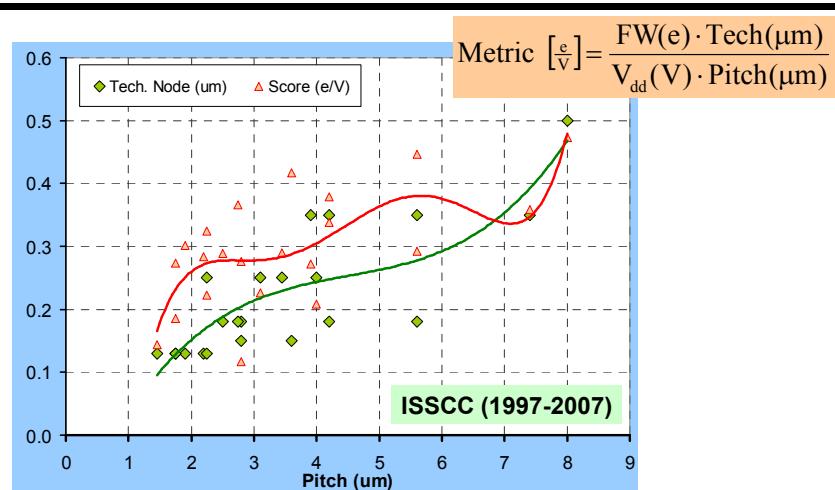
Homayoon Haddad

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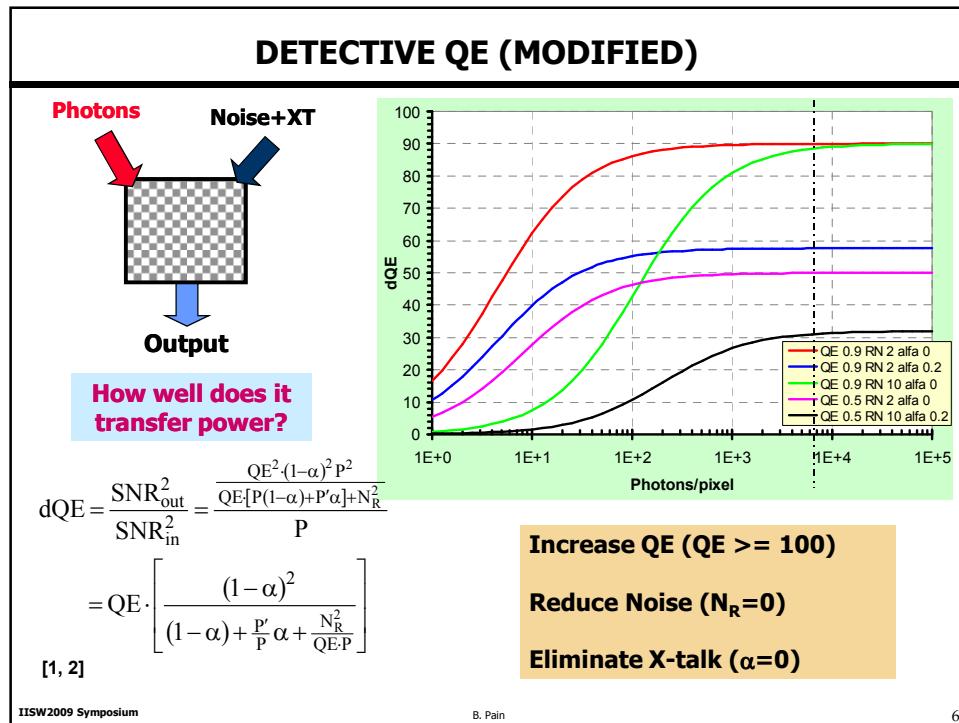
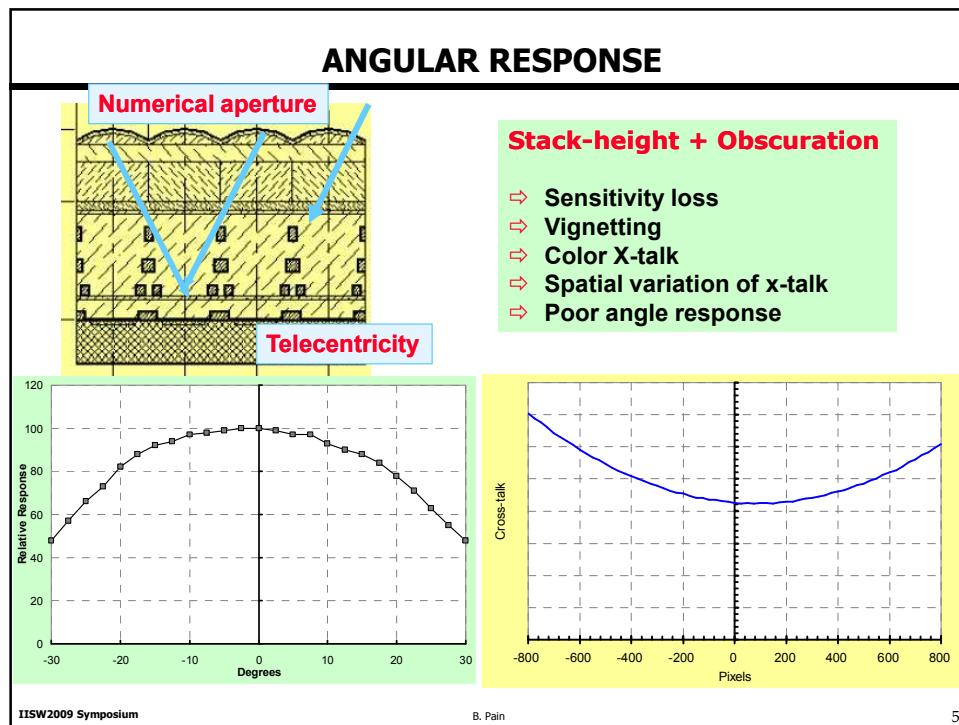
Indian Institute of Technology, Kharagpur

PROBLEMS of SMALL PIXEL

PIXEL SCALING TRENDS

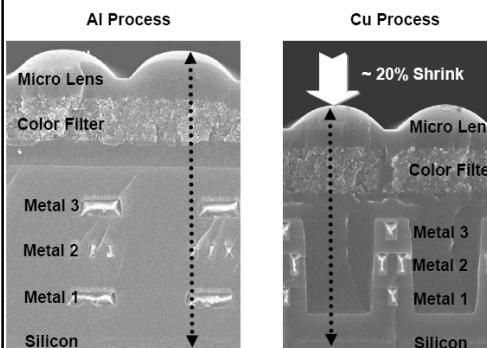


Continuous Technology "Breakthrough"
Needed to Keep up with the Scaling Trend

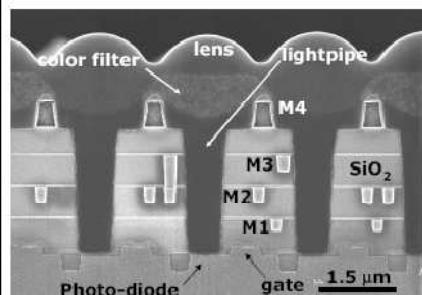


FRONT-SIDE ILD MODIFICATION

THINNER FRONT-END [3]



LIGHTPIPE APPROACH [4]

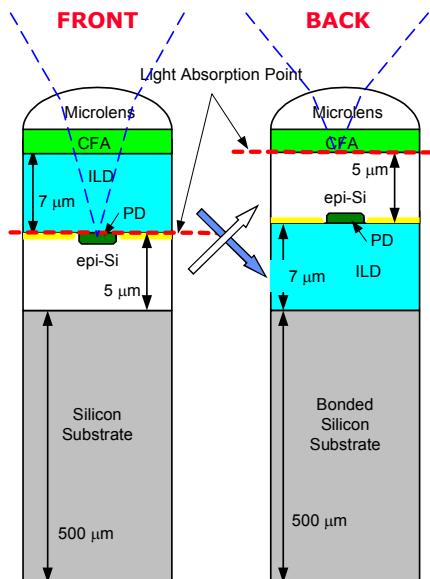


Process Complexities
Basic Problems remain

Difficulties in material selection

BACK-ILLUMINATION

BACK-ILLUMINATION: A SOLUTION



- **High Sensitivity and quantum efficiency**
100 % fill-factor

- **Excellent X-talk and Angular Response**

“Canyon” effect eliminated
No obscuration
Spurious reflections eliminated

- **Efficient microlens and anti-reflection coating**

Planar surface

- **Advanced pixel processing**

Dynamic range expansion
Global shutter
Gain ranging
Low noise

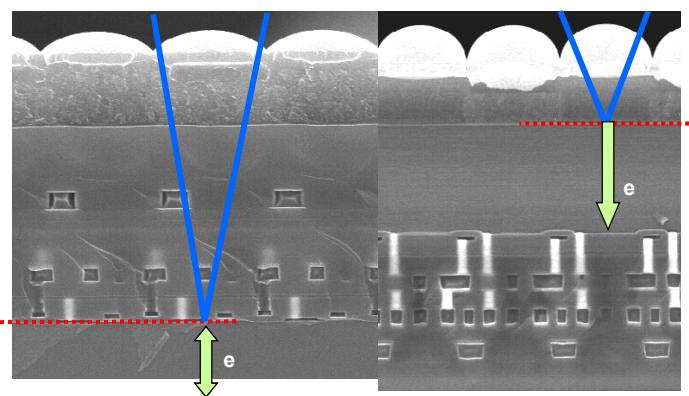
- **Compatibility with next generation dielectrics and metals**

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CROSS-SECTION



[5]

- Collection much closer to microlens
- No Obscuration
- Supports larger numerical aperture

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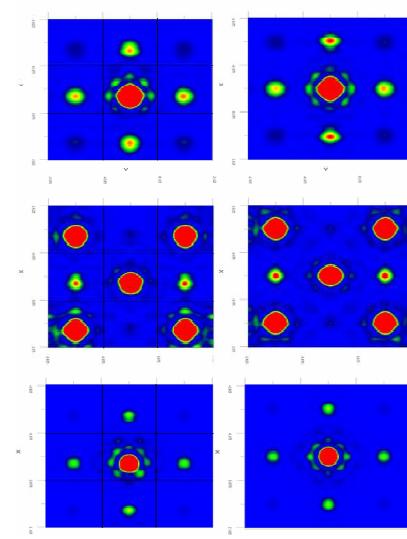
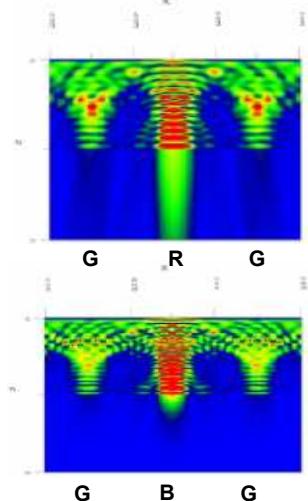
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BACK TO MAXWELL

Plenty of optical energy leakage due to pixel dimension, wave-effects, CFA

FDTD simulation of energy coupling



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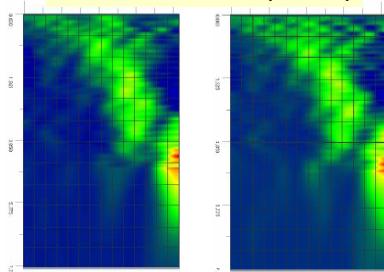
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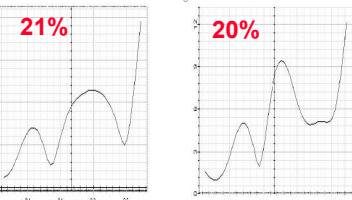
OPTICAL ADVANTAGE

Optical Coupling into Silicon for 1.75 μm pixel

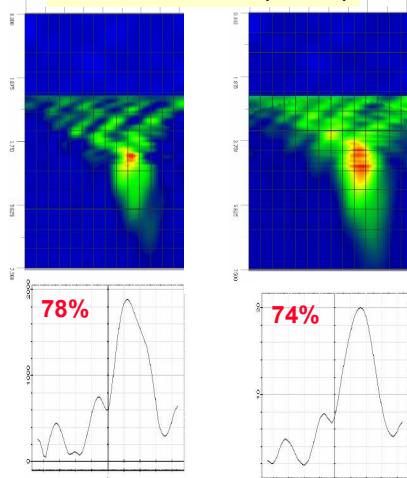
Front Illumination (TE/TM)



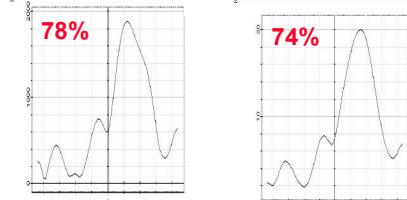
21%



Back Illumination (TE/TM)



78%



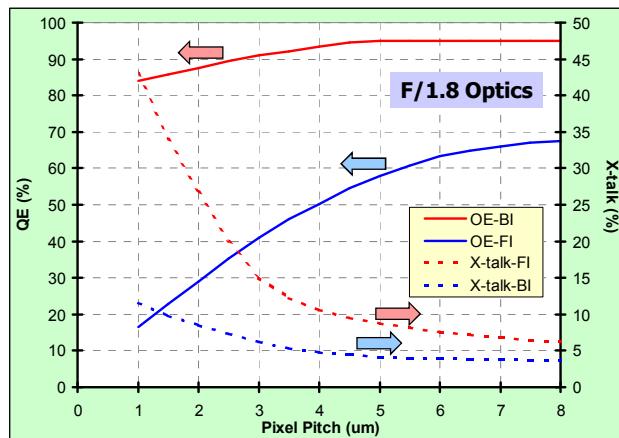
Almost 3x improvement at F 2.0

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QE & OPTICAL CROSS-TALK



- QE goes down and Cross-talk goes up
- QE loss due energy spread via E-M field propagation
- Front-side QE also limited by imperfect AR coating

BACK-THINNING ISSUES

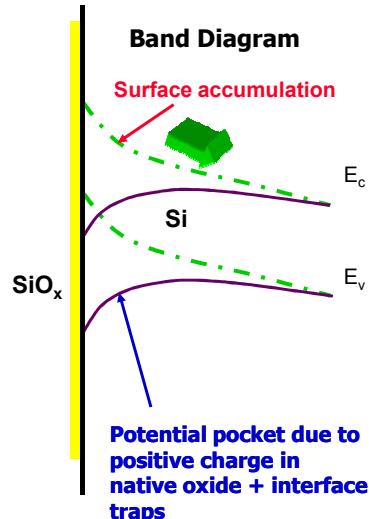
Manufacturable + Wafer-level Processing + Good device performance

- Accurately thinning 700 μm substrate with <50 Å surface roughness
 - ⇒ Appropriate etch-stop
- Backside passivation
 - ⇒ Hold exposed surface in accumulation
- Device support (during and after thinning)
 - ⇒ Attachment of support wafers – must allow post-processing
- Packaging
 - ⇒ Where do pads come out from? Wire-bond or CSP?
- AR coating, Color, Microlens
 - ⇒ Alignment key
 - ⇒ Stack issues
- Diffusion Cross-talk Control
 - ⇒ Field-shaping implants
 - ⇒ Back-surface gradients

PASSIVATION OF EXPOSED SURFACE

PASSIVATION PROBLEM:

- Exposed Si-SiO₂ interface quality is poor
 - high trap density, potential pocket due to band-bending
 - loss of blue QE and high dark current

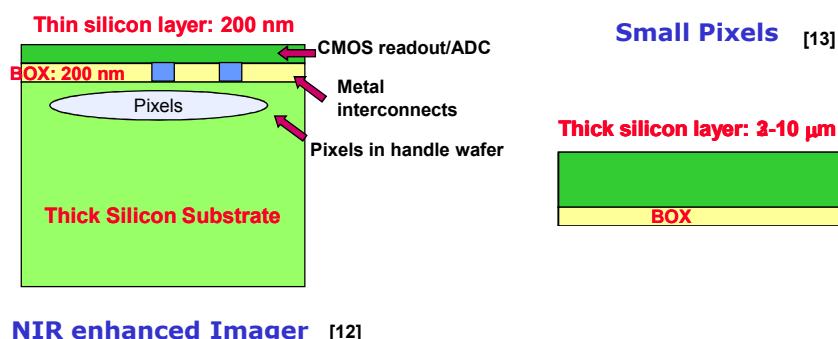


BACKSIDE TREATMENT

- Implant + RTA Anneal
 - Cannot be used due to the presence of metals
- Implant + Laser Anneal [6, 7]
 - PRNU, Dark current
- Delta-doping: few monolayers of boron added by MBE to the back surface [8]
 - Excellent results, but non-standard process
- Flash gate: deposited oxide + UV flooding [9, 10]
 - Outgassing, Long-term stability
- Back-gate: deposited oxide + Silver capping [11]
 - Non-desirable metal; AR coating issues
- Back-gate: deposited oxide + ITO gate
 - Process Control; AR coating issues

FABRICATION STEPS

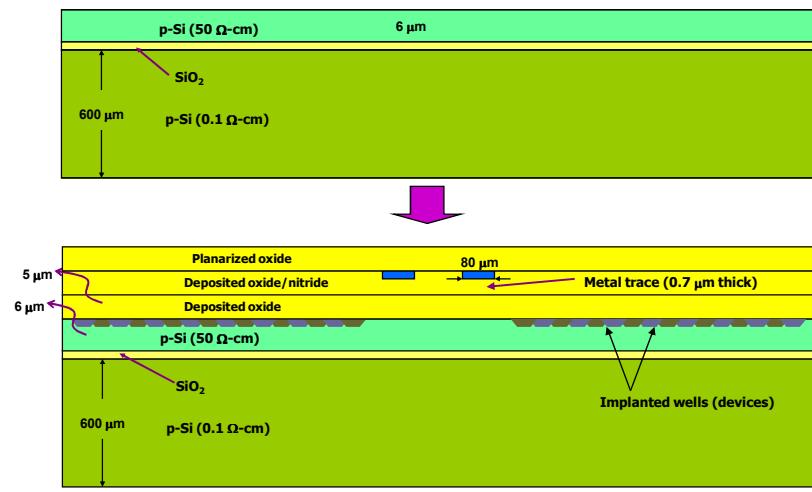
SOI TO THE RESCUE



SOI IMAGER FABRICATION

- SOI wafer with thick device layer (~ 2-10 μm)
- Imager-compatible bulk-CMOS process

[13, 14]

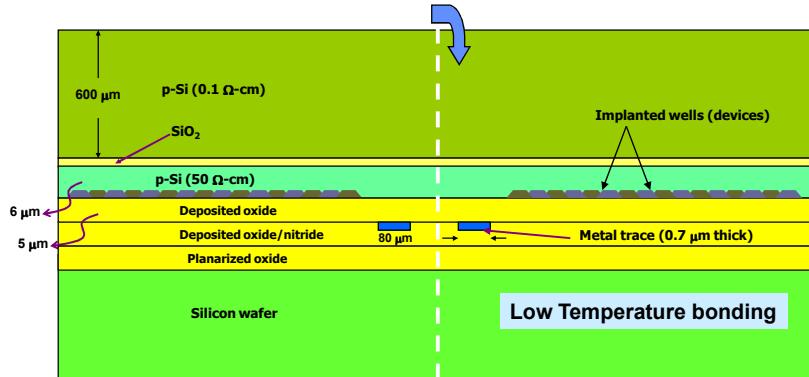
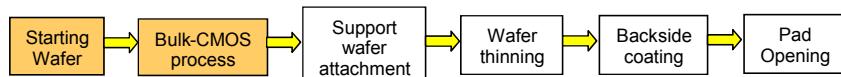


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SOI IMAGER FABRICATION



- Provides mechanical support
- Bonding process/material must be back-end compatible

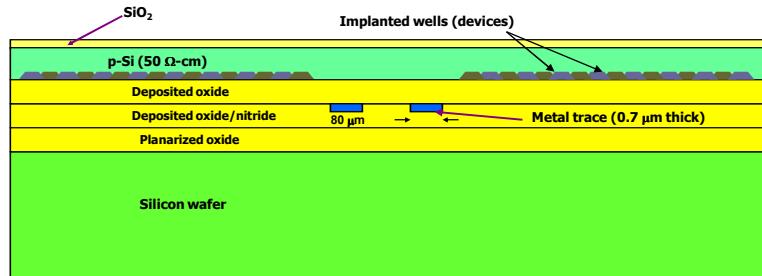
[15]

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THINNING



THINNING

- Wafer-level thinning
- Natural high-selectivity (Si-SiO₂) etch-stop

PASSIVATION

- Buried oxide made by thermal oxidation
- Pre-implanted region for passivation
- Self-passivation: surface never exposed

Chemical Etch

- Hot KOH/TMAH wet-etch
- RIE with SF₆
- XeF₂ vapor-phase

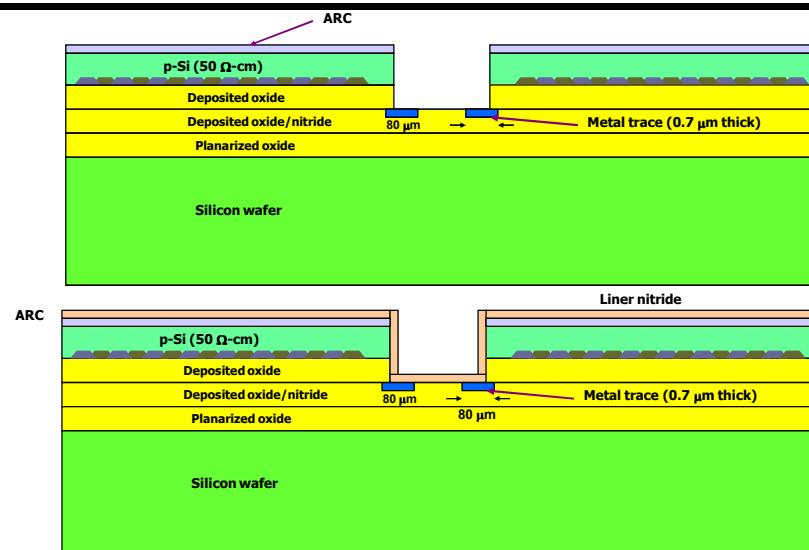
	KOH	SF ₆	XeF ₂
Local	<20 Å	<500Å	<20Å
Global	<200Å	3000Å	<40

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BACK-to-FRONT ALIGNMENT



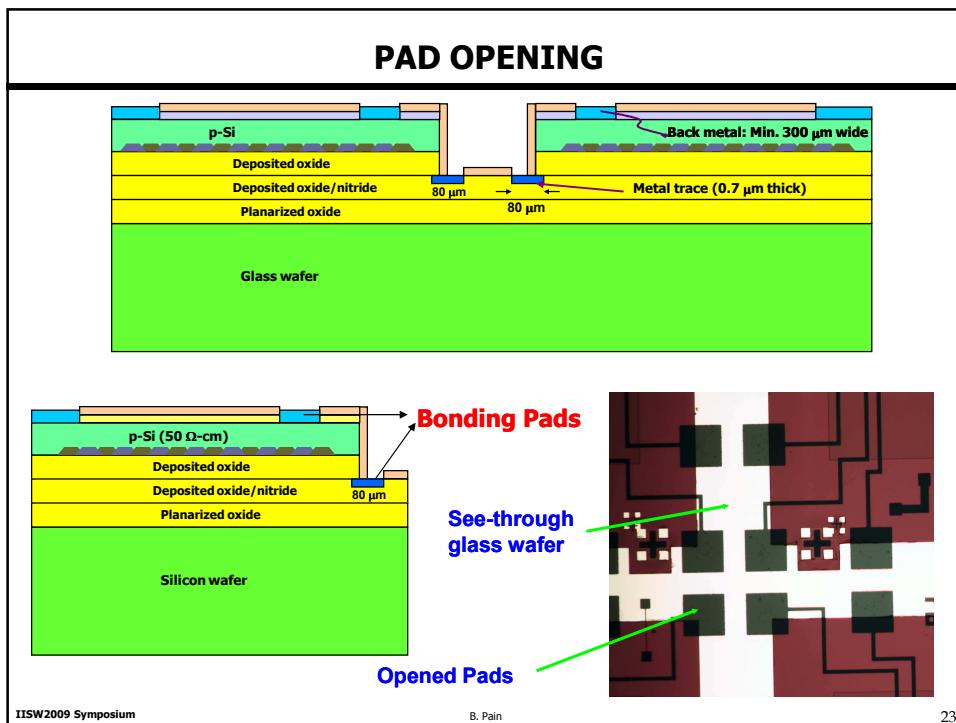
Exposed metal holds alignment keys

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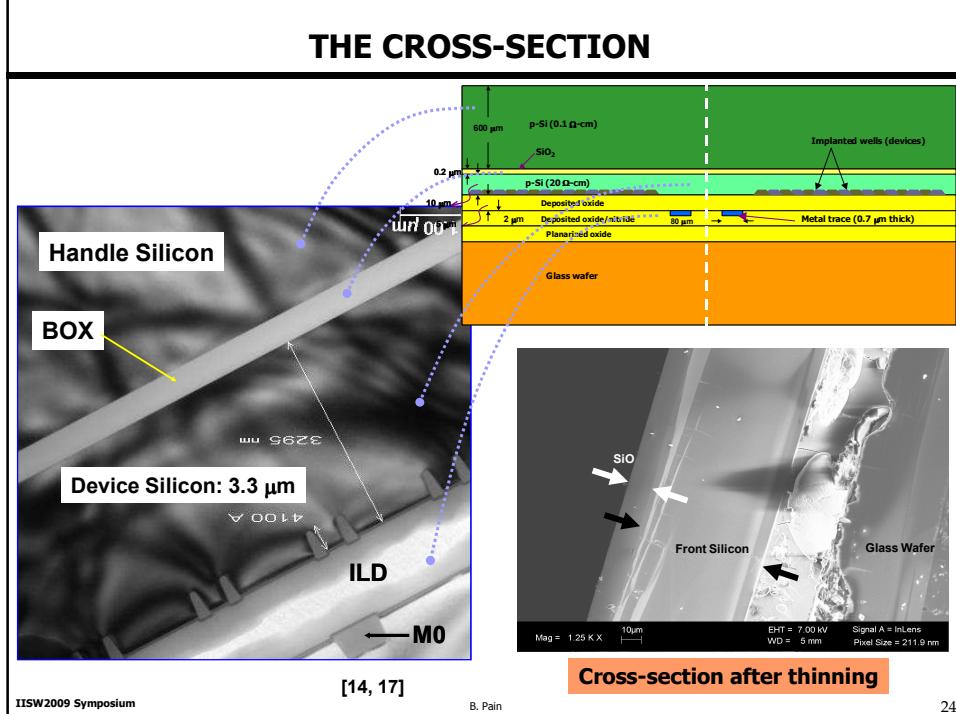
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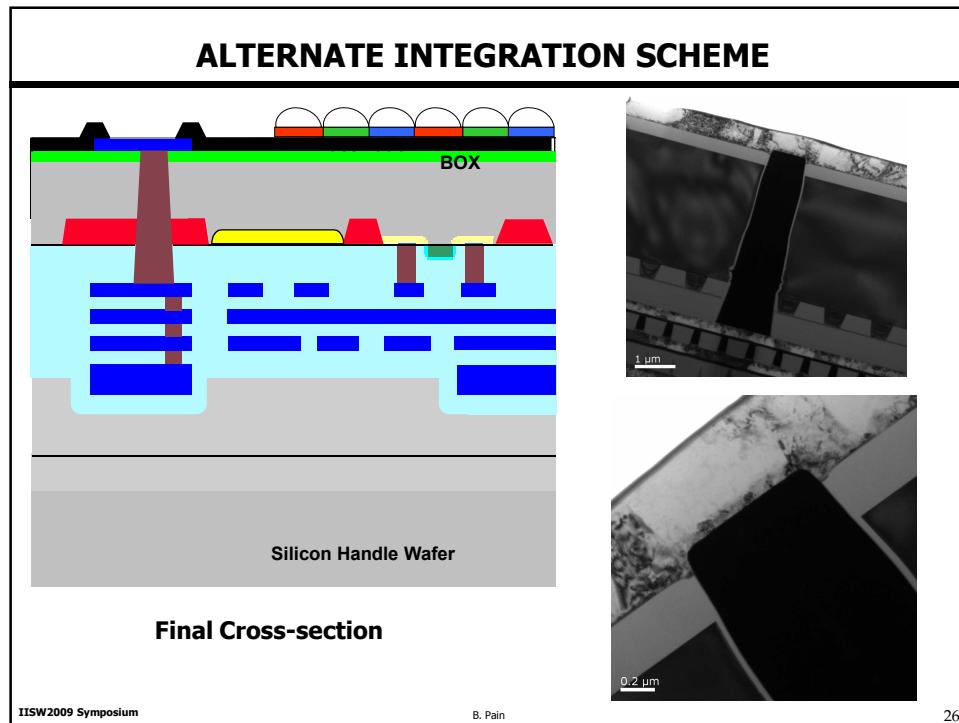
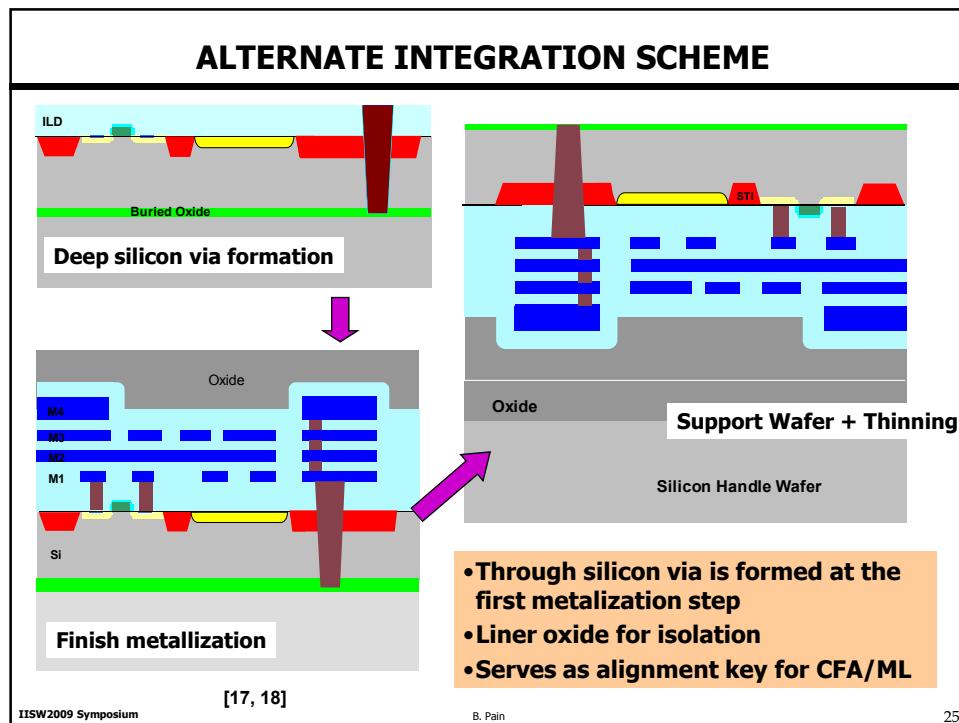
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PAD OPENING

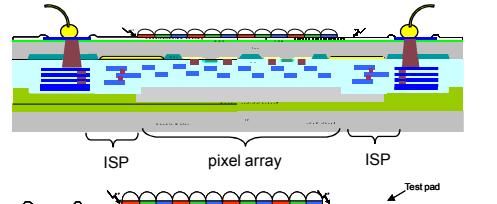


THE CROSS-SECTION



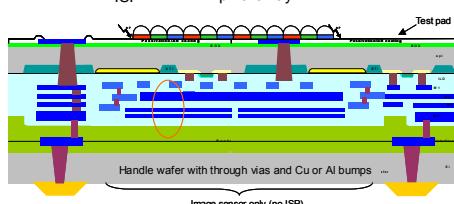


POSSIBLE EVOLUTION



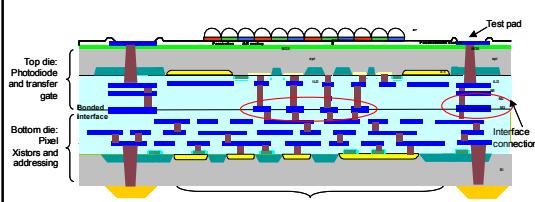
1st Generation

Through Silicon Contacts for wirebonds
Pixel optimization



2nd Generation

Higher Dynamic Range – In-pixel Cap
Better Z-height - WLCSP



3rd Generation

Only pixel in wafer – best performance
SOC integration

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PERFORMANCE

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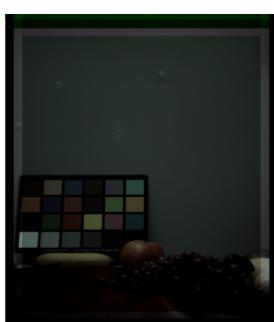
COLOR BIS IMAGER



Back-illuminated 1.75 μm Color Picture

[17]

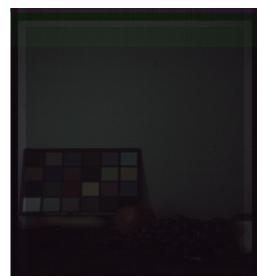
PERFORMANCE IMPROVEMENT



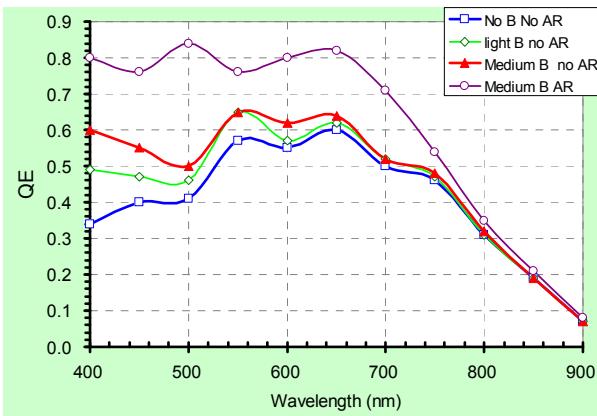
Median luminance = 3 lux

Median luminance = 690 lux for D65

- ↑ 2.5x increase in Sensitivity for 2.2 μm pixel
- ↑ Dark current & Full-well about the same
- ↑ Angular response improves by 5x
- ↓ Electrical cross-talk worse



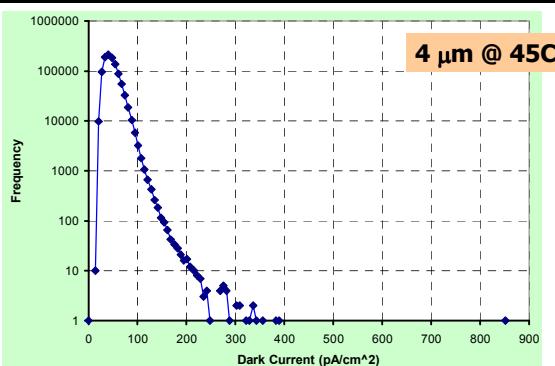
QUANTUM EFFICIENCY



- Surface Boron is an effective tool to improve QE
- Blue QE affected by boron content at the surface
- For color Imager: 20% loss going through CFA and OCL

[14]

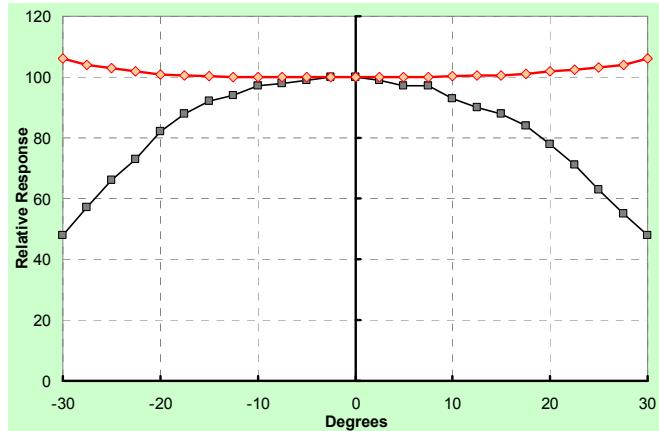
WELL BEHAVED DARK CURRENT



Front Illuminated	Nitride cover	53
Back surface Boron	Nitride + H ₂ anneal	Dark Current (e/sec)
Minimum	None	8000
Small	None	419
Small	Yes	133
Medium	Yes	57
High	Yes	76

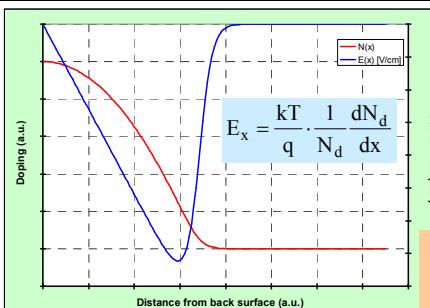
[14]

ANGULAR RESPONSE



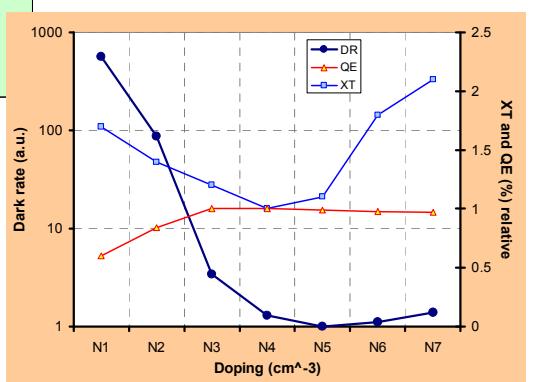
Slight increase in relative angular response is due to optical path difference

BACK FIELD



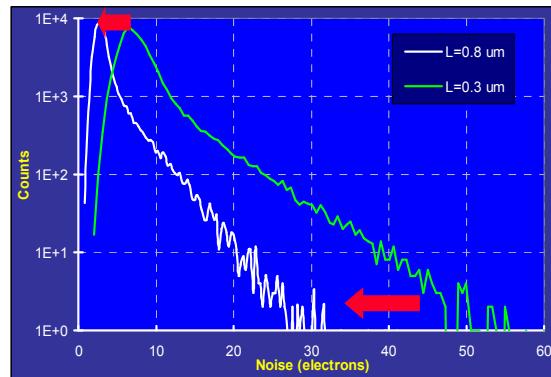
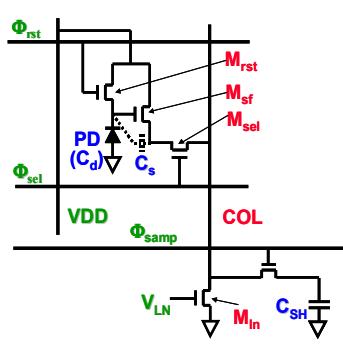
Doping Trade-offs

- Simulated Nominal Back doping gradient and electric field
- Back-field drives minority carriers towards front
- Back-field suppresses Cross-talk
- Proper doping gradient is extremely important



RTS NOISE REDUCTION

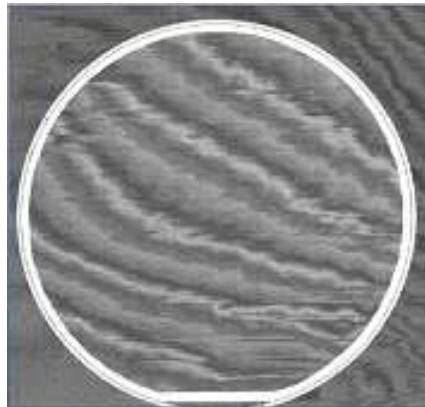
$$C_{SH} = 1.5 \text{ pF}; G_{cp} \sim 45 \mu\text{V/e}; I_{bias} = 3 \mu\text{A}$$



- Source follower as the main source of RTS
- Both modal noise and noise spread is reduced by length increase

MANUFACTURABILITY ISSUES

SUPPORT WAFER BONDING



Acoustic micrograph of low-temperature oxide-oxide bonded support wafer (courtesy Ziptronix, Inc.): No voids

Passes die-level thermo-mechanical tests (thermal shocks and temperature cycles)

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Alternate schemes?

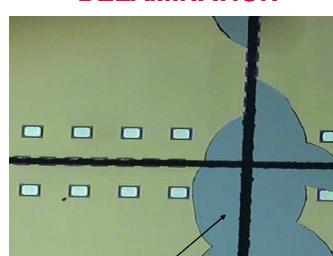
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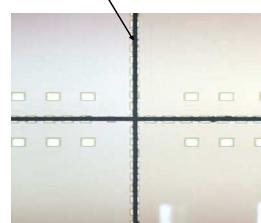
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"PEEL OFF"

DELAMINATION



Sawing Process optimization to prevent delamination



EDGE EXCLUSION



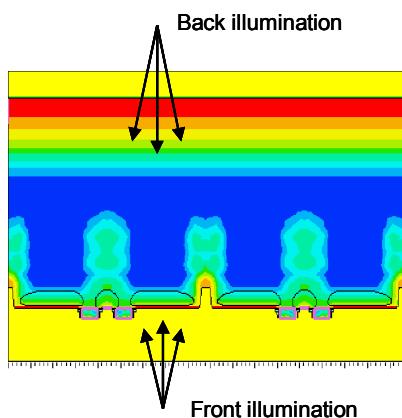
Optimization of bonding and grinding process to eliminate edge-cracking during subsequent processing

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THE THREE THINGS ...



Electrical Cross-talk

- Separated generation and collection area
- Back surface field
- Deeper Junction

QE

- Integration of AR stack on the BOX

Dark Current

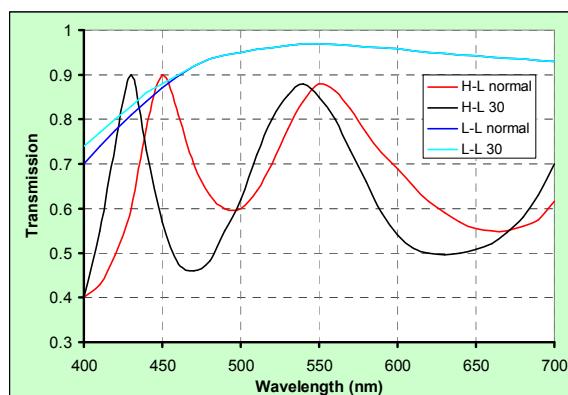
- Back surface passivation with integrated AR stack

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AR STACK OPTIMIZATION



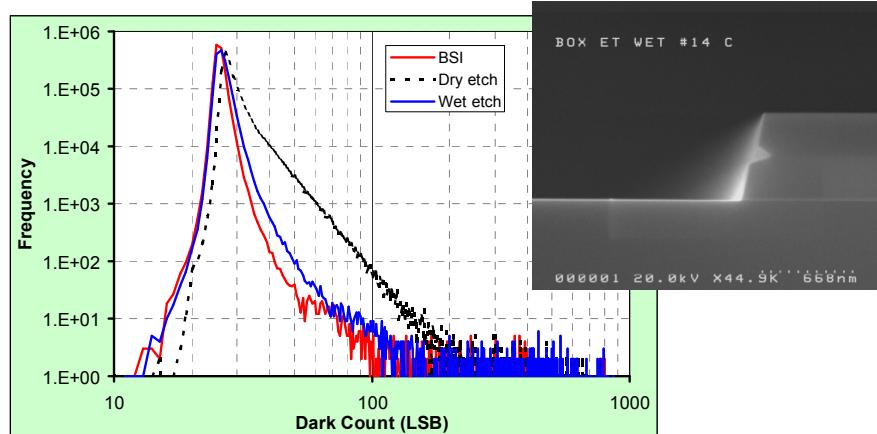
- Excellent AR stack can be achieved with SiN/SiO layers
- Need to ensure that angular response is acceptable
- BOX not the ideal-choice for 1st AR layer

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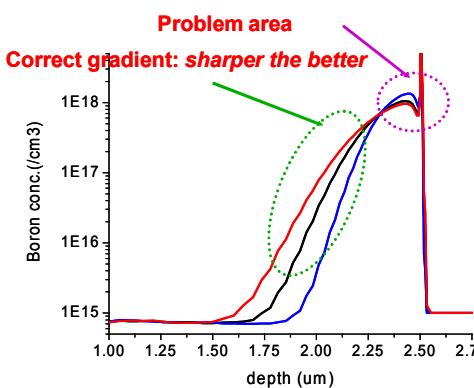
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DARK CURRENT with AR STACK

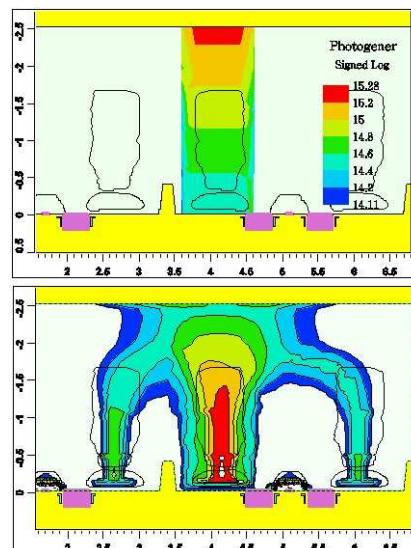


BOX etching does not increase dark current, if done right!

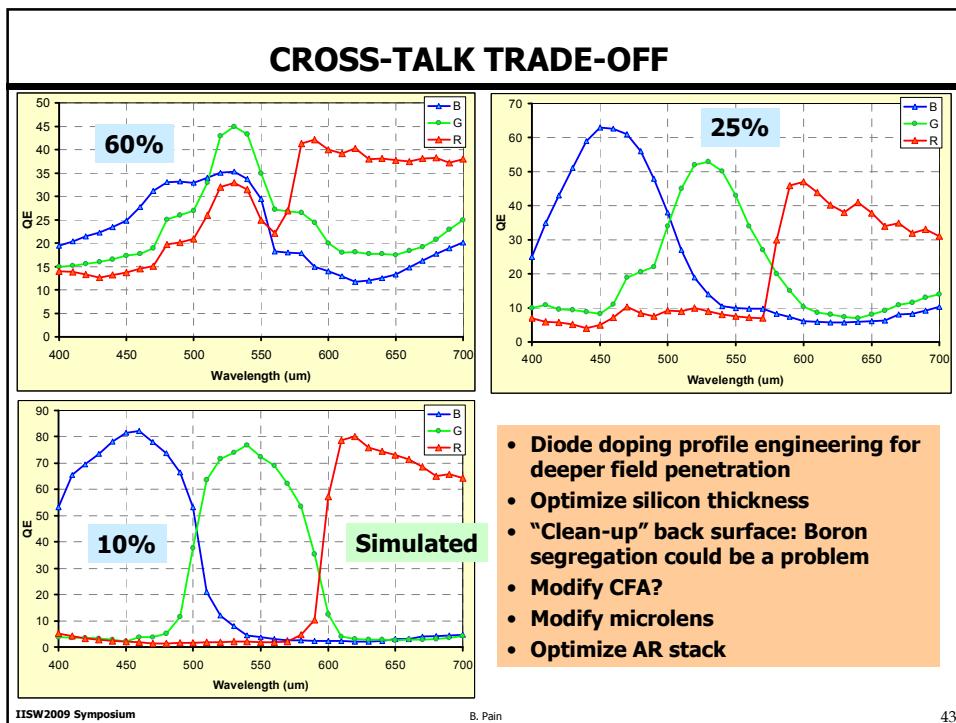
CROSS-TALK



Simulated Current flow



- Boron needed to passivate interface states
- Boron gradient needs to be optimized
- Boron segregation is the source of problems
- N-type substrate is preferable



MOVING FORWARD (in lieu of conclusion)

Cost - how low can you go?
 Special SOI wafer needed?
 Will SOI wafer become cheaper and have shorter turn-around time?
 Where are the yield and reliability “gotchas”?

Performance
 SOI wafer quality? Will lack of gettering be an issue?

Alternate Support Wafer Attachment
 Need for an alternative to LT-bonding? Alternate support materials?

Appropriate Optical Stack
 What materials for AR stack?
 Alternate CFA?

Improving Cross-talk
 Boron segregation - N-type material?
 Alternate diode profiles and barrier implants? Deep trenches?
 Alternate dielectric for improved passivation? ITO?

Packaging
 Chip-on-board (COB) or Chip-scale-packaging (CSP) or wafer scale (WSP)?

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