Fully depleted, BSI CCDs on high-resistivity silicon

2009 IISW Symposium on Back Illumination of Solid-State Image Sensors

June 25th, 2009

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University of California Observatories / Lick Observatory

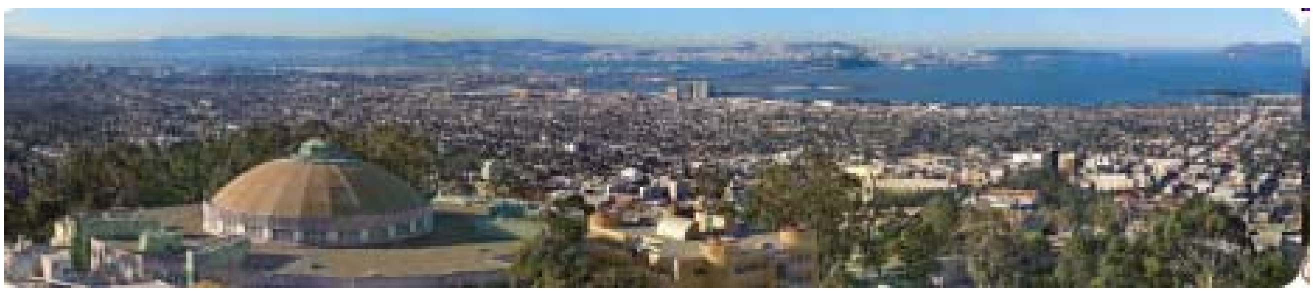
Introduction to Lawrence Berkeley National Laboratory

LBNL is one of the U.S. Department of Energy's national laboratories, and is managed for the DOE by the University of California

The Laboratory conducts unclassified research and has an annual budget of approximately $600 million U.S. dollars

Founded in 1931 by Ernest Lawrence, the Laboratory employs ~ 4000 scientists, engineers, and support staff

The CCD development work is done under the auspices of the Physics Division with major support from the Engineering Division



Outline

- Fully depleted CCD physics and performance
  - — Quantum efficiency and fringing
  - — Spatial resolution
  - — Transistors fabricated on high-resistivity silicon
  - — Backside defects

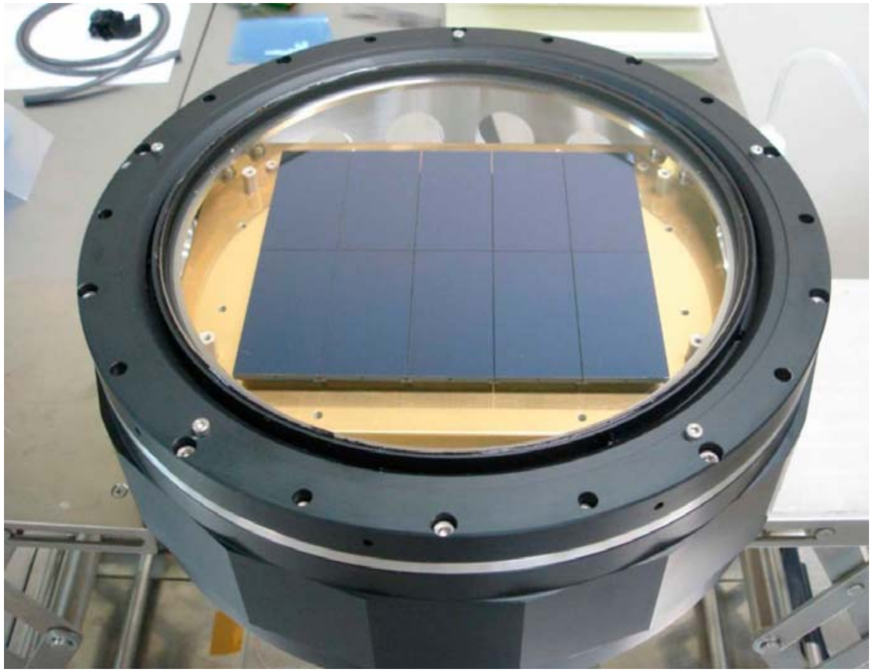
- CCD fabrication
  - — Hybrid fabrication model
  - — Dark Energy Survey project
  - — 4k x 4k (15 μm pixel) development

- Summary

Impact of fully depleted, back-illuminated CCDs on astronomy and astrophysics

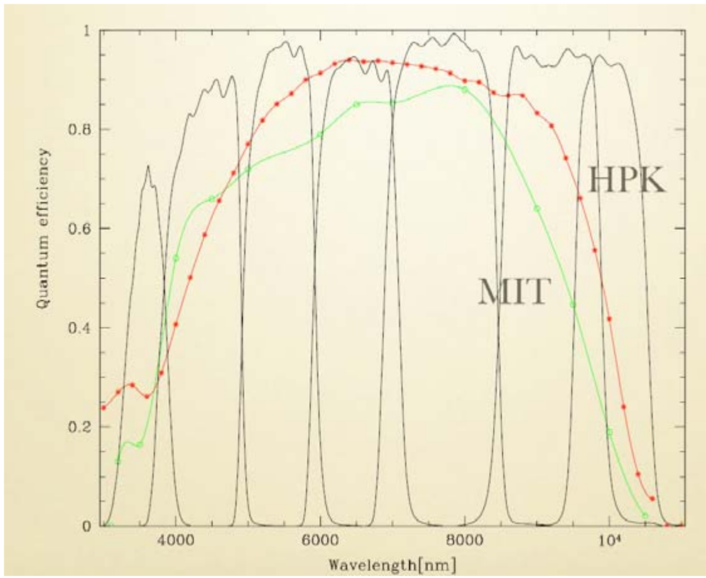
- Many major camera upgrades at ground-based telescopes are using or are planning to use fully depleted, back-illuminated CCDs:
  - Subaru Super and HyperSuprime Cameras
    - 10, 2048 x 4096 (15 µm pixel), 200 µm thick, fully depleted p-channel CCDs in operation since August 2008 (Super Suprime-Cam)
      - http://www.naoj.org/Pressrelease/index_2008.html#081120
    - HyperSuprime-Cam will require ~ 200 CCDs
    - Fabricated by Hamamatsu Corporation

Commercial development of FD CCDs



2k x 4k CCDs fabricated at Hamamatsu Corporation for the Subaru Telescope

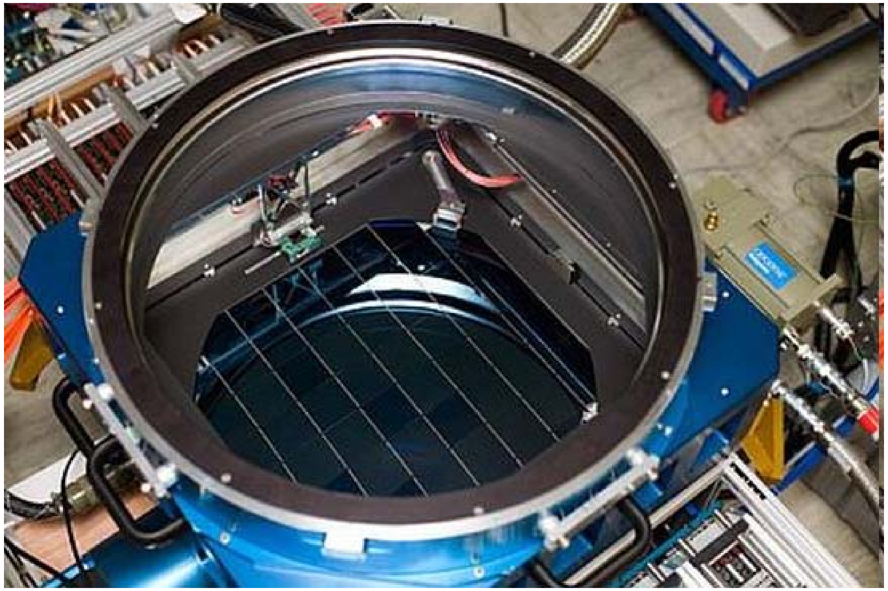
http://www.naoj.org/Pressrelease/index_2008.html#081120



—Pan-Starrs (University of Hawaii)

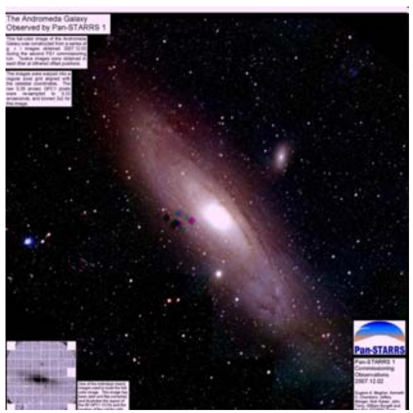
- 1.4 Gpixel camera, 1 installed August 2007 with 3 more proposed
- MIT Lincoln Laboratory orthogonal transfer, 75 μm thick fully depleted n-channel CCDs fabricated on ~ 5 kΩ-cm, p-type silicon
- 60, ~ 5k x 5k (10 μm pixel) CCDs per camera
- http://pan-starrs.ifa.hawaii.edu/public/
- Similar project: WIYN Observatory One-degree imager

—Pan-Starrs (University of Hawaii) cont’



Images from Pan-Starrs 1 Camera

Early 2008 commissioning



Impact of fully depleted, back-illuminated CCDs on astronomy and astrophysics (cont')

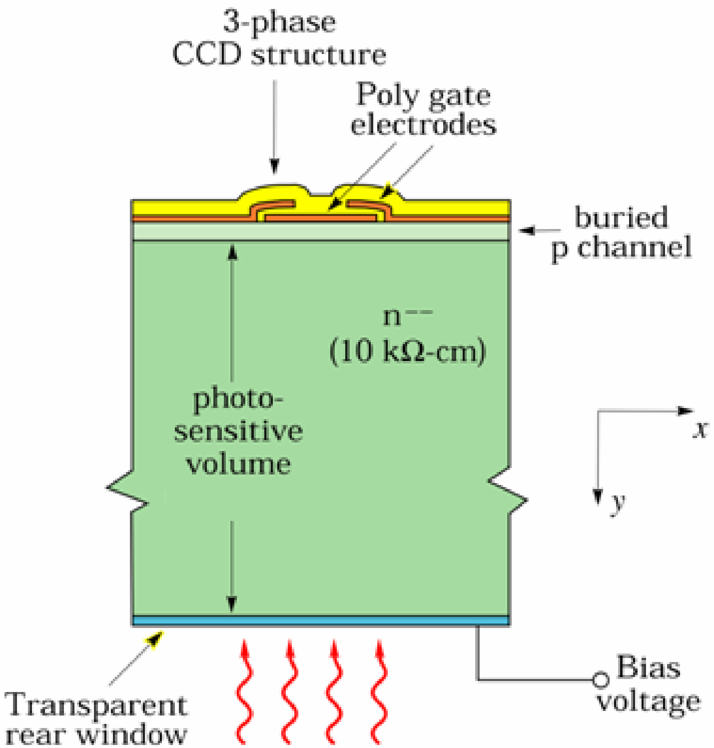
—Dark Energy Survey camera

- 62, 2048 x 4096 (15 µm pixel), 250 µm thick, fully depleted p-channel CCDs (~ 0.5 Gigapixel camera)
- Fabrication at DALSA/Lawrence Berkeley National Laboratory, packaging and testing at Fermi National Accelerator Laboratory
- http://www.darkenergysurvey.org/

—Large Synoptic Survey Telescope (LSST)

- ~ 200, 4k x 4k (10 µm pixel), 100 µm thick, fully depleted CCDs required (~ 3.2 Gigapixel camera)
- http://www.lsst.org/lsst/science/concept_camera

Fully depleted, back-illuminated CCD



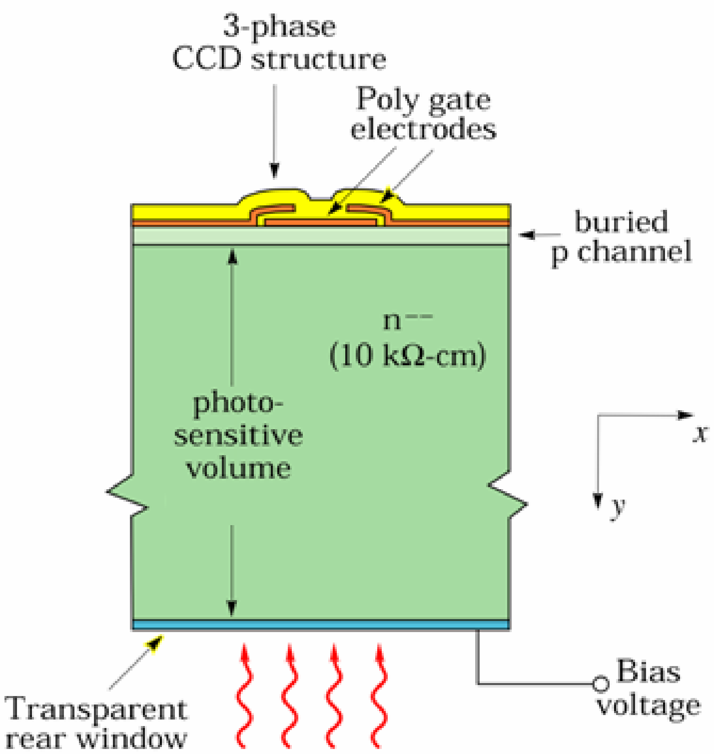
1) Concept: Fabricate a conventional CCD on a thick, high-resistivity silicon substrate
   - 200-250 µm typical, 675 µm in special cases

2) Use a substrate bias voltage to fully deplete the substrate of mobile charge carriers
   - Merging of p-i-n and CCD technology
   - High-ρ Si allows for low depletion voltages

3) The thickness results in high near-infrared quantum efficiency and greatly reduced fringing

4) The fully depleted operation results in the ability to control the spatial resolution via the thickness and the substrate bias voltage

Fully depleted, back-illuminated CCD



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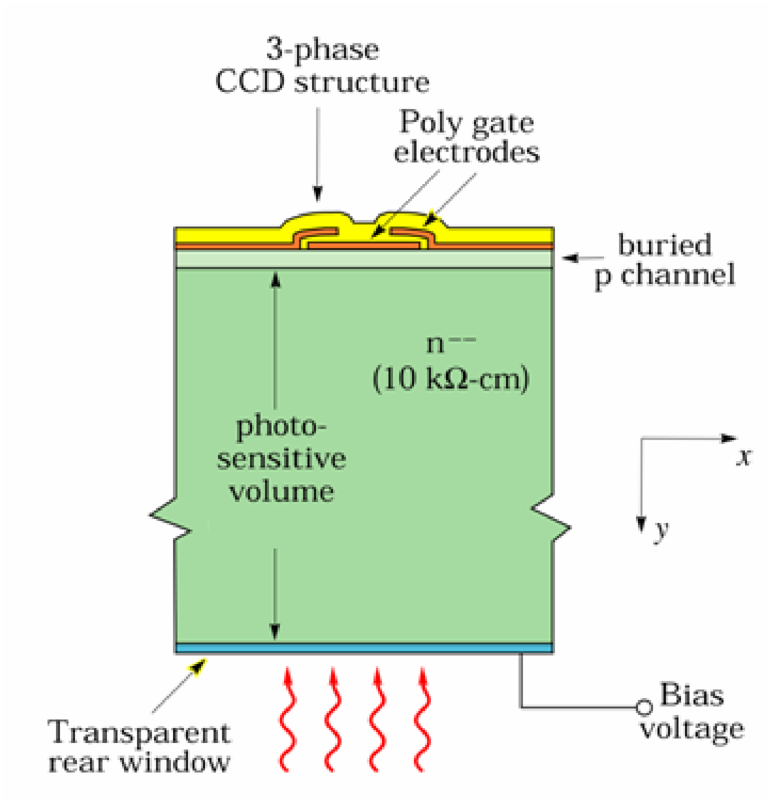
10 kΩ-cm corresponds to a doping level of ~ 4 x 10^{11} cm^{-3}, or about 1 part in 10^{11}

Fully depleted, back-illuminated CCD



Drawbacks of thick, fully depleted CCDs:

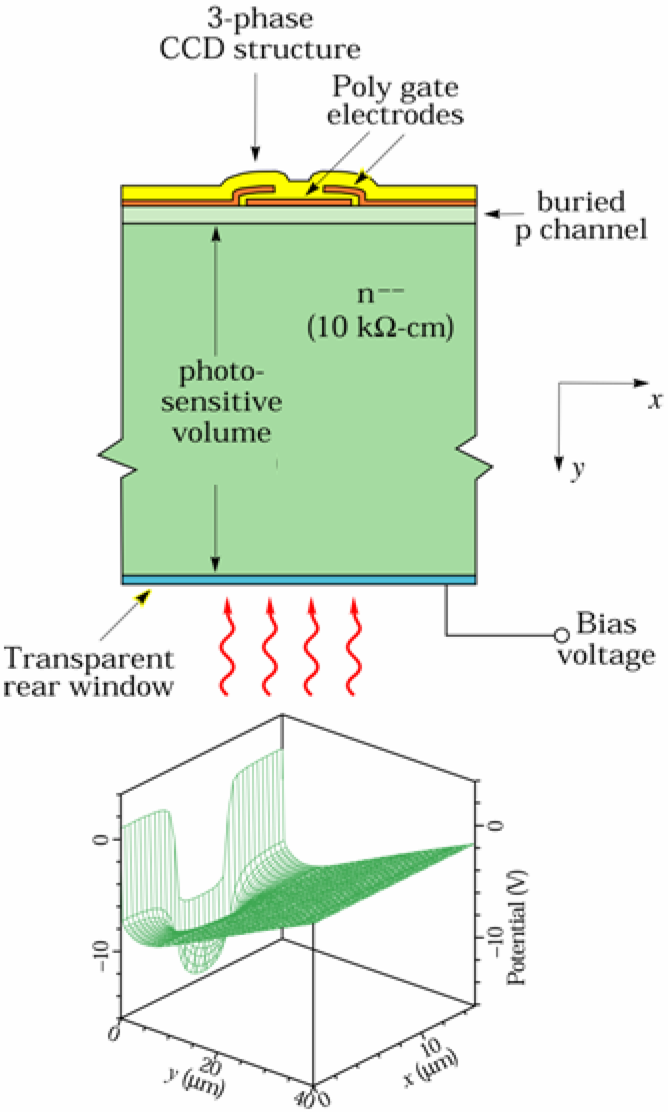
1) Charged particles leave ionizing tracks
   - Cosmic rays, Compton electrons
   - More pixels affected than in a thin CCD

2) Imaging with long wavelength light could result in degraded spatial resolution when fast optics are used

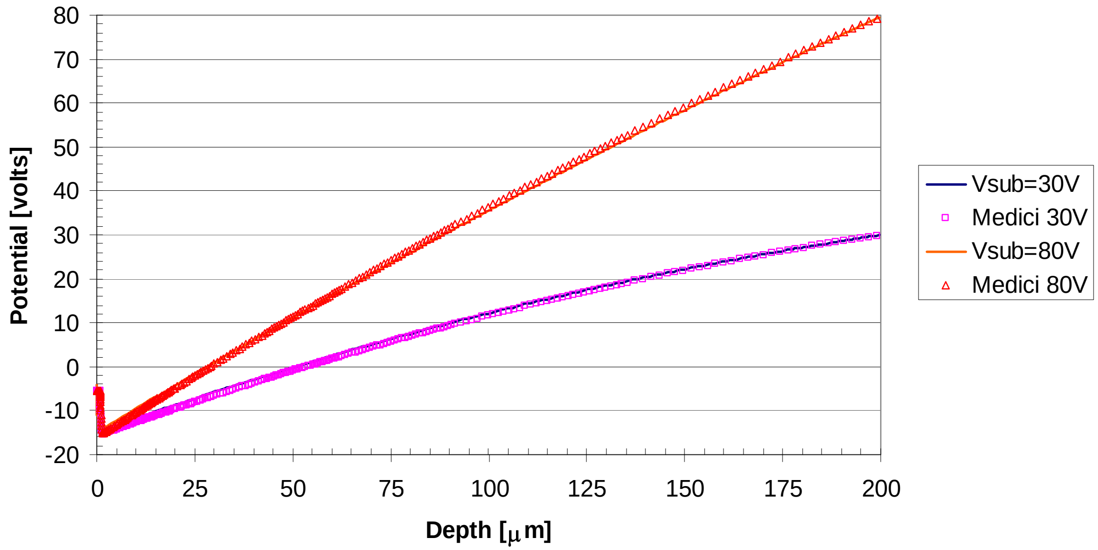
3) Surface "pinning" methods to reduce surface dark current are not straightforward to implement when large substrate bias voltages are used

4) Susceptible to backside defects, especially for overdepleted operation

Fully depleted, back-illuminated CCD



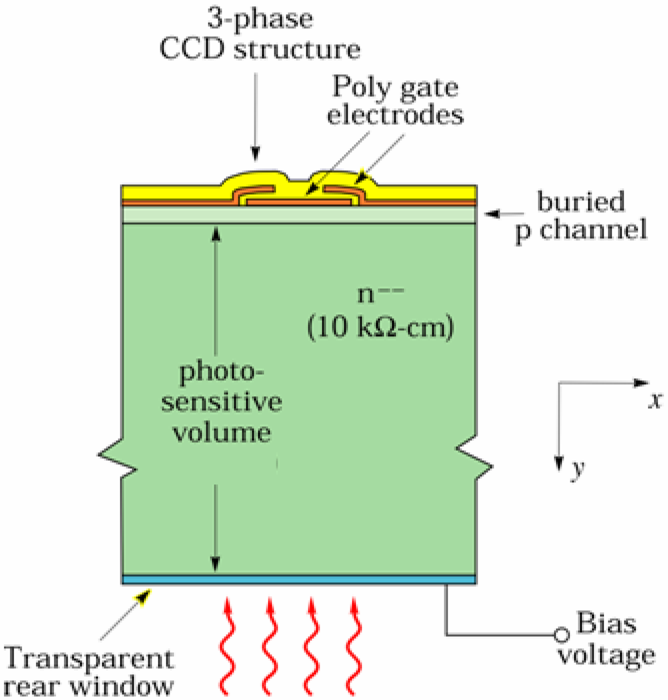
MEDICI 2-D simulation

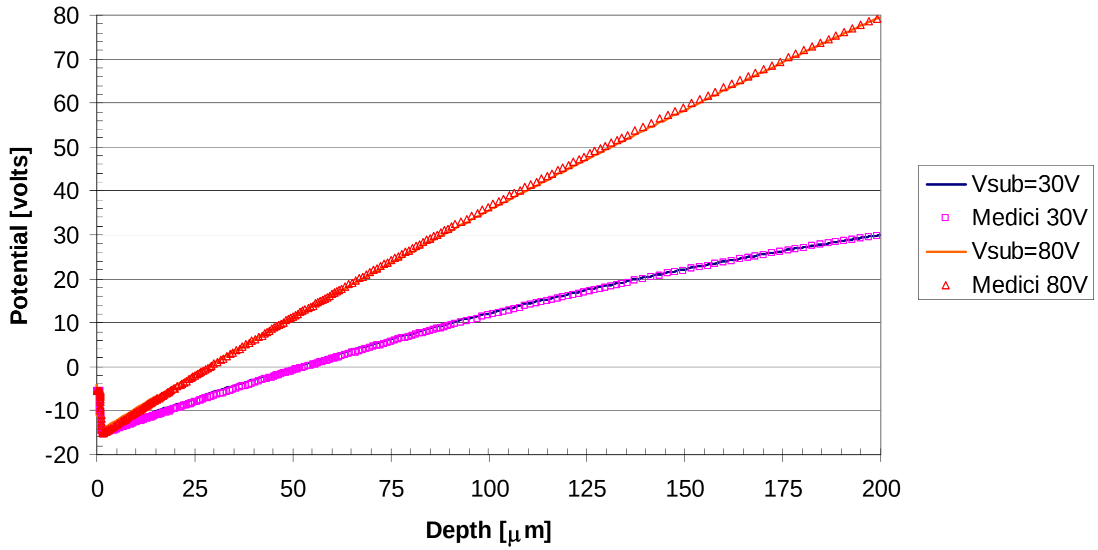


Potential versus depth along center of pixel
1-D potential calculations and Medici simulation

The fully depleted operation produces a drift field throughout the detector substrate

Fully depleted, back-illuminated CCD





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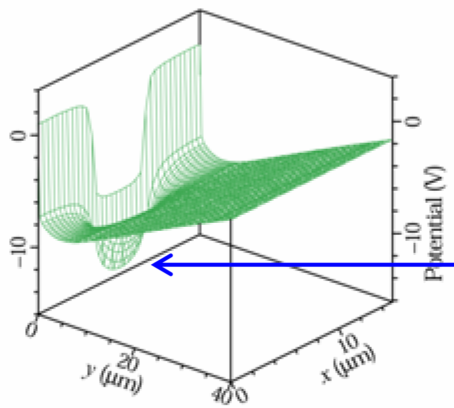
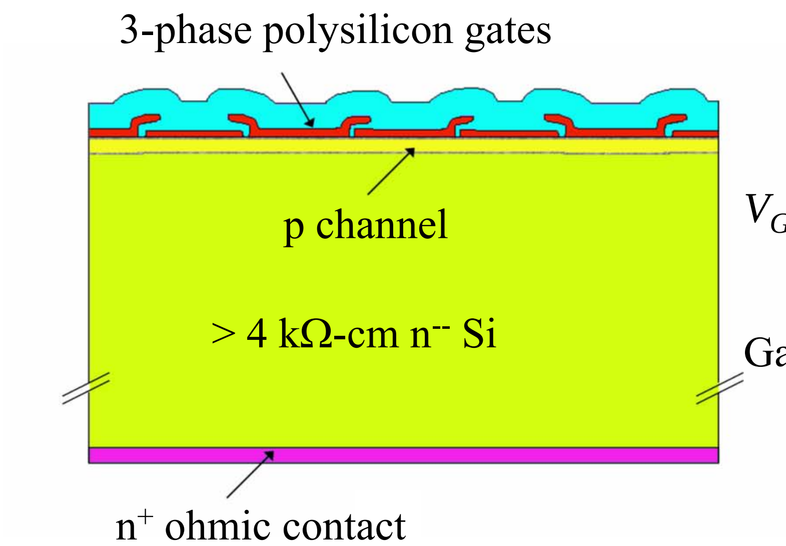


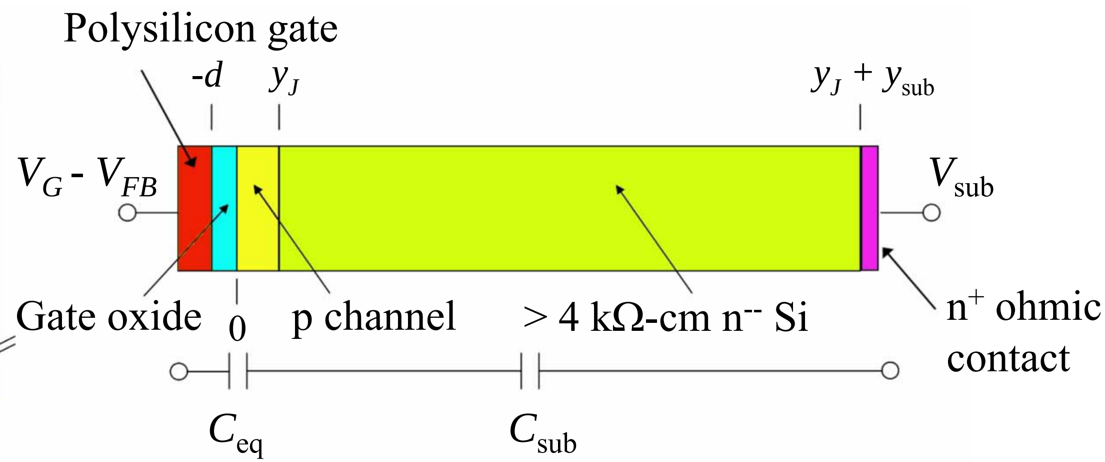
MEDICI 2-D simulation

The value of the CCD potential minimum, where holes are collected, is not a strong function of the substrate bias voltage, and as a result operation over a wide range of substrate bias voltages is possible

High-voltage considerations: Channel

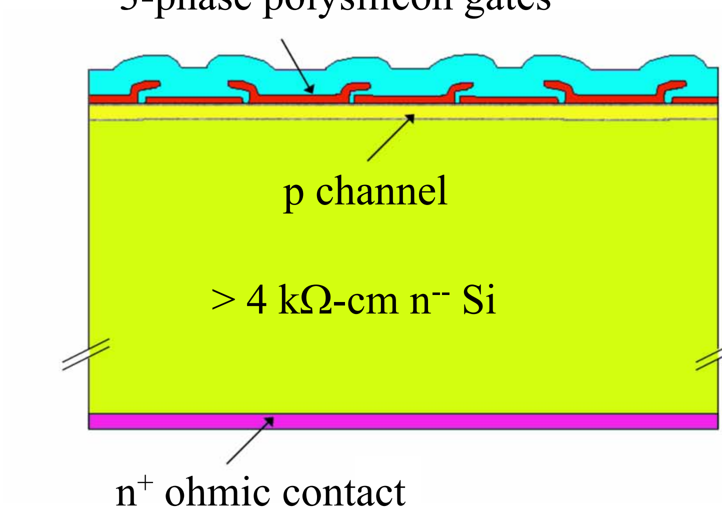


a) CCD cross section



b) Simplified cross section for 1D Poisson solution

High-voltage considerations: Channel



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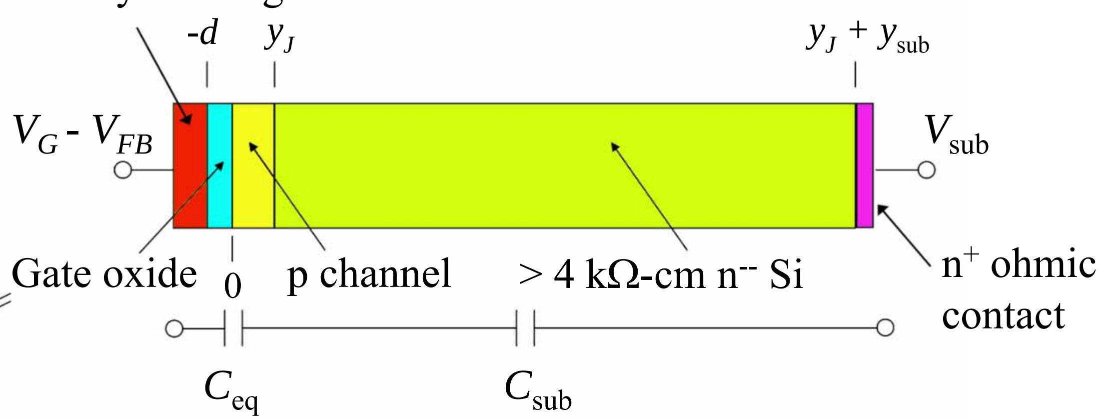


b) Simplified cross section for 1D Poisson solution

Solution to 1-D Poisson equation (depletion approximation, IEEE Trans. Elec. Dev., **50**, 225, 2003):

$$V(y_J) = V_J \approx V_G - V_{FB} - \frac{qN_A}{2\varepsilon_{Si}} y_J^{\,2} \left(1 + \frac{2\varepsilon_{Si} d}{\varepsilon_{SiO_2} y_J}\right) \quad \text{independent of } V_{\mathrm{SUB}}$$

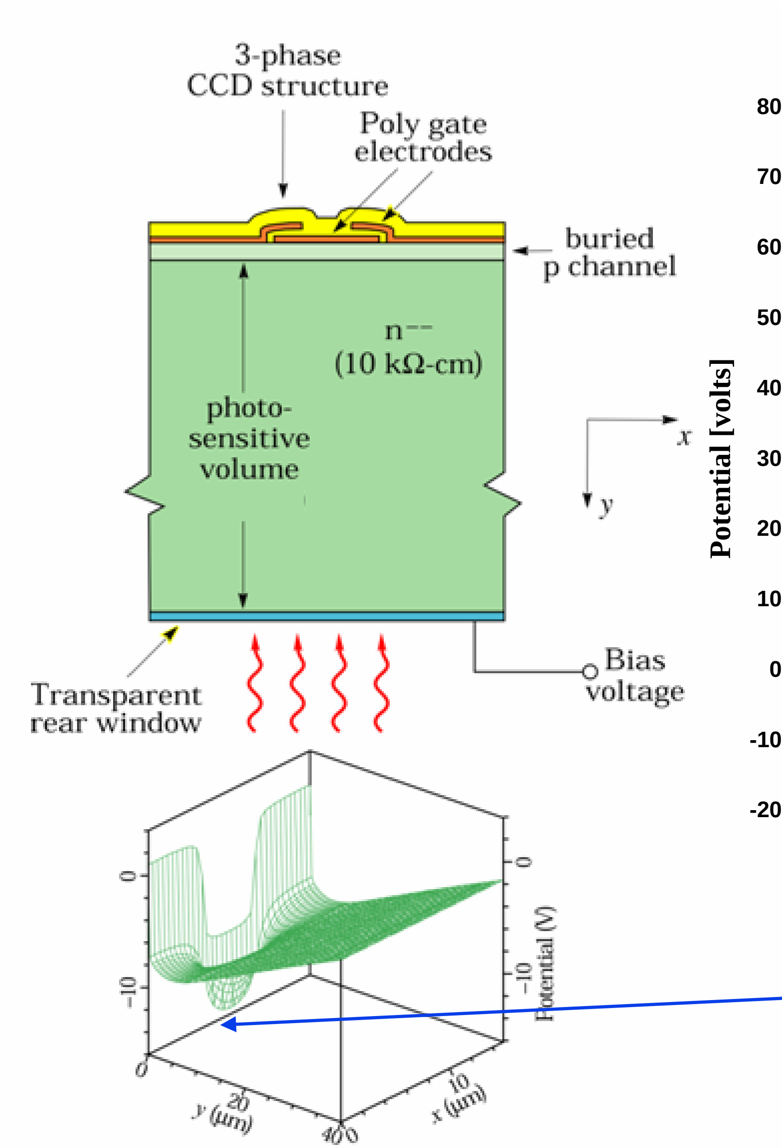
$$\text{Valid for } N_{D,sub} \ll N_A \text{ and } y_{SUB} \gg y_J + \left(\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}\right) d$$

Substrate doping

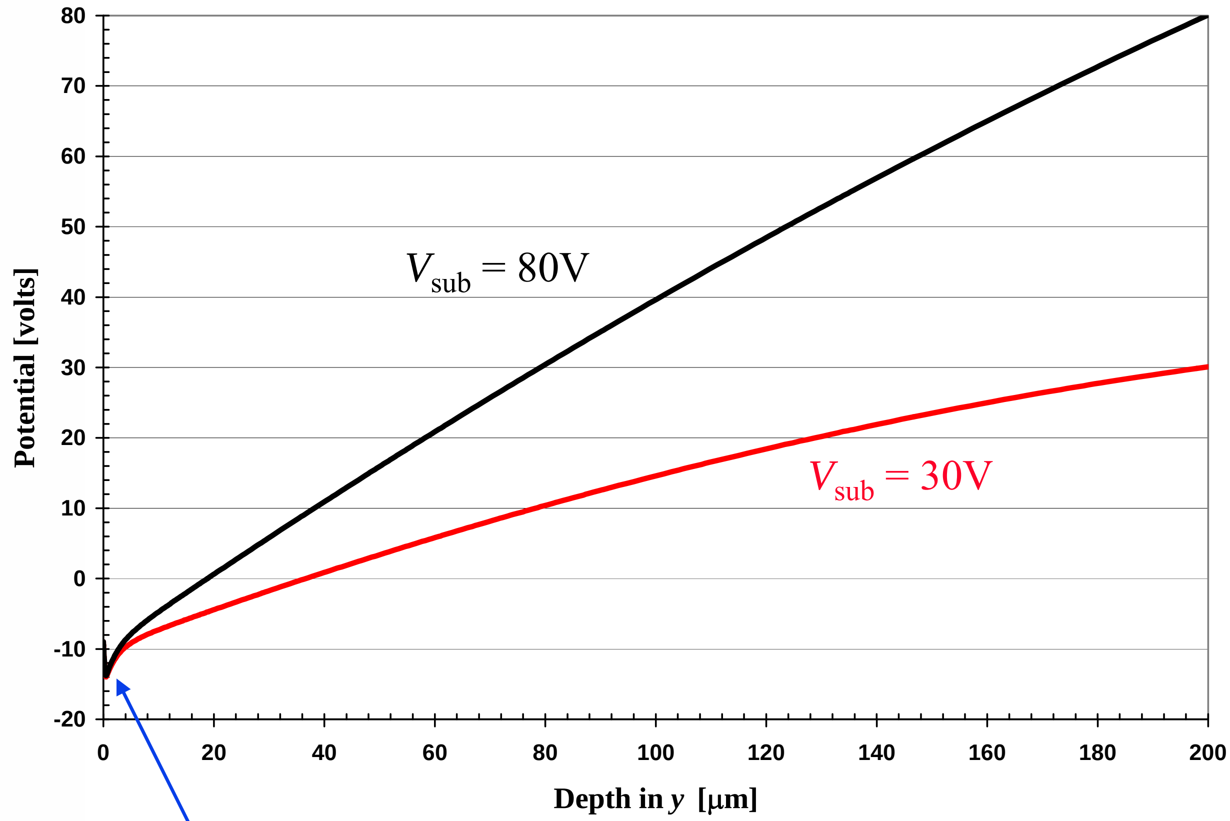
Channel doping

Capacitor voltage divider

High-voltage considerations: Channel



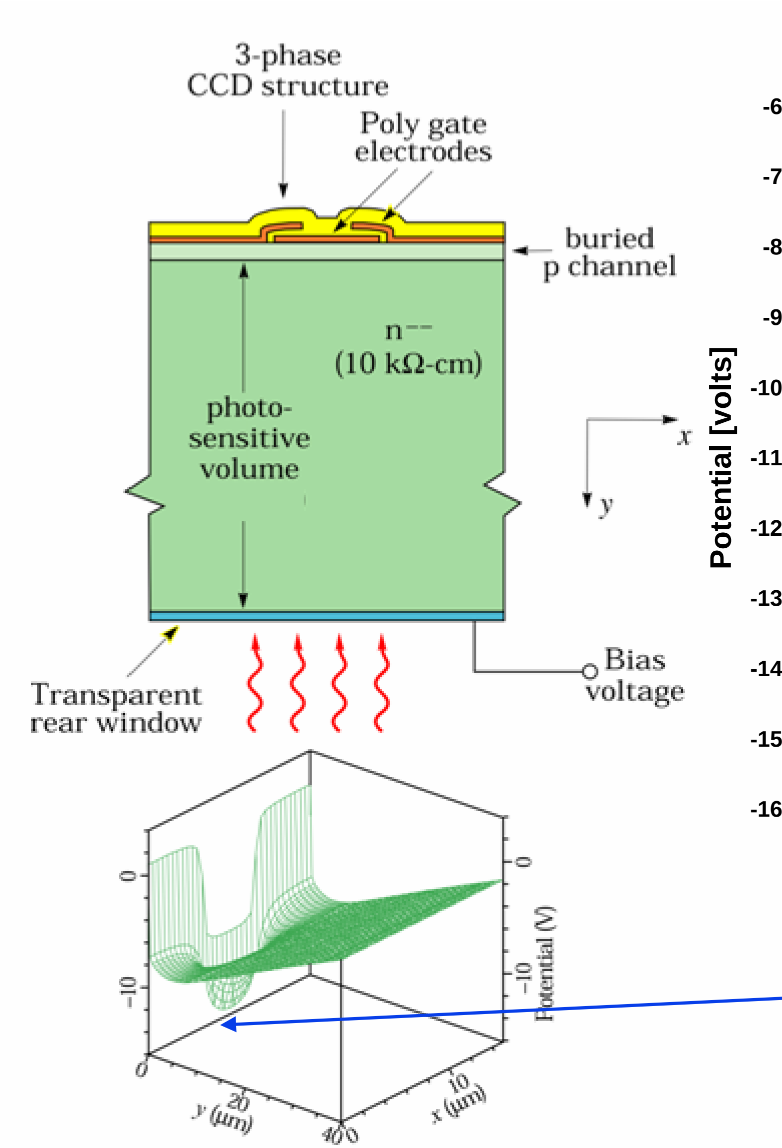
MEDICI 2-D simulation



Potential minimum
(collecting phase)

MEDICI simulations

High-voltage considerations: Channel



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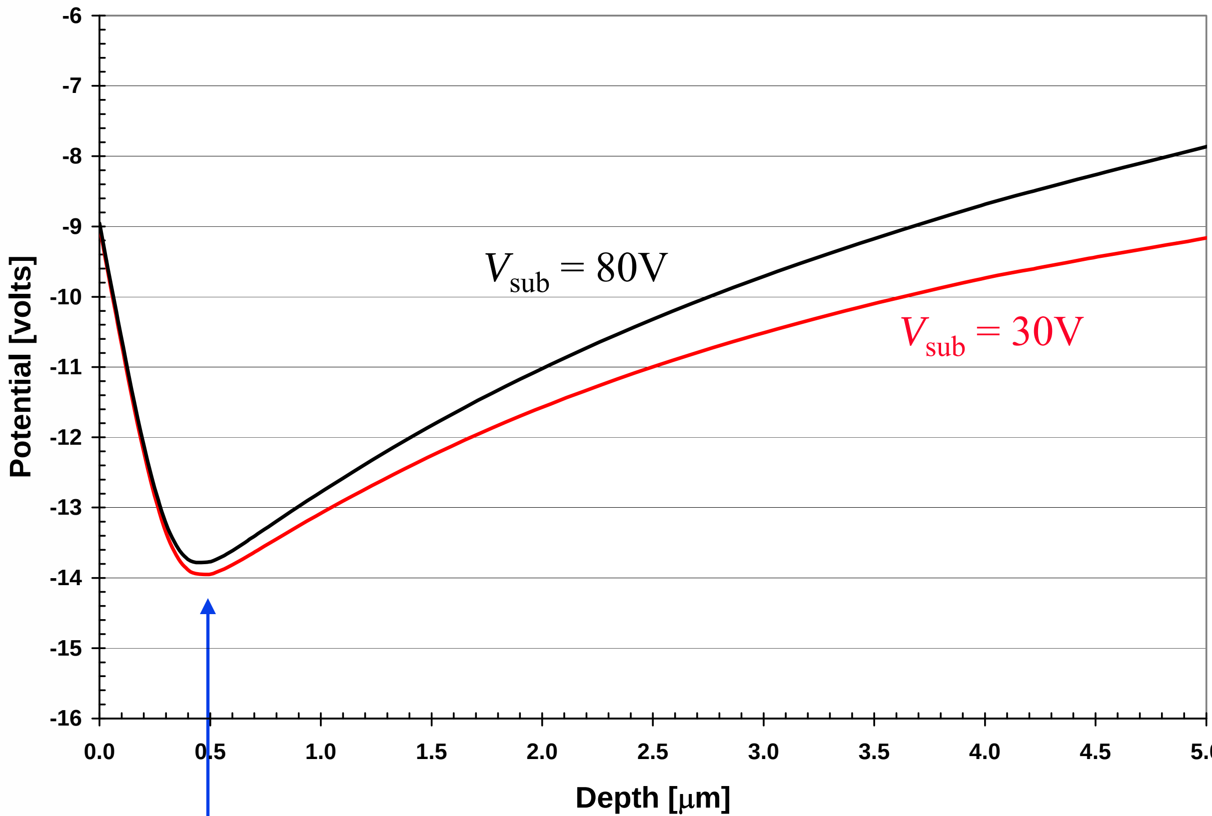

Potential minimum
(collecting phase)

MEDICI simulations

CCD development at LBNL

- The CCDs developed at LBNL for astronomy and astrophysics are operated at cryogenic temperatures for ultra-low dark current (-100 – -140°C typical), and are read out slowly for low noise (50–100 kpixels/sec typical)

- The CCD developed at LBNL is a p-channel CCD
  - —Information is carried by holes, not electrons
  - —The choice of p-channel CCDs was due to our p-i-n diode experience with n-type, high-resistivity silicon substrates
    - Easier to achieve low dark current when compared to p-type silicon
  - —An unexpected bonus of the choice of p-channel is enhanced resistance to the effects of space protons in p-channel CCDs
    - Charge transfer efficiency degradation much less in p-channel

Outline

- Fully depleted CCD physics and performance
  - Quantum efficiency and fringing
    - The 200-250 µm thickness gives good near-infrared response
    - Fringing due to multiply reflected light is reduced
    - The blue response is enhanced with a thin, backside n^+ layer
  - Spatial resolution
  - Transistors fabricated on high-resistivity silicon
  - Backside defects
- CCD fabrication
  - Hybrid fabrication model
  - Dark Energy Survey project
  - 4k x 4k (15 µm pixel) development
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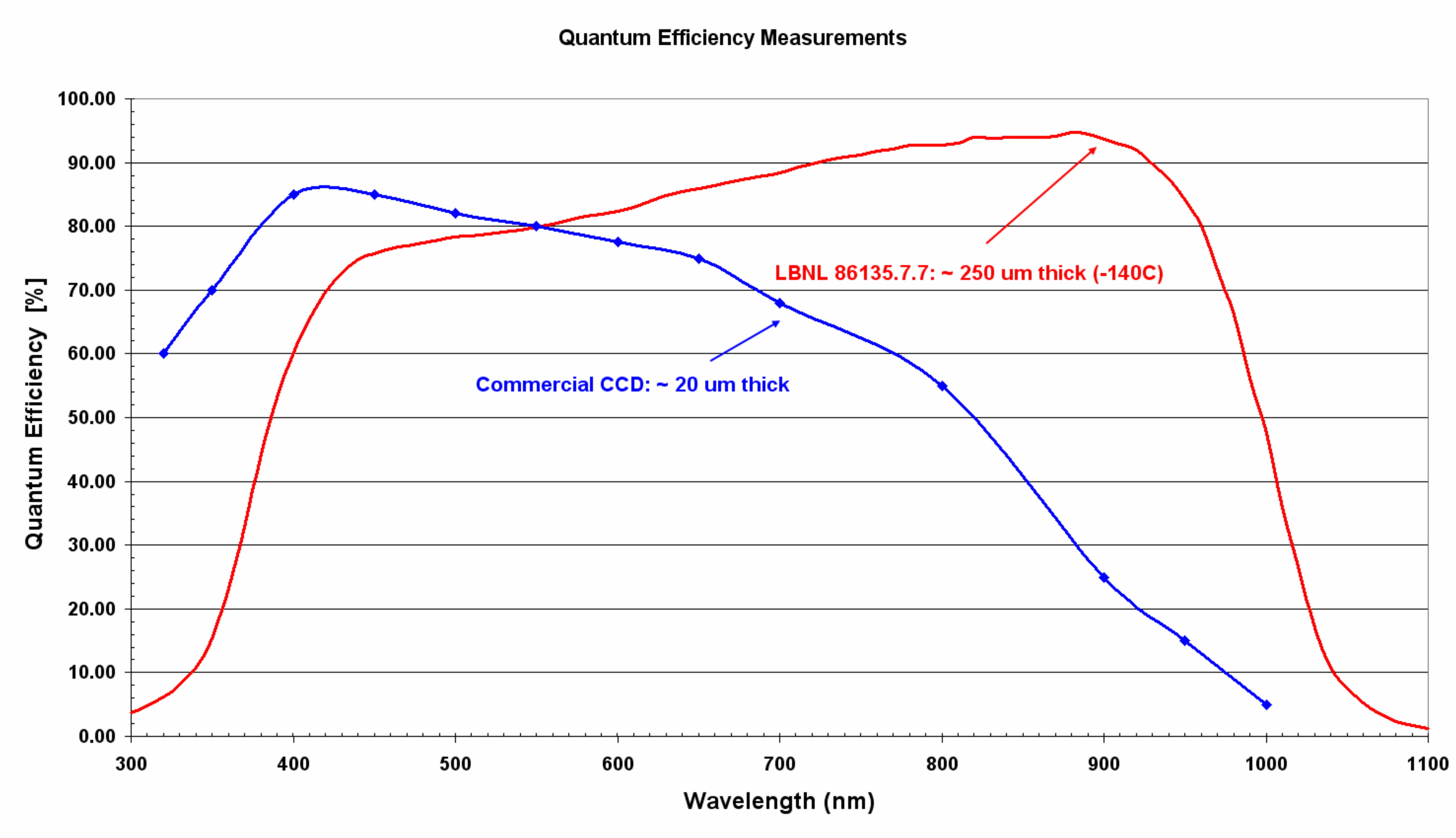
Quantum efficiency

A key advantage of thick CCDs (~200–300 μm thick) compared to thinned scientific devices (~10–20 μm thick) is improved near infrared response and reduced fringing



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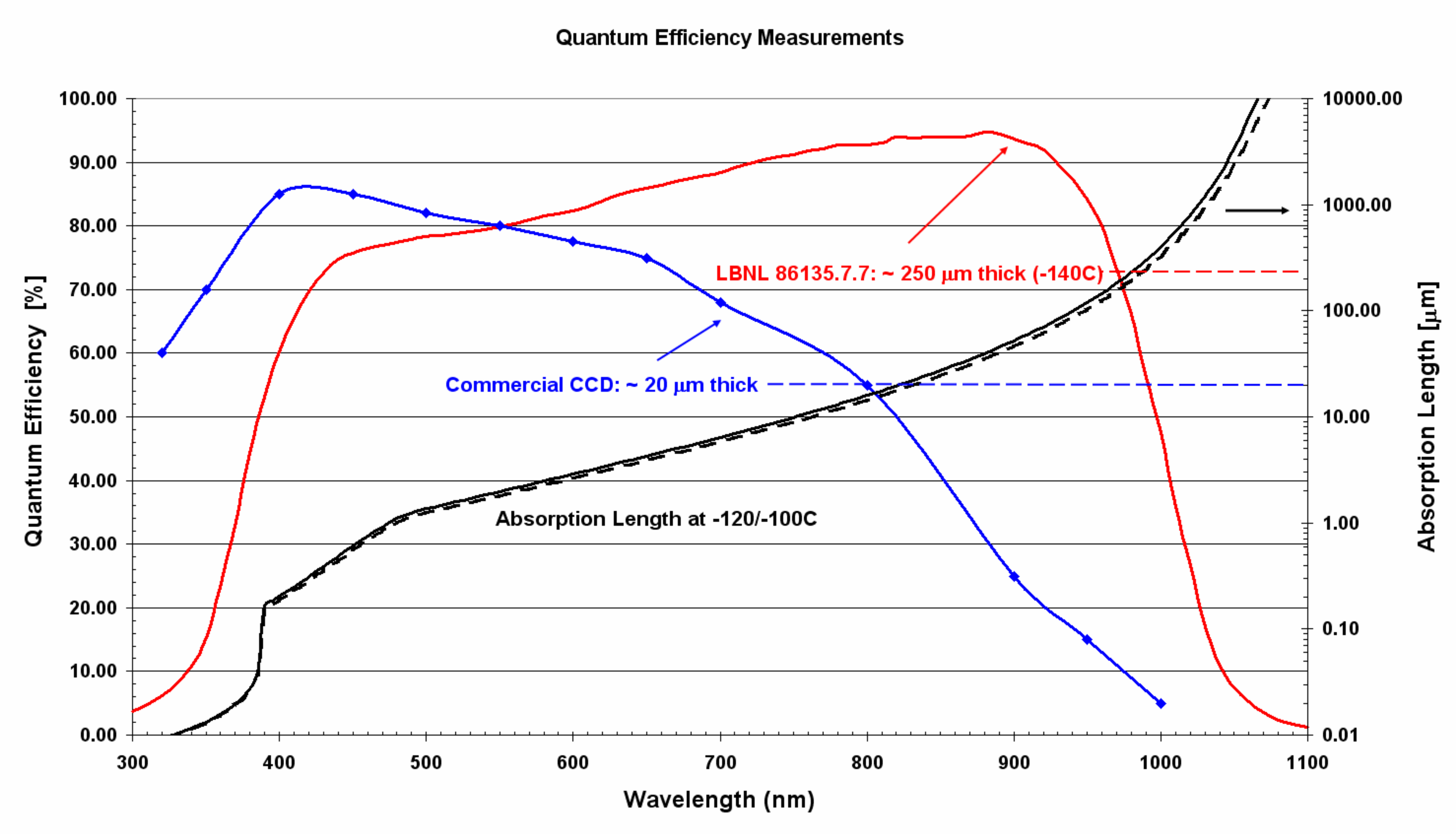
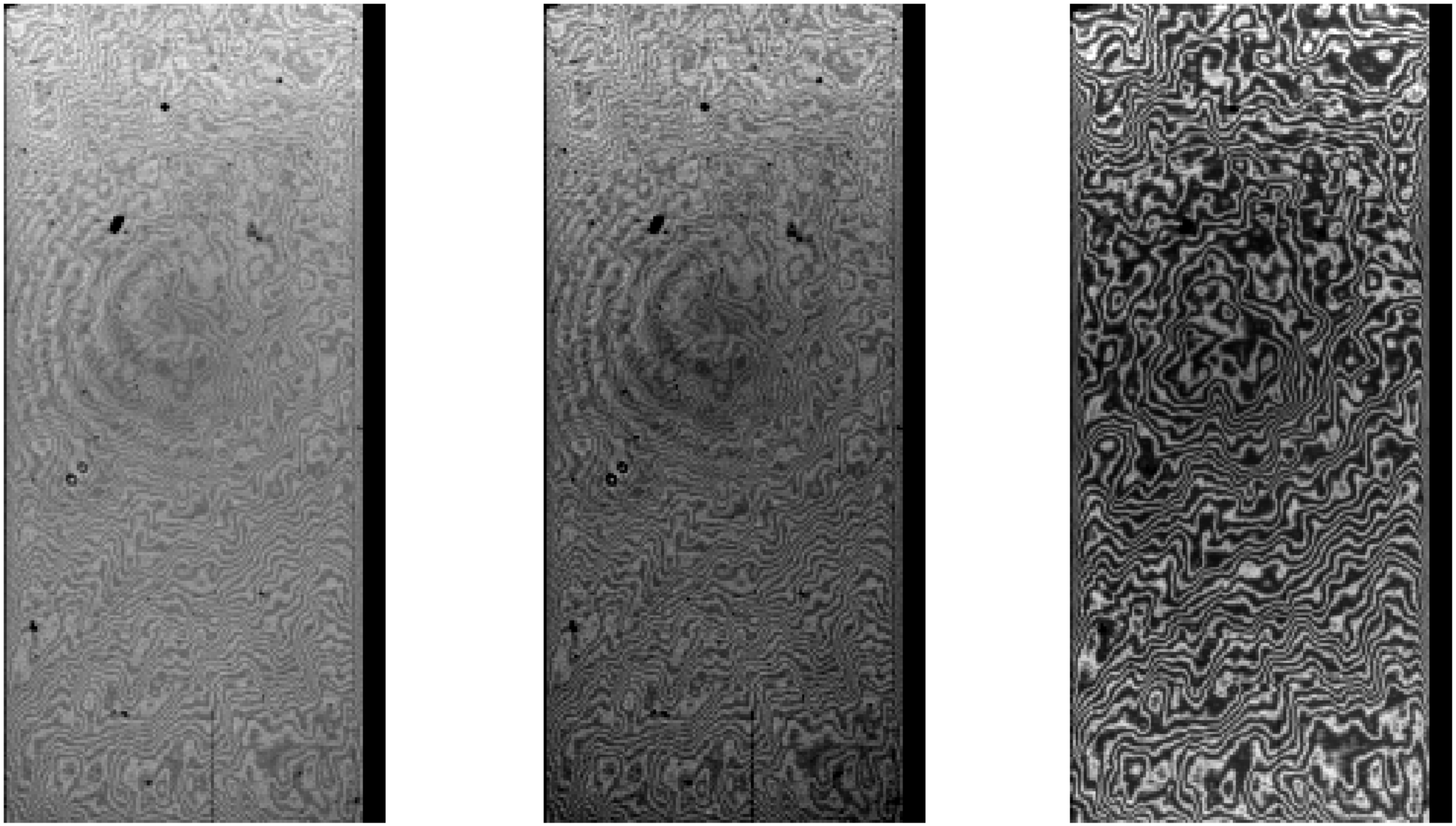


Fringing

Fringing due to multiply-reflected light (uniform illumination, 10–20 μm thick CCD)

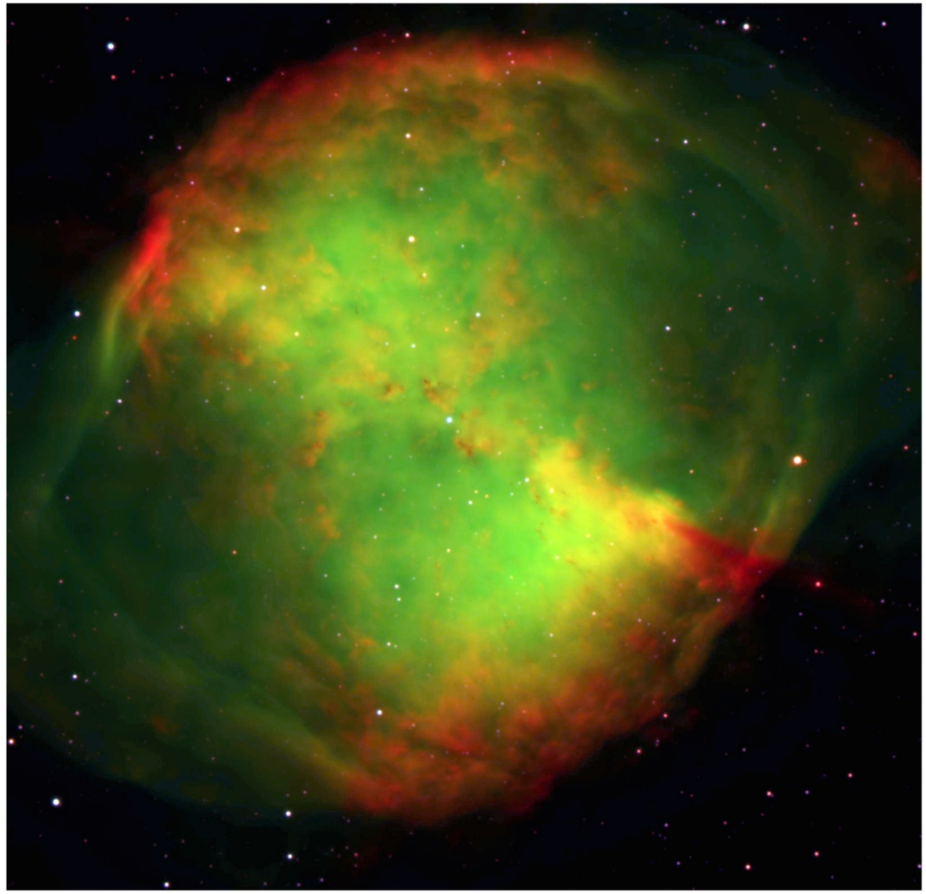


λ = 800 nm 900 nm 1 μm

Measurements courtesy of R. Stover, M. Wei of Lick Observatory

Near IR vs Visible image (Dumbbell nebula)

ESO image at visible wavelengths: 429/501/656 nm



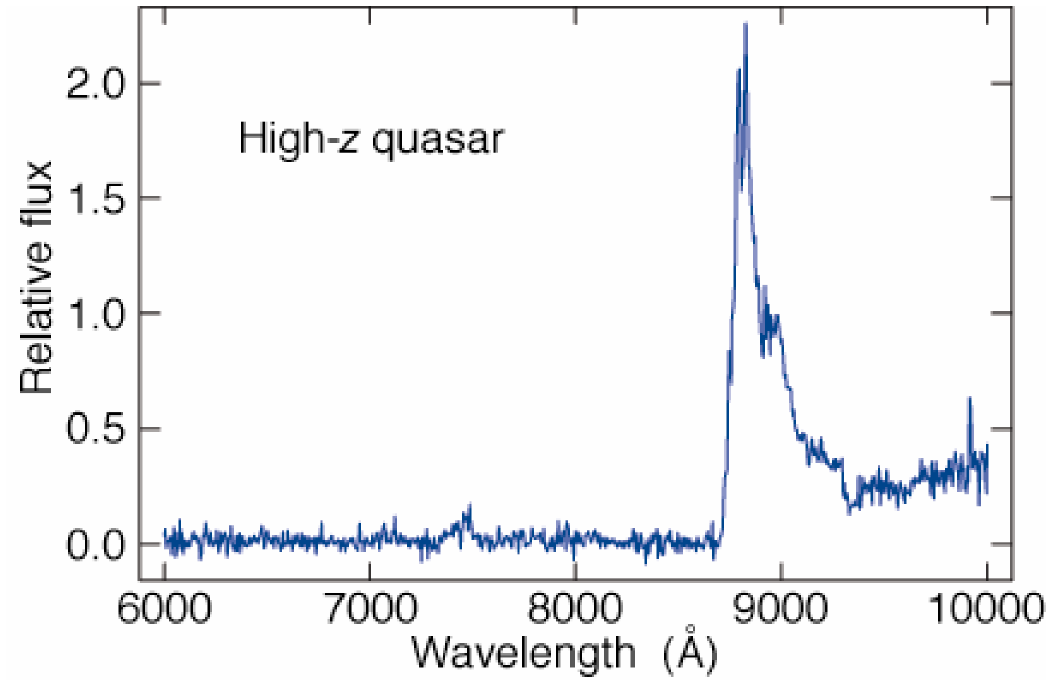
LBNL 2k x 4k CCD: Blue: H-α at 656 nm
Green: SIII at 955 nm Red: 1.02 μm

Planetary Nebula NGC 6853 (M 27) - VLT UT1+FORS1

ESO PR Photo 38a/98 (7 October 1998)

Near infrared imaging and spectroscopy

LNBL 1980 x 800 CCD: z > 6 Quasar spectrum
NOAO Multi-aperture Red Spectograph



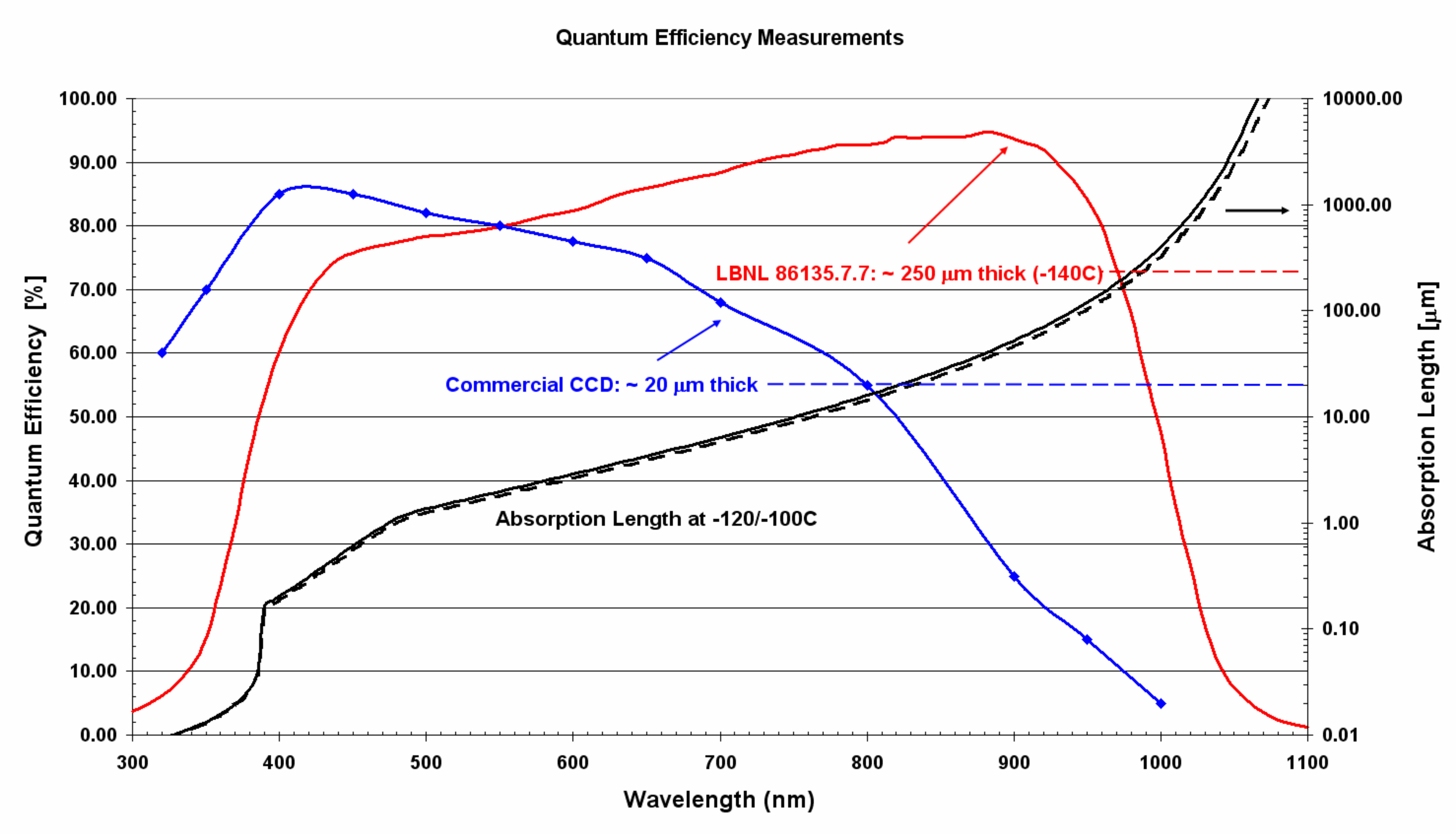
Data courtesy of Xiaohui Fan, University of Arizona Astronomy Department and the Sloan Digital Sky Survey, and Arjun Dey of the National Optical Astronomy Observatory

LBNL 2k x 4k CCD: Blue: H-α at 656 nm
Green: SIII at 955 nm Red: 1.02 μm

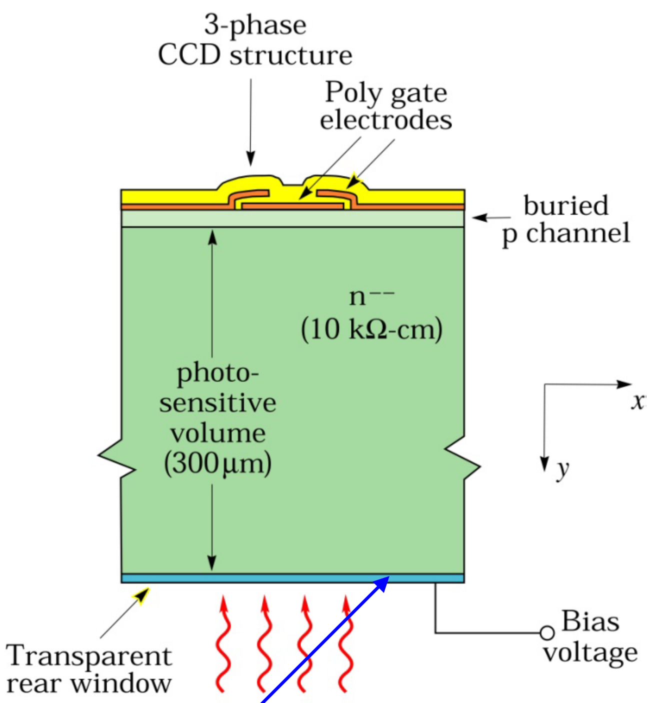
Quantum efficiency

At blue wavelengths the absorption length is very small, e.g. ~ 0.1 μm at 400 nm

Requires a thin entrance window for high quantum efficiency

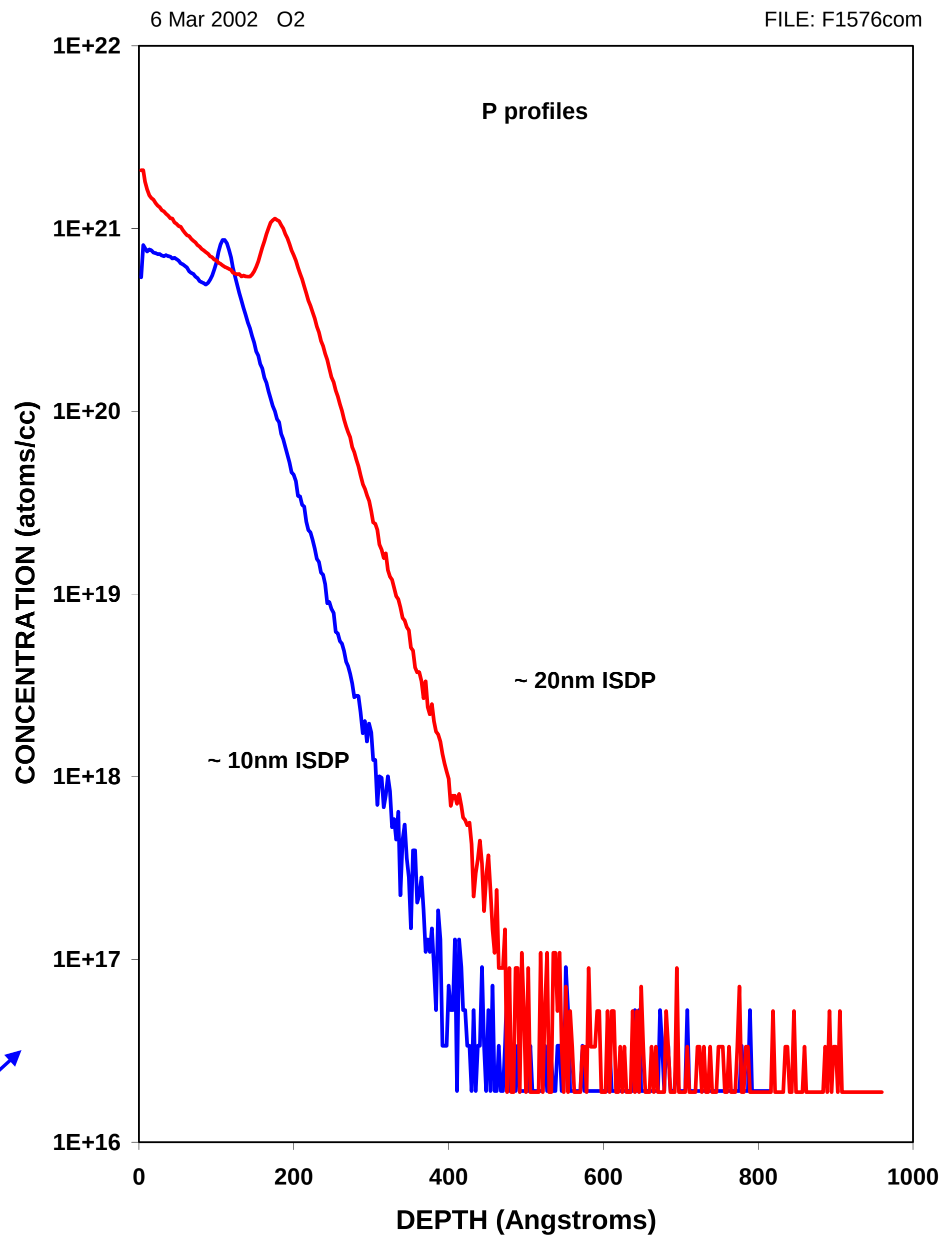


Thin backside n$^+$ ohmic contact development



Thin backside n$^+$ contact for good blue response formed by in-situ doped polysilicon (ISDP) deposition

SIMS phosphorus depth profile



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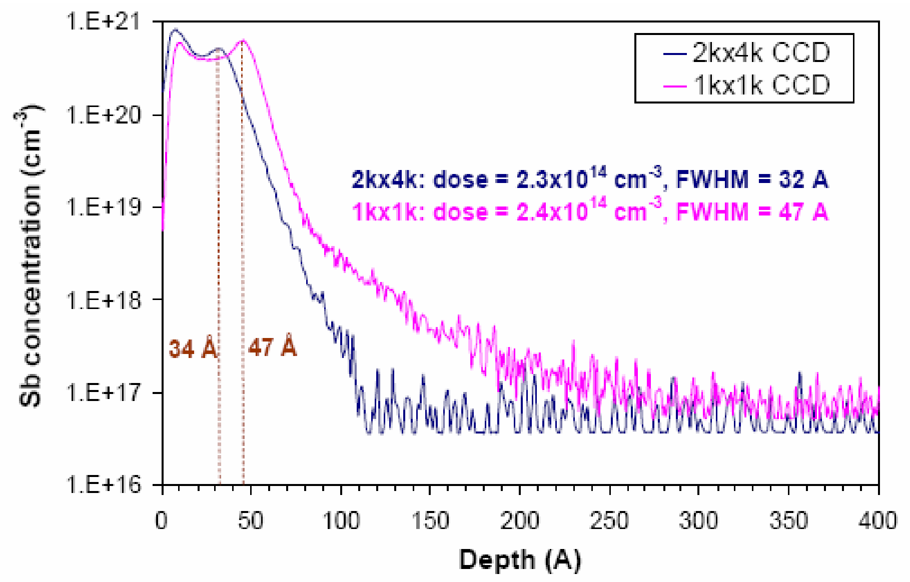
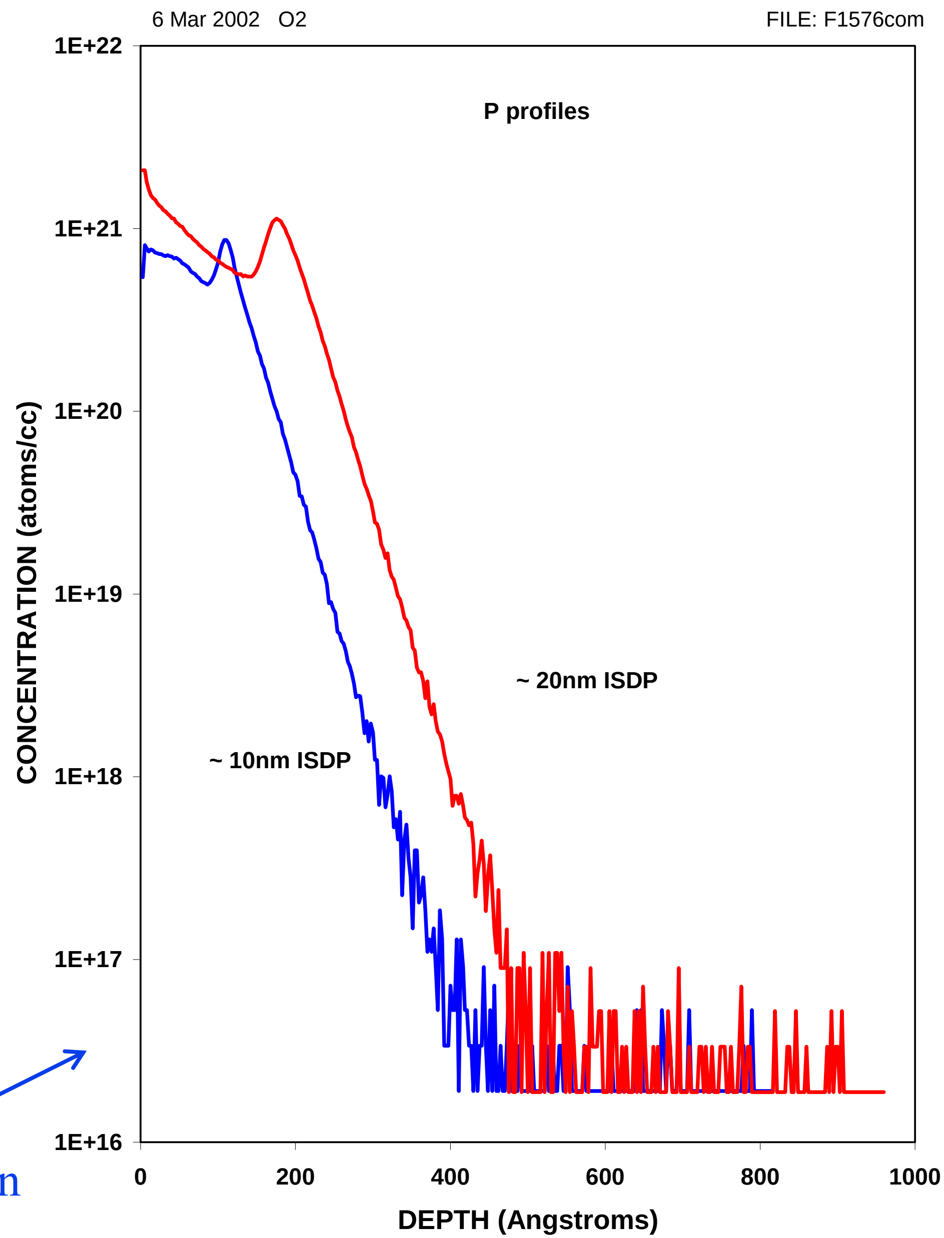


Fig. 1. Antimony concentration versus depth from the back surface of 1 k × 1 k and 2 k × 4 k CCDs obtained by SIMS (Charles Evans and Associates). The broader peak for the 1 k × 1 k CCD is due to a thicker silicon cap layer.

JPL MBE backside layer

J. Blacksberg *et al*, IEEE Trans. Elec. Dev., 55, 3402, 2008



LBNL in-situ doped polysilicon

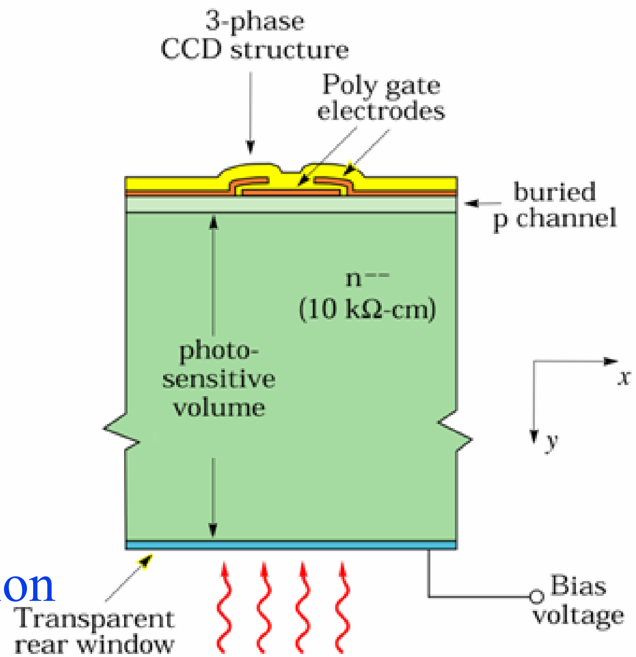
Outline

- Fully depleted CCD physics and performance
  - Quantum efficiency and fringing
  - **Spatial resolution**

In thick, fully depleted CCDs the photogenerated holes must travel relatively large distances to the collection wells

The fully depleted substrate provides a drift electric field to reduce the transverse diffusion of carriers that results in degradation of spatial resolution

Thinned CCDs often have an undepleted, i.e field-free region that dominates the spatial resolution



PSF for field-free layer

One can show that the rms point spread function for carrier diffusion in a region without an electric field is equal to the thickness of the field-free layer

Start with the Crowell-Labuda modulation-transfer function expression derived for back-illuminated diode arrays used in the Bell Labs “Picturephone®”

M. Crowell and E. Labuda, “The silicon diode array camera tube,” *Bell. Syst. Tech. J.*, **48**, 1481, 1969.

PSF for field-free layer

The Silicon Diode Array Camera Tube

By MERTON H. CROWELL and EDWARD F. LABUDA

(Manuscript received November 26, 1968)

A new electronic camera tube has been developed for Picturephone® visual telephone applications; with minor modifications it should also be suitable for conventional television systems. The image sensing target of the new camera consists of a planar array of reversed biased silicon photodiodes which are accessed by a low energy scanning electron beam similar to that used in a conventional vidicon. This paper presents a description of the operating principles and an analysis of the sensitivity and resolution capabilities of the new silicon diode array camera tube.

We also give the detailed experimental results obtained with the tubes. The gamma of a silicon diode array camera tube is unity and its spectral response is virtually uniform over the wavelength range from 0.45 to 0.90 micron with an effective quantum yield greater than 50 percent. For a 13.4 millimeter square target the silicon diode array camera tube's sensitivity is 20 μamp foot-candles of faceplate illumination with normal incandescent illumination or 1.3 μamp per foot-candle with fluorescent illumination; with a center-to-center diode spacing of 15 micron it's modulation transfer function is greater than 60 percent for a spatial frequency of 14 cycles per millimeter. Typical dark currents for a 13.4 millimeter square target are in the range of 5 to 50 nanoamperes.

PSF for field-free layer

1484 THE BELL SYSTEM TECHNICAL JOURNAL, MAY–JUNE 1(

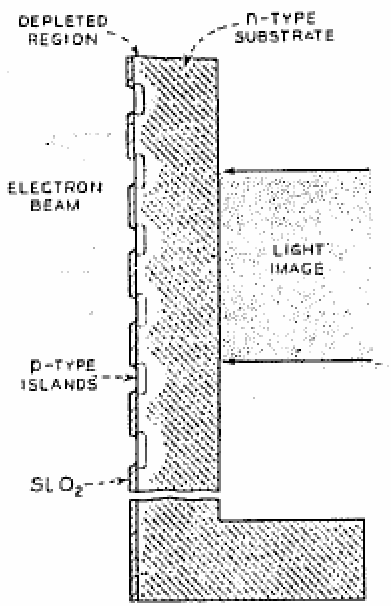


Fig. 2 — Schematic of a diode array target. To obtain a self-supporti ture, the perimeter of the wafer is left much thicker than the substra area of the diode array.

ELECTRONIC CAMERA TUBE 1487

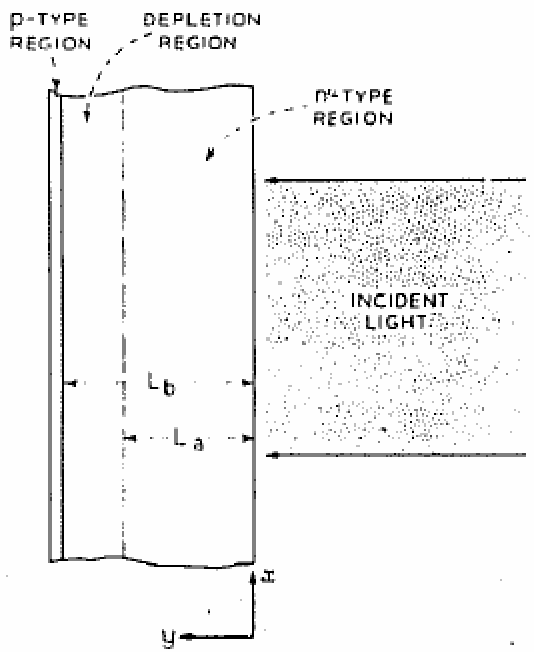


Fig. 3 — Schematic of the simplified model used to estimate the light sensitivity and resolving ability of a diode array target.

Crowell and Labuda back-illuminated photodiode array for the Picturephone®

Not fully depleted

PSF for field-free layer

Crowell and Labuda solved the continuity equation for the back-illuminated photodiode array with a sinusoidally varying light input to get the MTF

Neglecting recombination and assuming the light is absorbed in a distance small compared to the field-free region thickness results in an approximate MTF given by

$$MTF_{ff} \approx \frac{1}{\cosh(kL_{ff})}$$

Where $k = 2\pi$/spatial period of the incident light

This expression was apparently well known to developers of back-illuminated infrared detectors

PSF for field-free layer

The point-spread function is the inverse Fourier transform of the modulation-transfer function, i.e.

$$PSF_{ff} = \frac{1}{2L_{ff} \cosh\left[\frac{\pi x}{2L_{ff}}\right]}$$

The rms width of the PSF from the Moment Theorem is

$$\sigma = L_{ff}$$

Key point: Partially depleted, back-illuminated imagers can have a spatial resolution that is dominated by the thickness of the field-free layer

Point Spread Function: Simplified Model

- Fully depleted CCD: Point spread function (PSF) is determined by the hole transit time in the electric field
- For carriers with the same arrival time at the CCD potential wells, the distribution is Gaussian

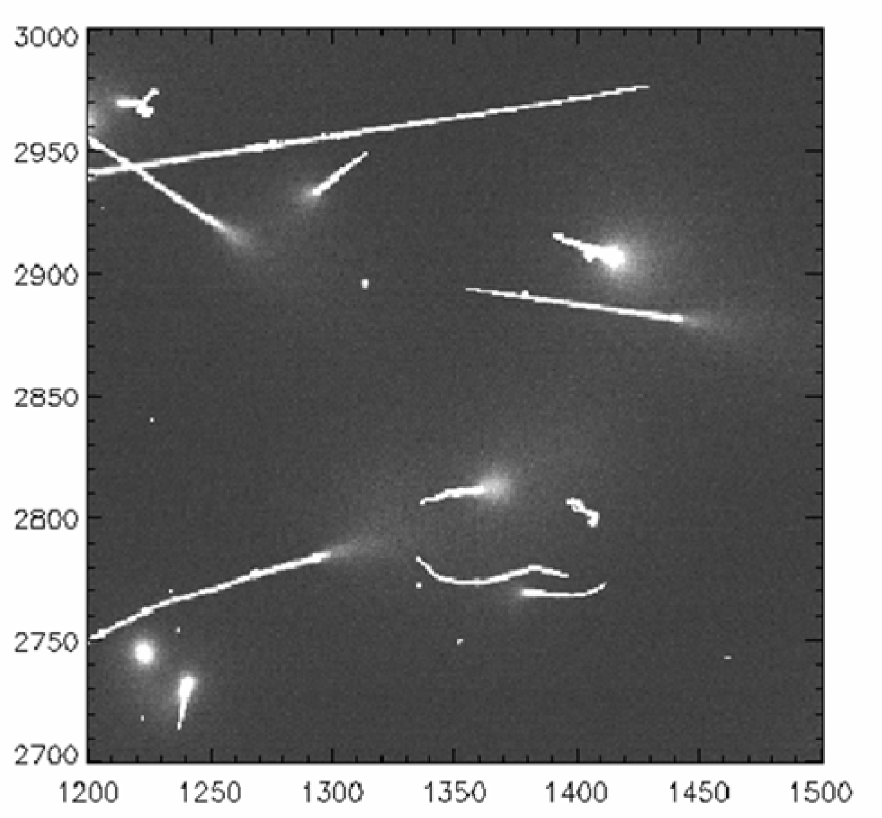
Constant field approximation (simplified model)

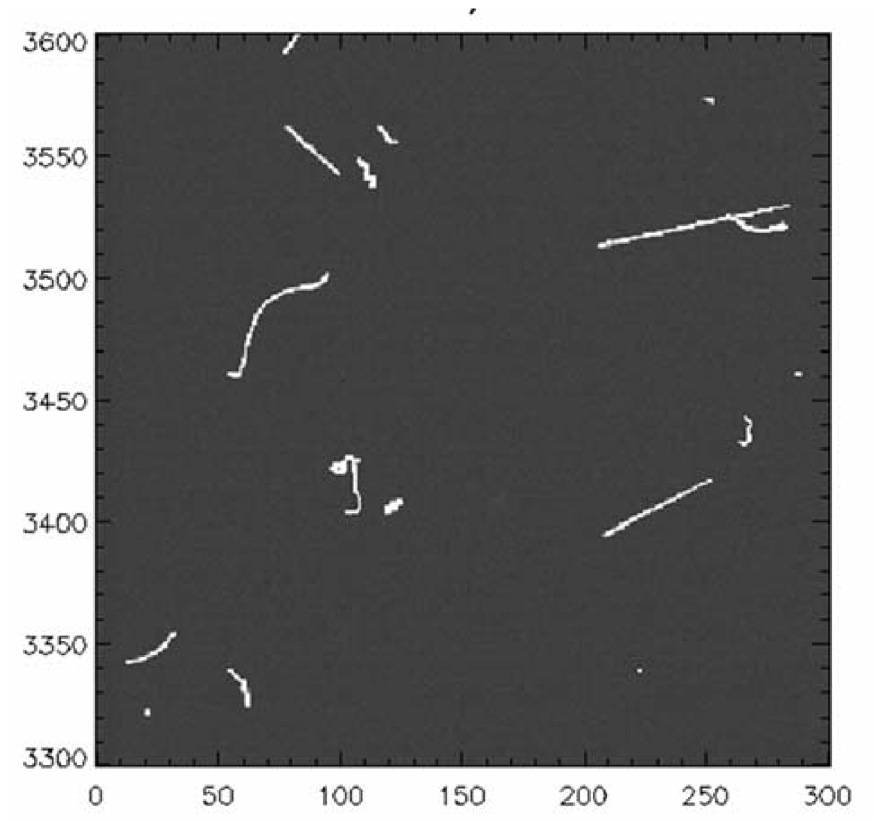
$$\sigma = \sqrt{2 D_p t_{tr}} \qquad t_{tr} = \frac{z_{sub}}{v} = \frac{z_{sub}}{\mu_p E} = \frac{z_{sub}^{\ 2}}{\mu_p (V_{sub} - V_J)}$$

$$D_p / \mu_p = kT / q \qquad \boxed{\sigma = z_{sub} \sqrt{\frac{kT}{q} \frac{2}{(V_{sub} - V_J)}}}$$

z_{sub}	~ Thickness of CCD
kT / q	Thermal voltage
$V_{sub} - V_J$	Voltage across drift region

Point Spread Function Issues



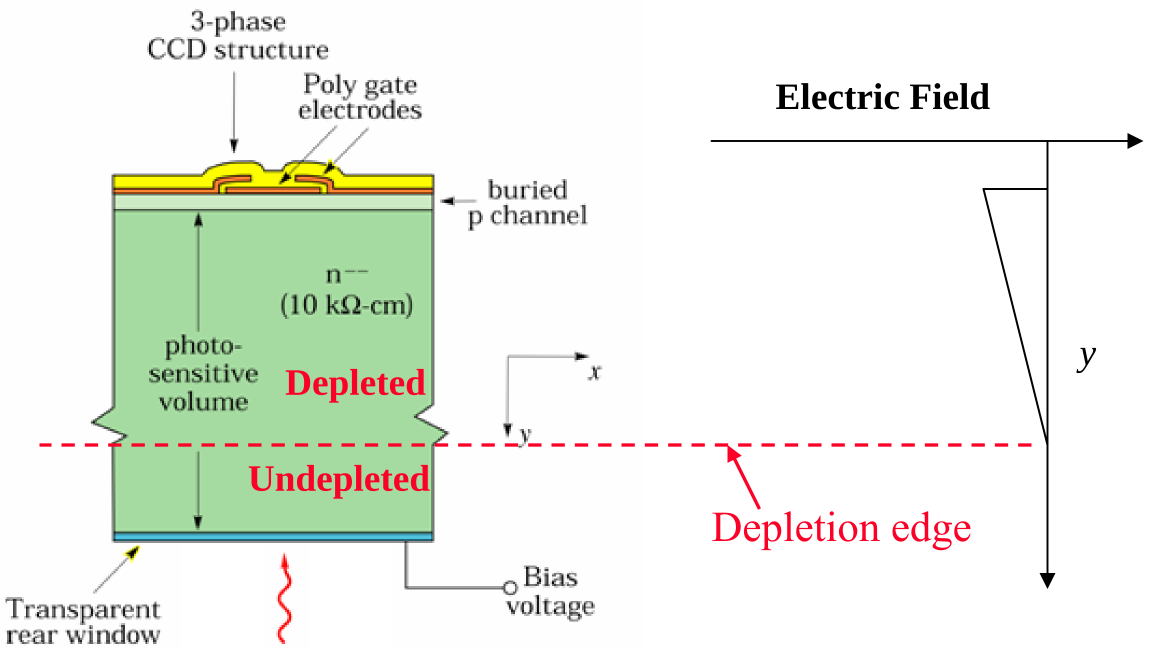


650 μm thick CCD
Not fully depleted at 100V

200 μm thick CCD
Fully depleted at 100V

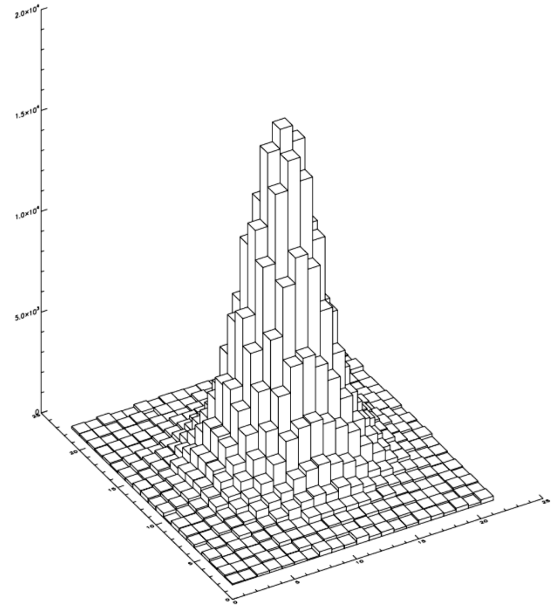
Long dark images (30 minute integrations) showing background radiation events from Compton electrons and cosmic rays

Spatial resolution: Effect of substrate voltage



Point source illumination

$V_{SUB} = 5V$



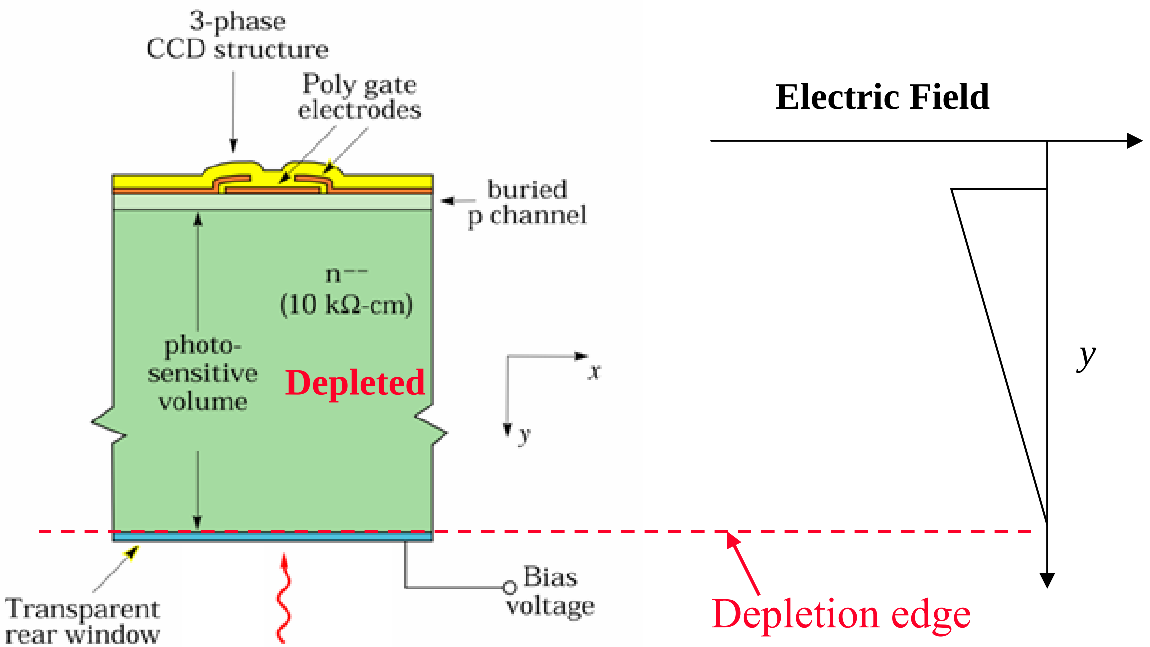
Measured charge distribution
Each square represents 1 pixel

At low substrate bias voltages the CCD is not fully depleted

The PSF is dominated by diffusion in the undepleted silicon

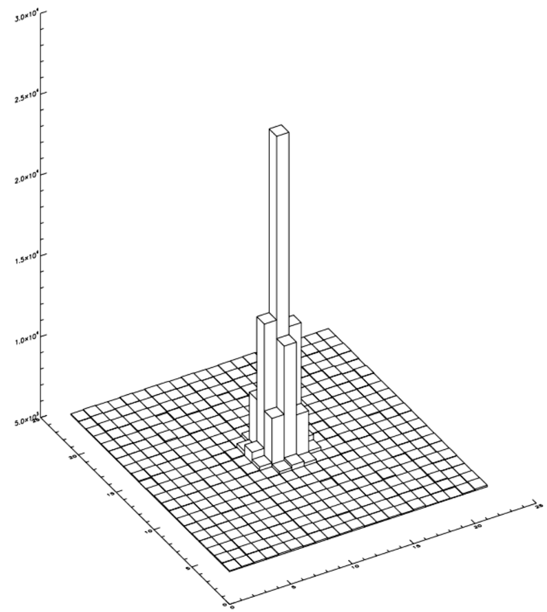
Can be shown that σ ~ the field-free region thickness

Spatial resolution: Effect of substrate voltage



Point source illumination

$V_{SUB} = 20V$



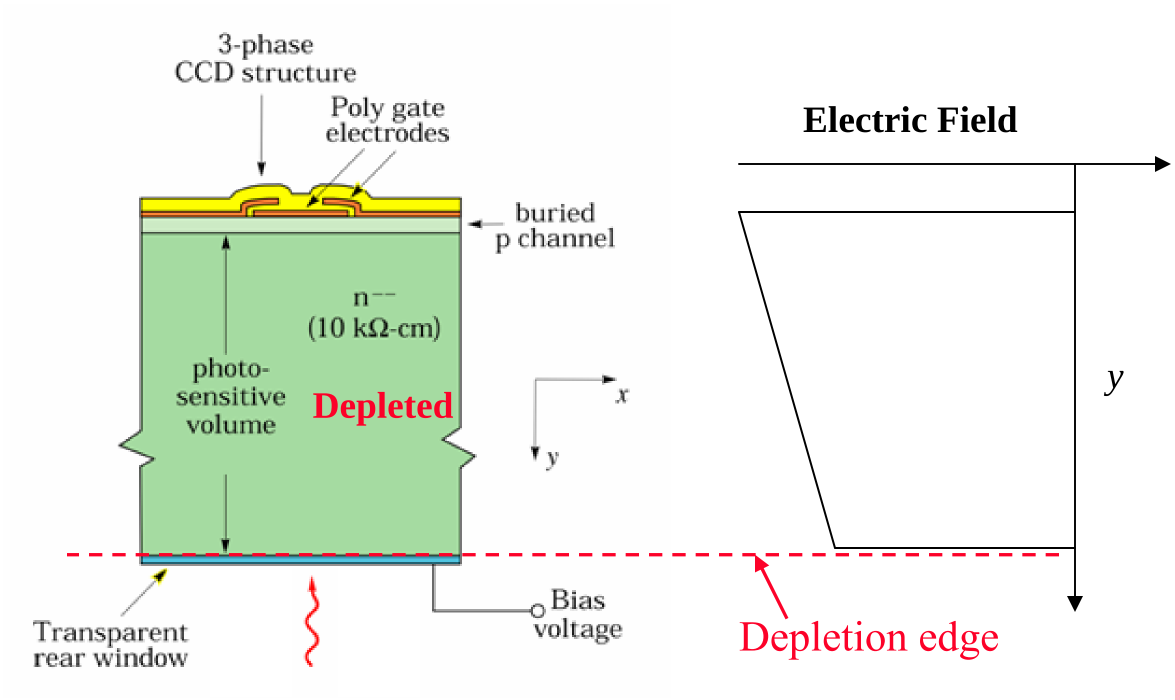
Measured charge distribution
Each square represents 1 pixel

At 20V the CCD corresponding to the data is just fully depleted

The PSF is limited by the transit time of the photogenerated holes

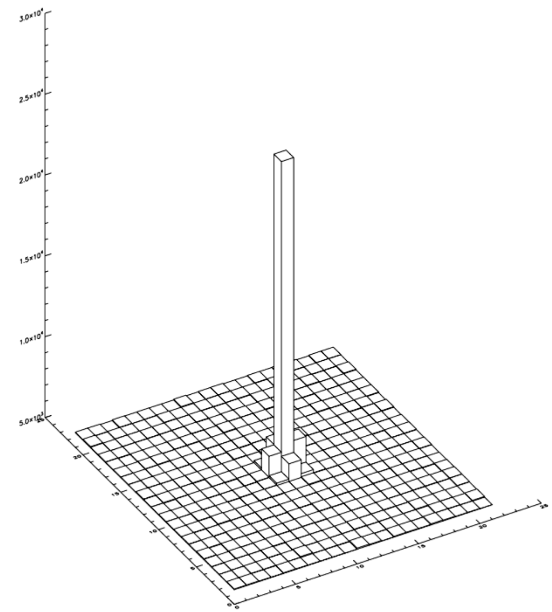
$$\sigma = \sqrt{2Dt_{tr}}$$

Spatial resolution: Effect of substrate voltage



Point source illumination

$V_{SUB} = 115V$

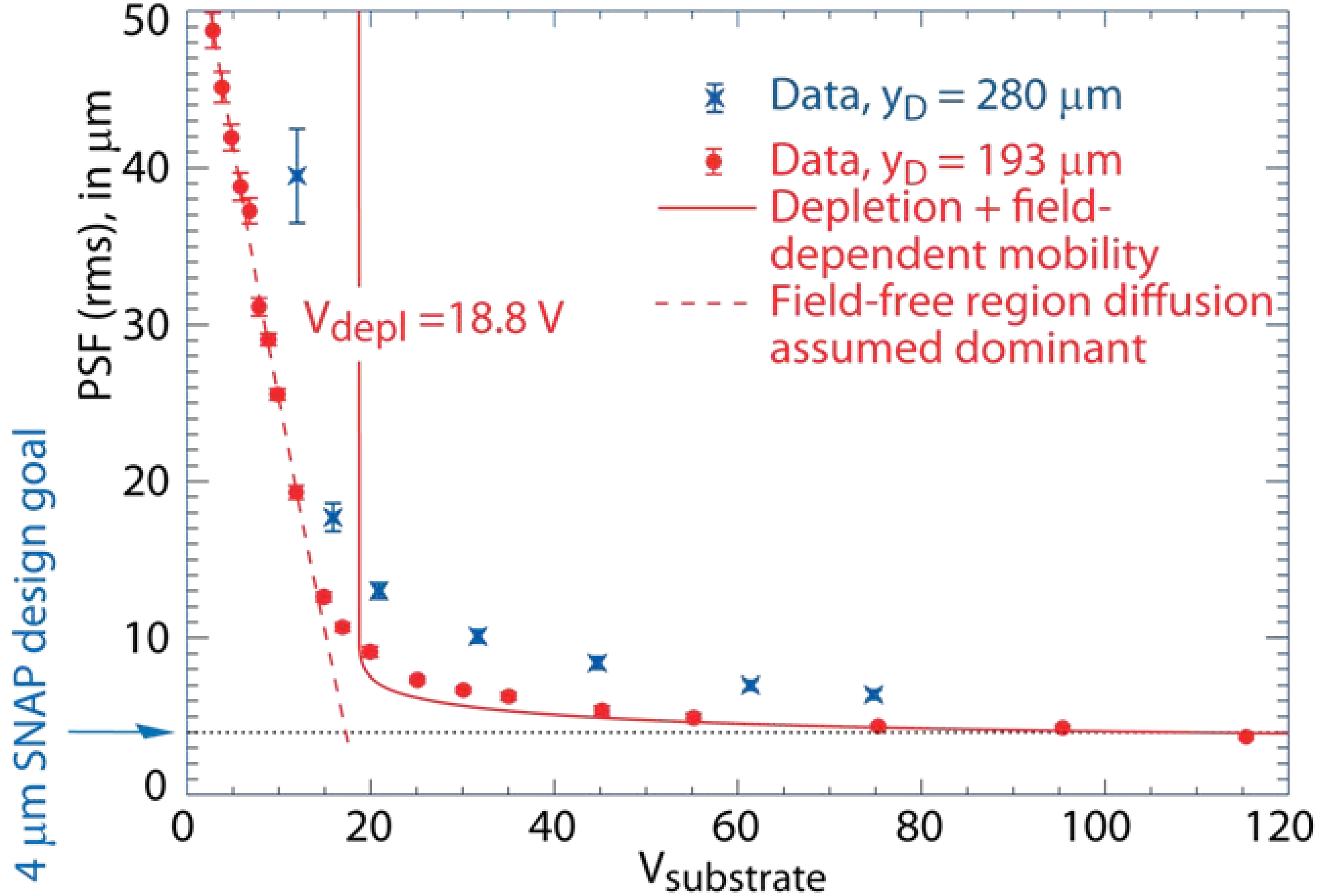


Measured charge distribution
Each square represents 1 pixel

The PSF continues to improve (but slowly) as V_{SUB} in increased

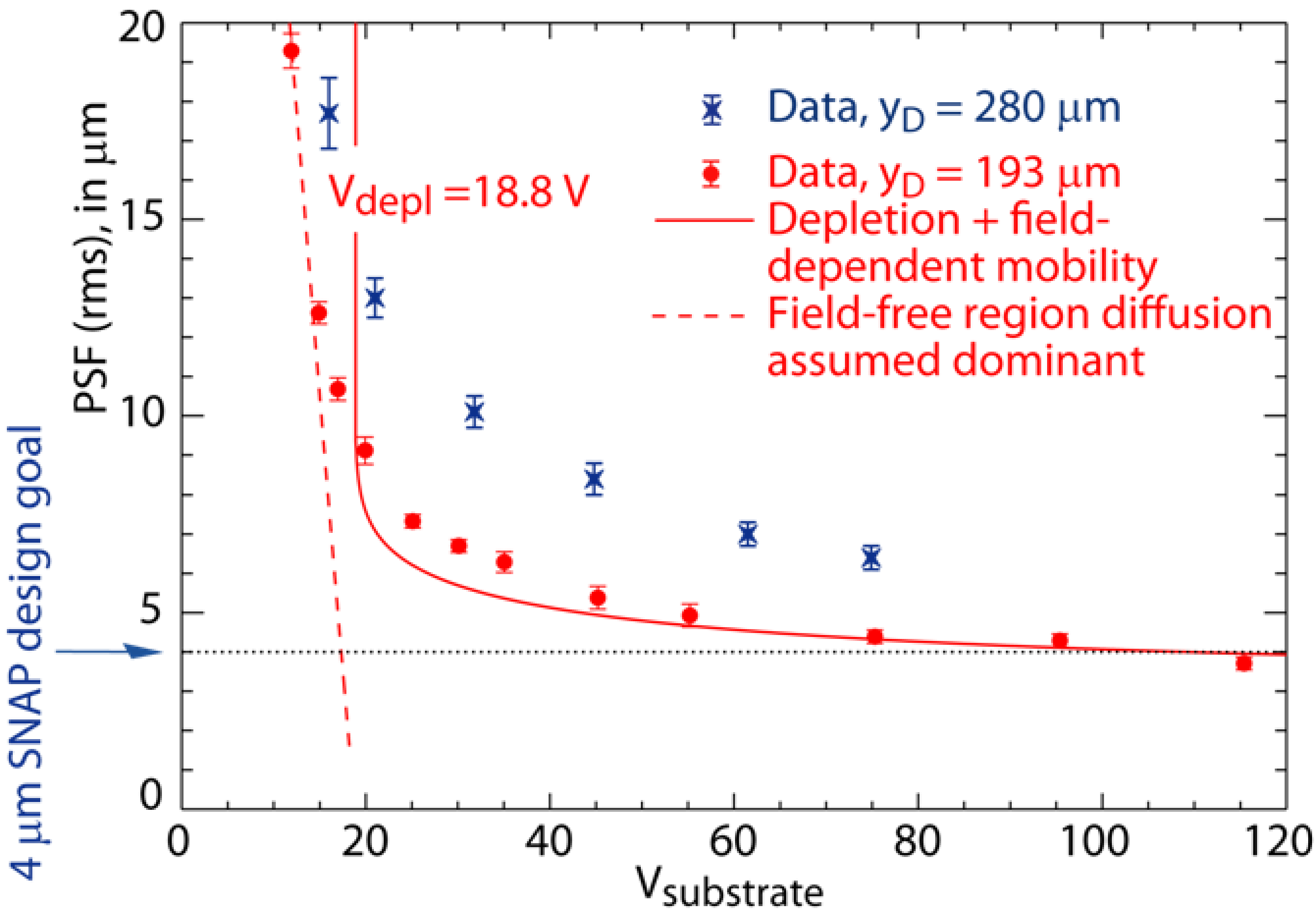
At V_{SUB}=115V the rms diffusion for this 200 μm thick,
10.5 μm pixel CCD is 3.7 ± 0.2 μm

PSF measurements on 200 and 280 μm thick CCDs



Need to include the electric field dependence of hole mobility for good fits at high voltage (J. Fairfield et al, IEEE Trans. Nucl. Sci., **53**, 3877, 2006)

PSF measurements on 200 and 280 μm thick CCDs



Need to include the electric field dependence of hole mobility for good fits at high voltage (J. Fairfield et al, IEEE Trans. Nucl. Sci., **53**, 3877, 2006)

Outline

- Fully depleted CCD physics and performance
  - — Quantum efficiency and fringing
  - — Spatial resolution
  - — Transistors fabricated on high-resistivity silicon
  - — Backside defects
- CCD fabrication
  - — Hybrid fabrication model
  - — Dark Energy Survey project
  - — 4k x 4k (15 µm pixel) development
- Summary

Transistors on high-resistivity silicon

- Vanstraelen *et al* of IMEC demonstrated the utility of the substrate bias voltage in suppressing punchthrough currents for p-channel transistors fabricated directly on high resistivity silicon
  - High energy physics applications
  - G. Vanstraelen, I. Debusschere, C. Claeys, and G. Declerck, *Nucl. Instrum. Meth. In Phys. Res. A*, **273**, 625, 1988

- Due to the extremely low substrate doping the body effect is quite small, resulting in small threshold voltage changes for large changes in V_{sub}

- Nonetheless, the channel length is limited by the punchthrough characteristics to about 2 – 3 μm

Transistors on high-resistivity silicon cont'

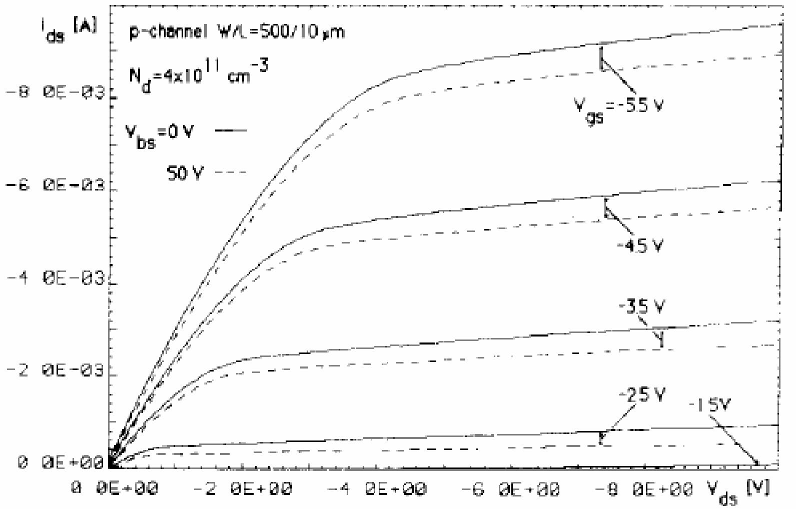


Fig. 9. $I_{ds}(V_{gs})-V_{ds}$ characteristics of the 10 μm device. Solid lines: $V_{bs} = 0$ V; dashed lines: $V_{bs} = 50$ V.

500/10 P-channel MOSFET (surface channel) 10 kΩ-cm substrate (n type)

G. Vanstraelen, I. Debusschere, C. Claeys, and G. Declerck, *Nucl. Instrum. Meth. In Phys. Res. A*, **273**, 625, 1988.

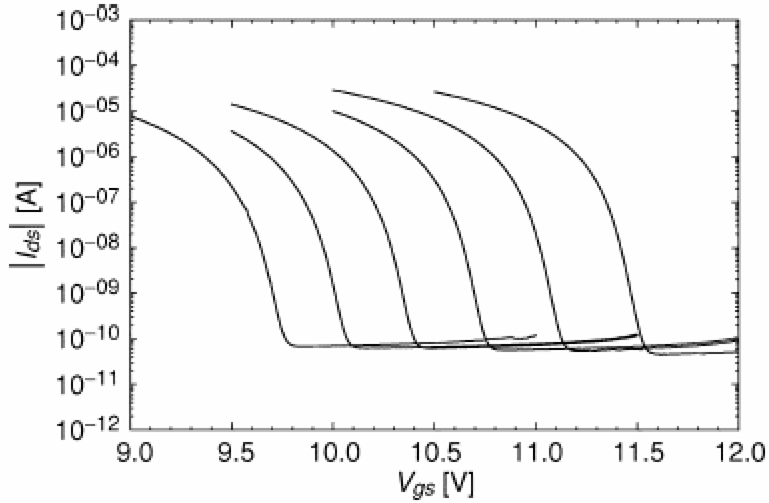


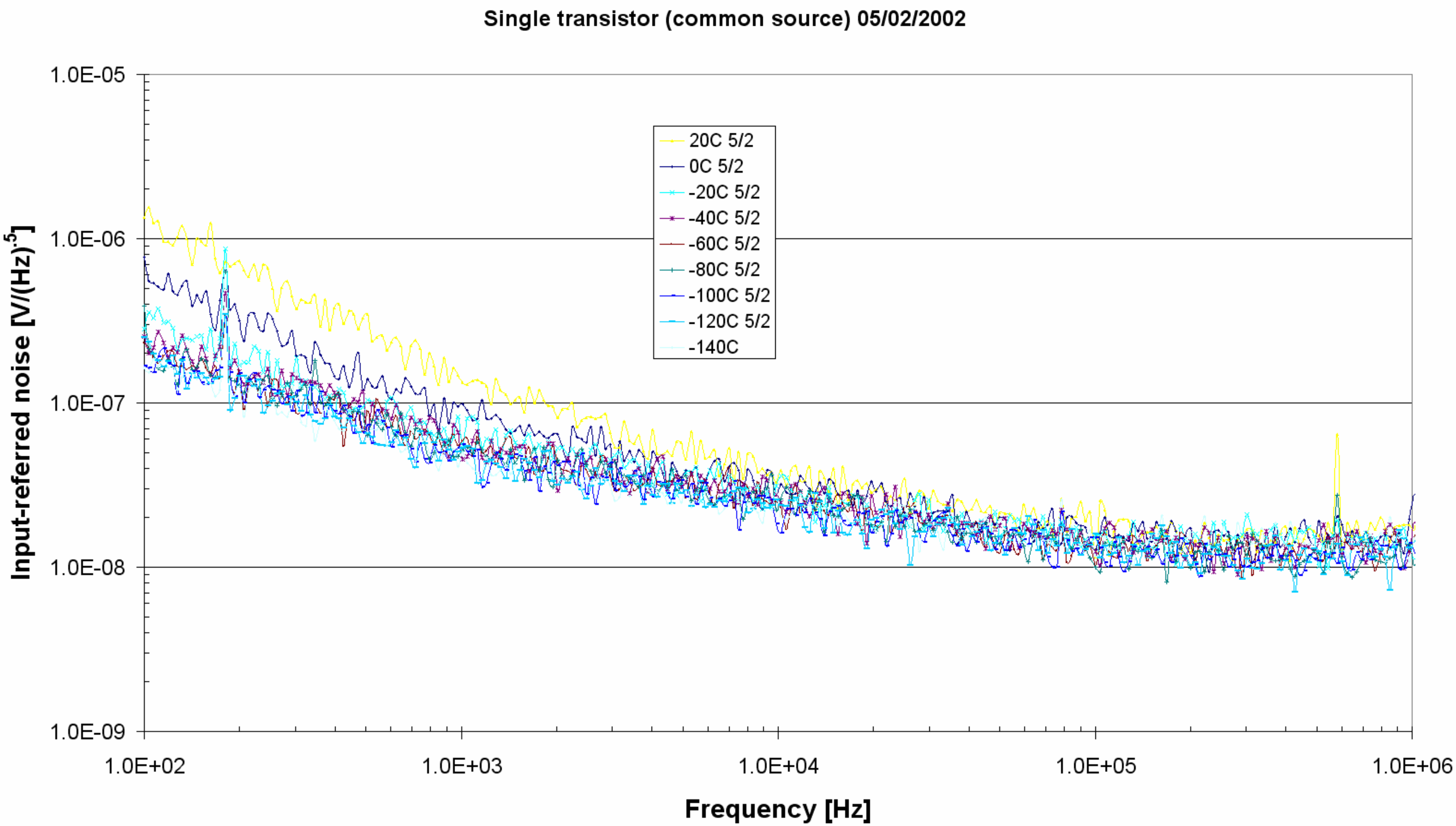
Fig. 8. Measured subthreshold characteristics of a 47/6 buried channel PMOSFET with 1.5-μm gate-to-source/drain spacing. The substrate bias varied from 25 (rightmost curve) to 75 V (leftmost curve) in 10-V steps. The temperature was $-128\,^{\circ}$C, and the drain to source voltage was -1 V.

47/6 P-channel MOSFET (buried channel) 10 kΩ-cm substrate (n type)

Source-follower transistor used on LBNL CCDs

S.E. Holland, D.E. Groom, N.P. Palaio, R.J. Stover and M. Wei, *IEEE Trans. Elec. Dev.*, **50**, 225, 2003.

Noise measurements (20C to -140C)



47/6 buried channel P MOSFET: White noise ~ 10 nV/Hz$^{1/2}$

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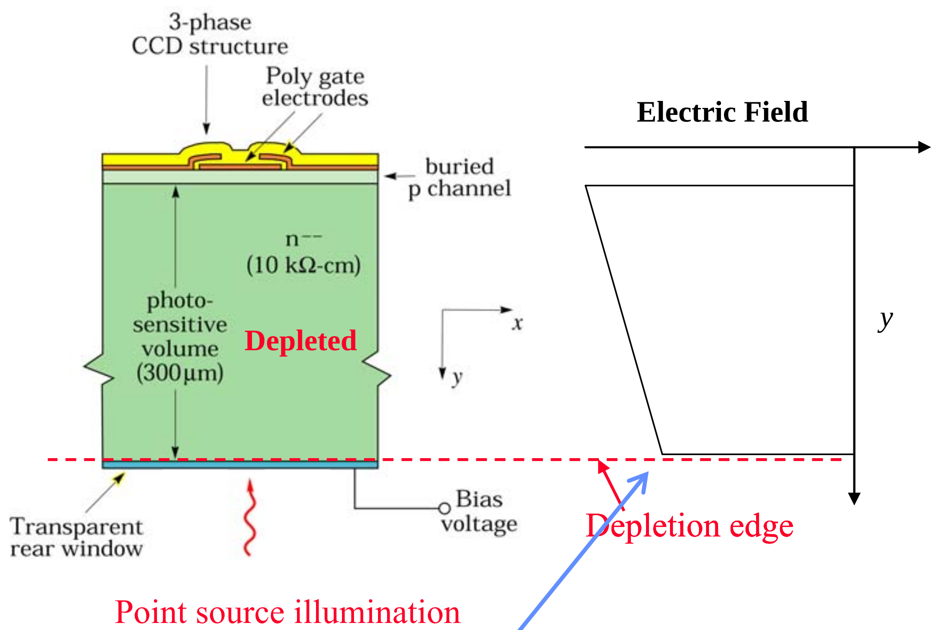
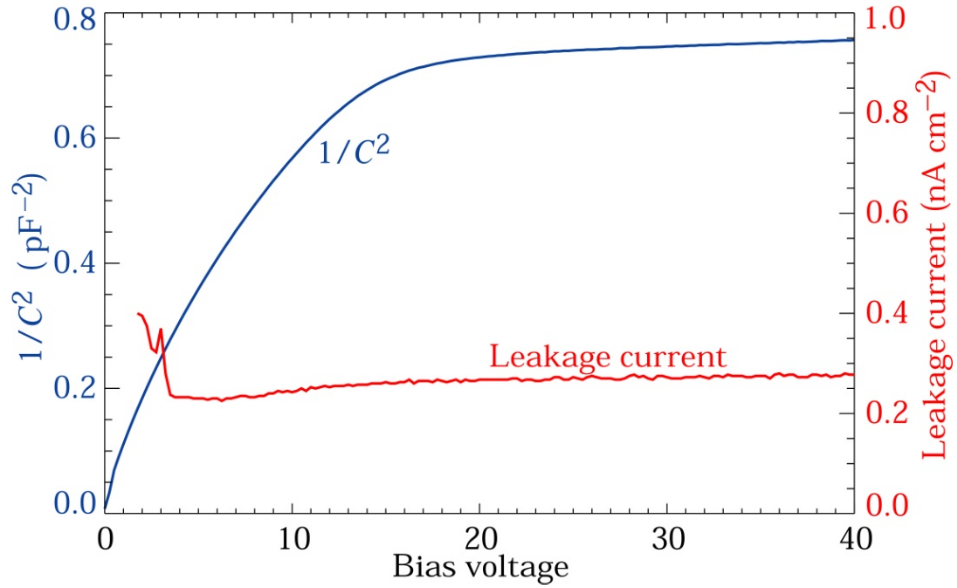
Fully depleted CCDs: Backside defects



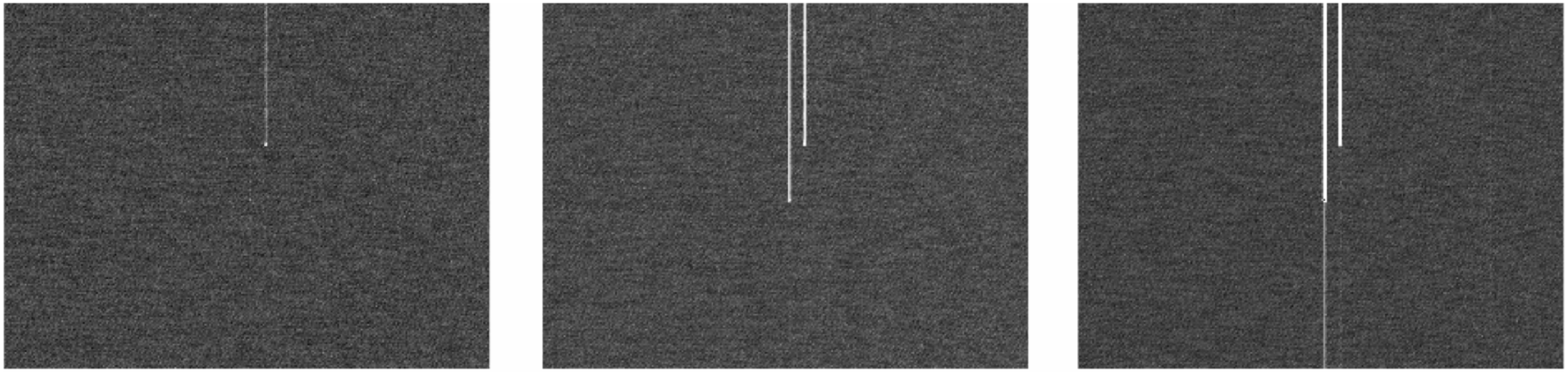


p-i-n test device on back-illuminated CCD wafer

Overdepleted operation results in a significant electric field at the backside of the CCD

Defects at the back side of the CCD can result in high dark current

High-voltage considerations: Dark current from backside defects

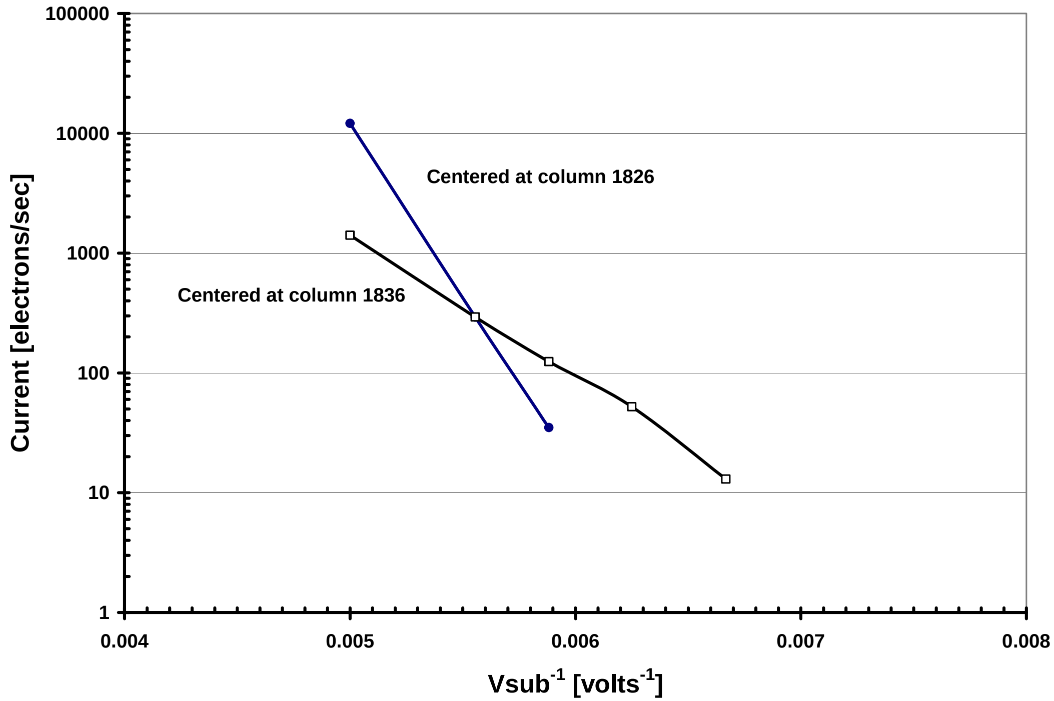


V_{sub} = 160V   180V   200V

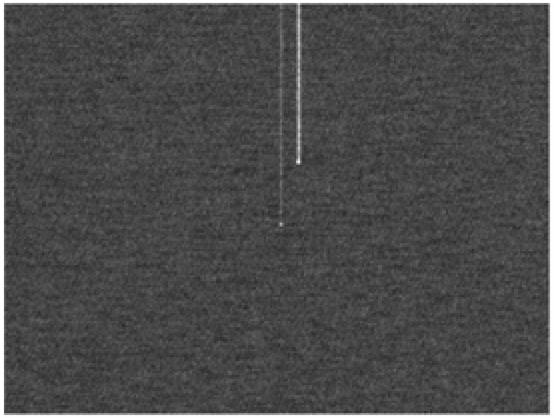
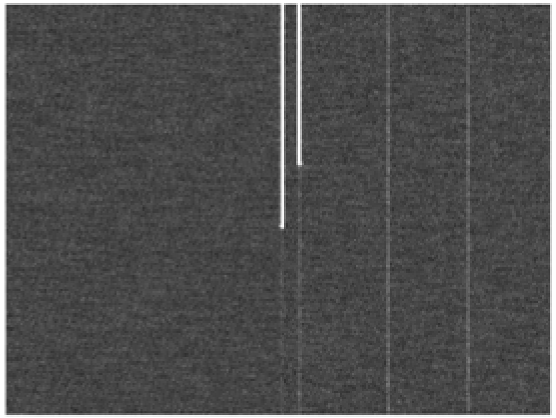
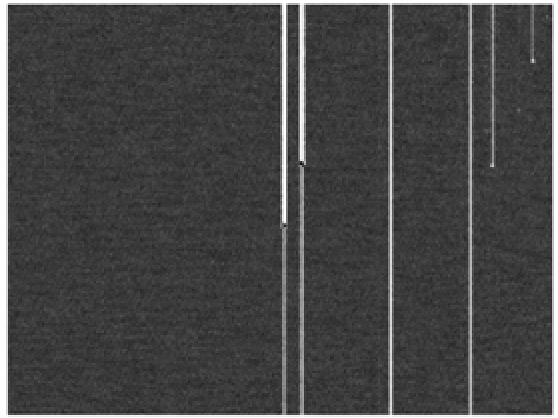
Sub-image: 290 x 220 pixels
Temperature = -140C

CCD 107409-22-3
1700 x 1836 (10.5 µm pixel)

200 µm thick CCD



High-voltage considerations: Dark current from backside defects

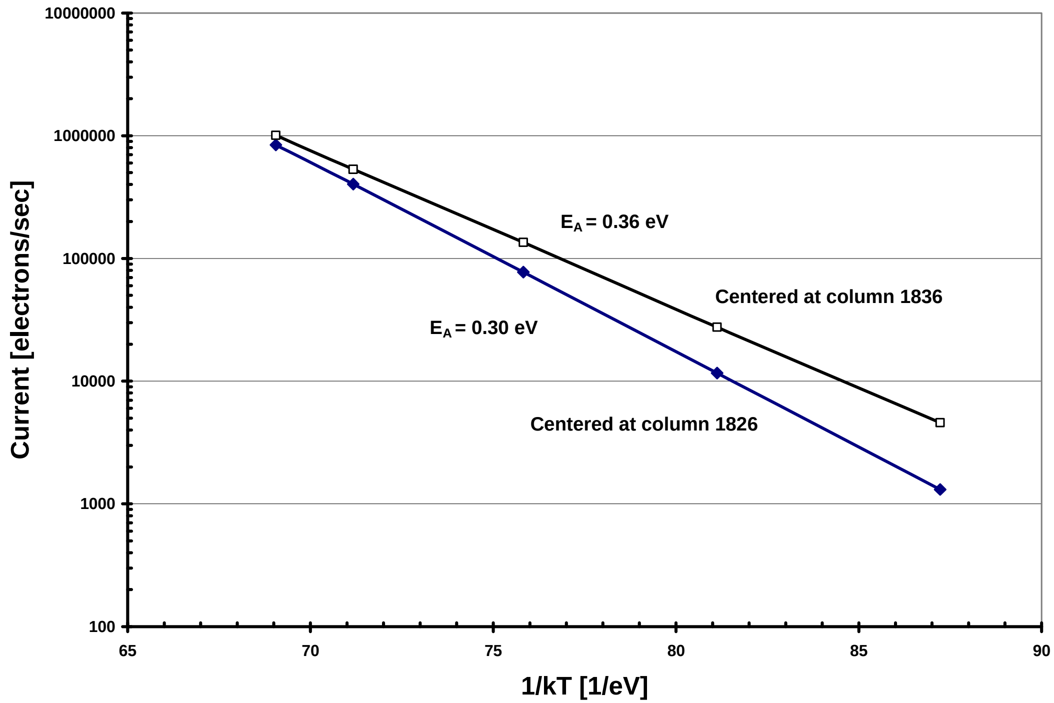




Temperature = -140C -120C -105C

Sub-image: 290 x 220 pixels
V_{sub} = 170V

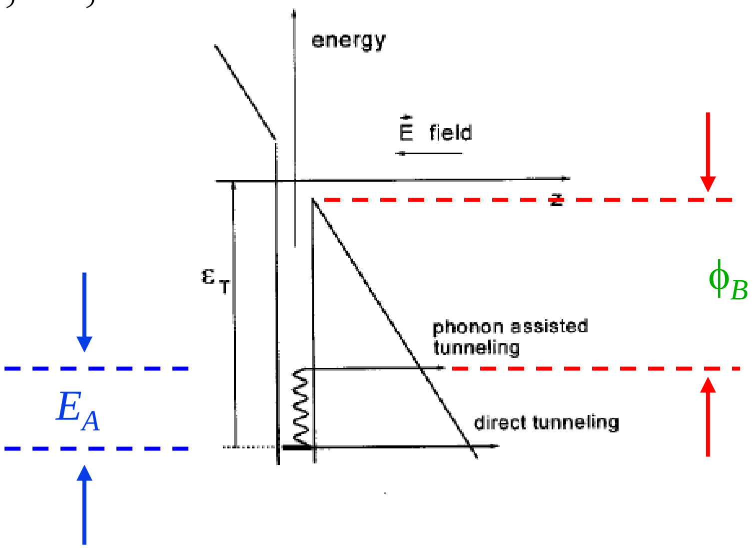
CCD 107409-22-3
1700 x 1836 (10.5 µm pixel)

200 µm thick CCD



Trap-assisted tunneling: Dark current issue with fully depleted CCDs

Phys Rev B, 61, 10361



WKB tunneling factor:

$$\exp\left(-\frac{4\sqrt{2}}{3}\frac{m_r^{1/2}\phi_B^{3/2}}{e\hbar E}\right)$$

Boltzmann factor: $\exp(-E_A/kT)$

Electric field at backside of fully depleted CCD:

$$E_{BACK} = -\left(\frac{V_{sub} - V_J}{y_{sub}} - \frac{qN_{D,sub}}{\varepsilon_{Si}} y_{sub}\right)$$

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CCD fabrication

- We use a hybrid fabrication approach to CCD production
  - —Most of the processing is done at DALSA Semiconductor, a commercial foundry located in Bromont, Quebec, Canada

CCD fabrication

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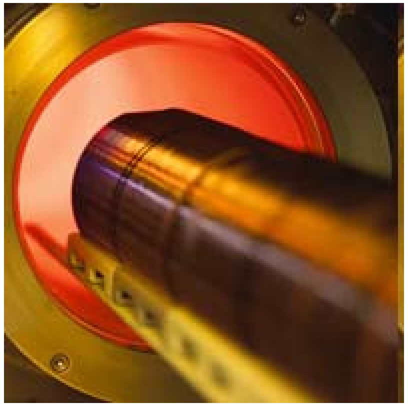
www.dalsa.com



2.5 μm CCD technology with scanner lithography for large-area CCD fabrication
150 mm diameter wafers

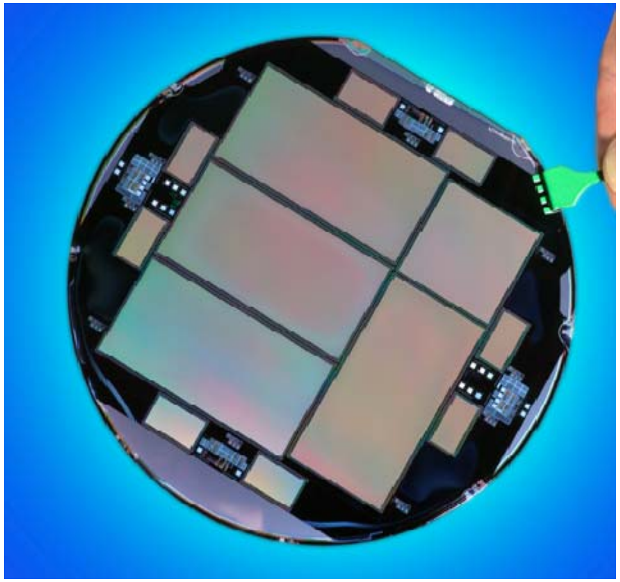
CCD fabrication

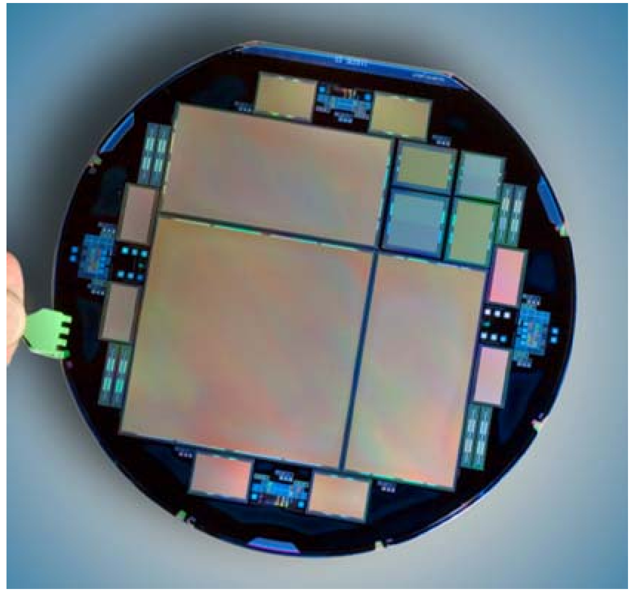
- Hybrid fabrication approach to CCD production (cont')
  - —The wafers are shipped to LBNL after completion of about 80% of the processing
  - —The wafers are thinned to the final desired thickness, typically 200–250 µm thick, at a commercial vendor
    - Process is backgrind followed by CMP to remove sub-surface damage introduced by the backgrind
  - —Processing of thinned wafers at the foundry is not feasible at this time, so the specialized steps on thinned wafers are done at LBNL

CCD fabrication

- Hybrid fabrication approach to CCD production (cont')
  - —The wafers are then completed for back-illumination at the LBNL MicroSystems Laboratory
    - Backside in-situ doped polysilicon deposition
    - Conventional contact/metal lithography and etch
    - Backside anti-reflection coatings
      - —55 nm ITO, 80 nm SiO_2
  - —The processing is done in <u>batch mode at the wafer level</u> using conventional semiconductor fabrication equipment, with some modifications to the equipment to avoid backside damage during robotic wafer handling

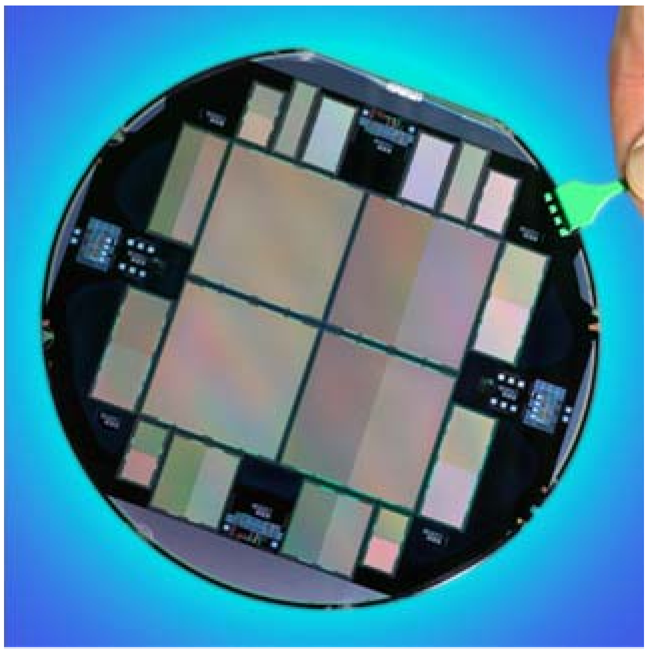
Current LBNL CCD efforts on 150 mm diameter wafers with DALSA Semiconductor





Dark Energy Survey camera wafer (FNAL)

62 2k x 4k CCDs required for a camera at CTIO telescope in Chile



4k x 4k wafer

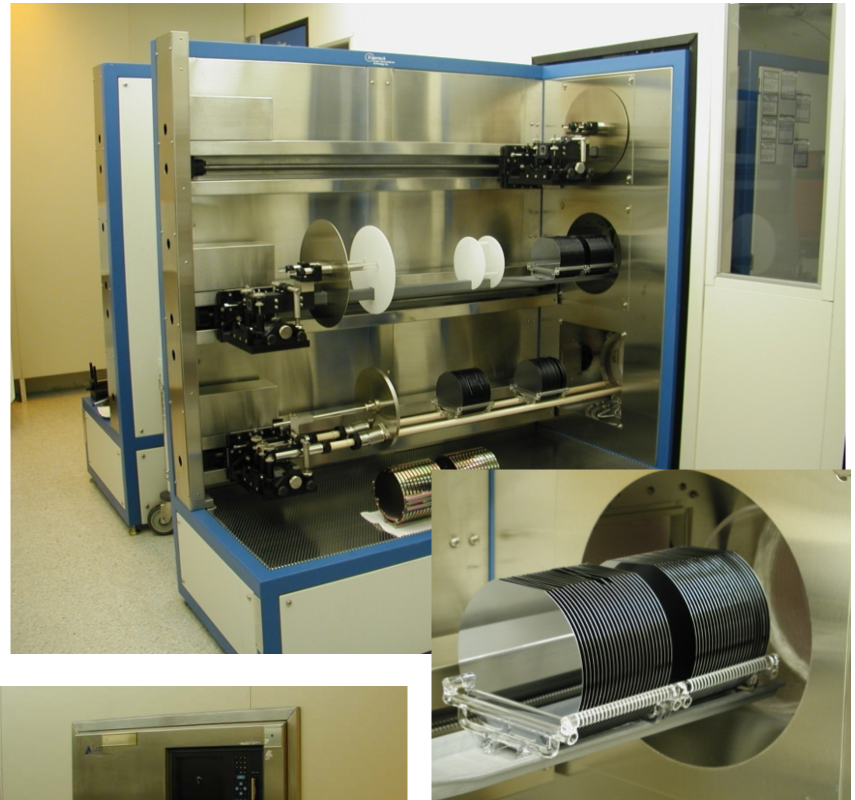
Sloan/Keck spectrograph upgrades and SWIFT spectrograph (Palomar)

SNAP V3 wafer
JDEM (space mission) candidate

LBNL MicroSystems Laboratory

- Class 10 semiconductor fabrication facility
  - Upgraded to 150 mm wafer capability

Projection aligner lithography system
Beta Squared Lithography (P/E)



Atmospheric and
low pressure
chemical vapor
deposition furnaces
Expertech (Thermco)

Dielectric plasma etcher
Lam 4520 XLE

CCD fabrication

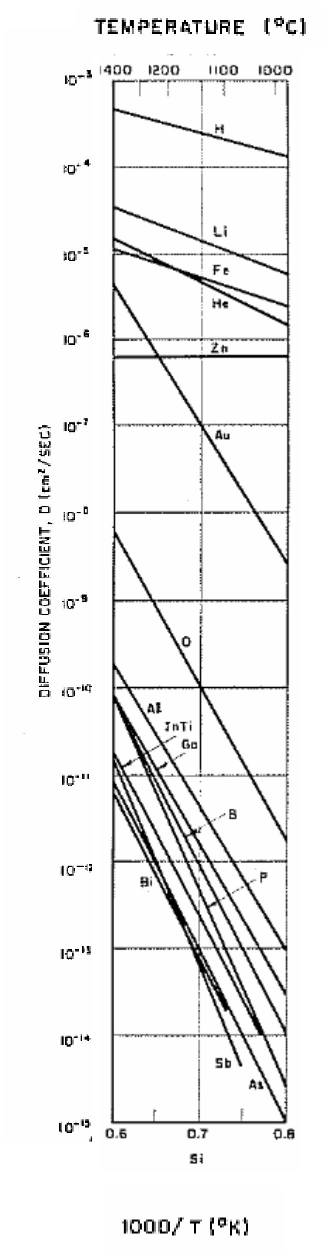
- Need to maintain the high resistivity of the wafers throughout the high-temperature processing steps used in CCD fabrication

- Also need to eliminate metallic contamination that can affect dark current and charge transfer efficiency

  —Gettering steps required

BERKELEY LAB

Gettering for high-resistivity silicon



From S. M. Sze, "Physics of Semiconductors Devices", 2nd edition, 1969.

- Metal contamination in silicon results in energy levels in the silicon bandgap, resulting in increased dark current and carrier trapping
- However, the metals are fast diffusers and can be trapped at gettering sites
- We begin CCD processing by depositing a 1 µm thick, in-situ doped (phosphorus) polysilicon (ISDP) layer on the backside of the wafer
  - Metals trapped in polysilicon grain boundaries and by P-vacancy complexes

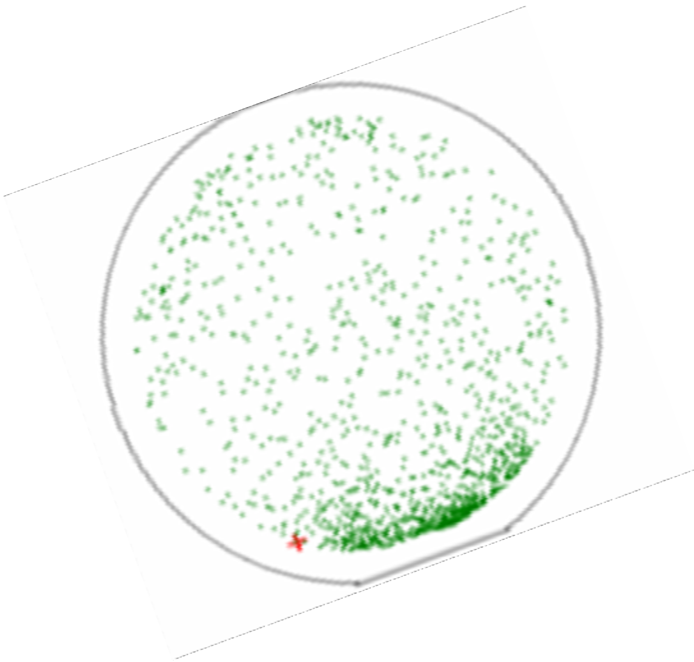
Gettering details

- The in-situ doped polysilicon gettering layer is not a standard process from the vendors of high-resistivity silicon wafers, so this step is done at DALSA Semiconductor

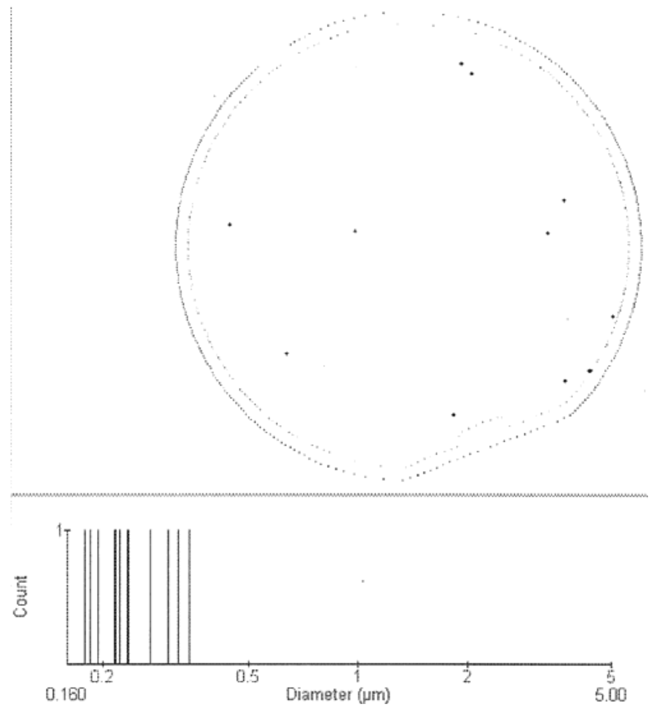
- We have observed metal contamination from robotic wafer handlers that contact the wafer before the gettering layer is deposited
  - Process flow has been modified to avoid this condition

- The polysilicon deposition process is inherently "dirty", and we repolish the front sides of the wafers to remove particles deposited during the long deposition step

Gettering issues: ISDP particles

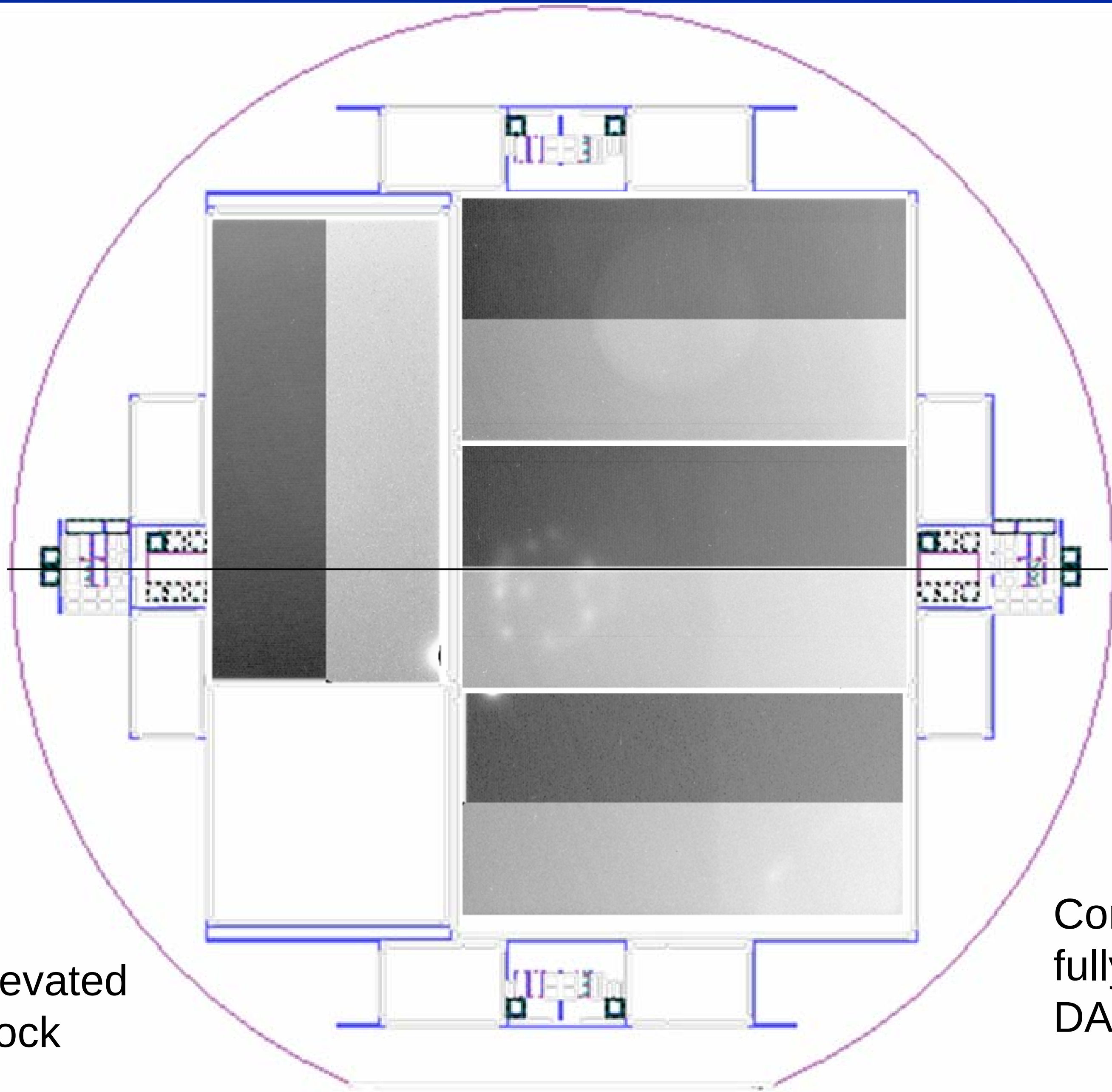


Particle map after ISDP deposition



Particle map/histogram after polishing

Cold probe image (-45C) map of FNAL DES wafer



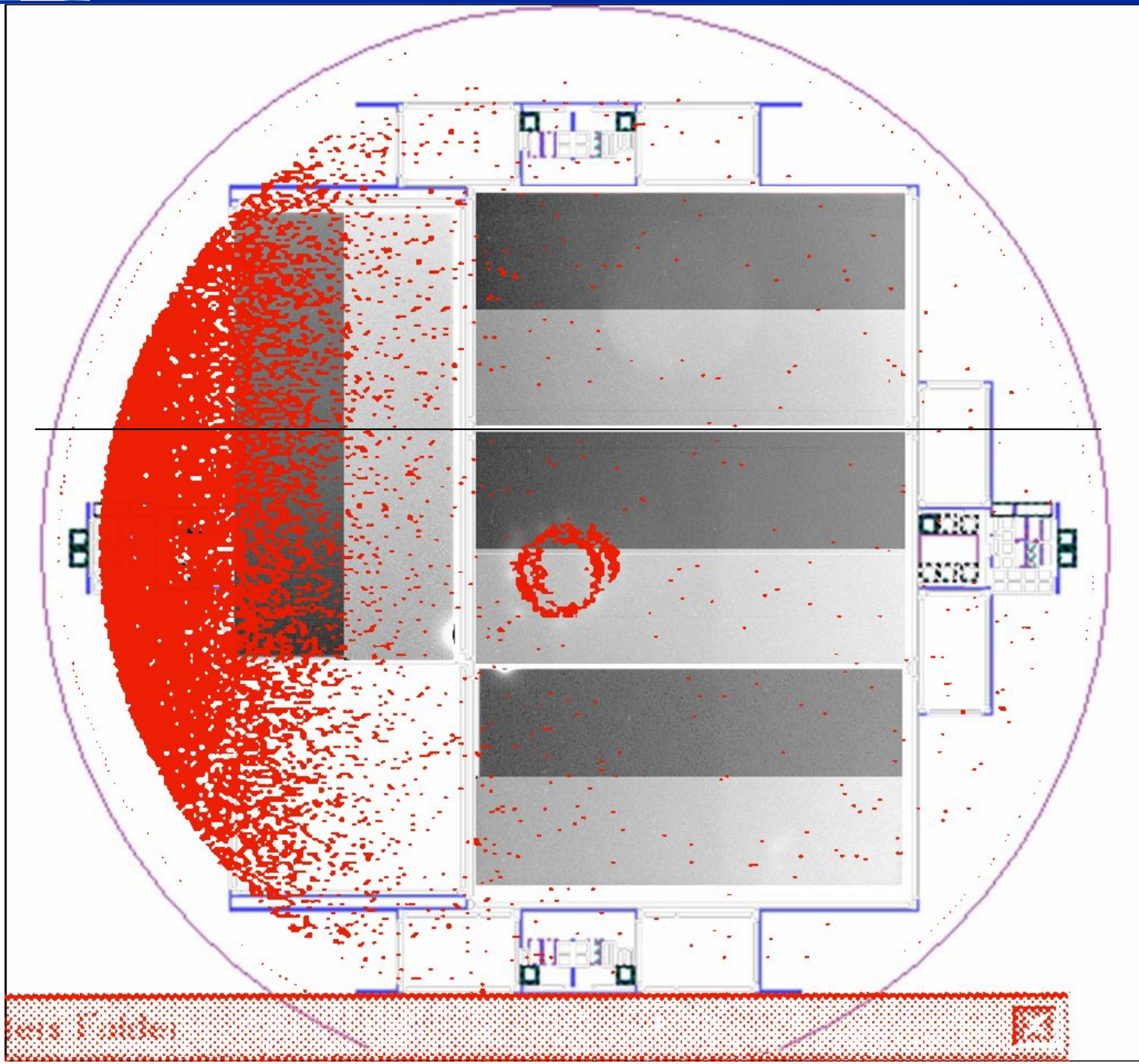
60s dark at elevated Vsub and Vclock

Control wafer fully finished at DALSA

Overlay of particle map on cold probe images

Red: Particle map supplied by DALSA

The source of the particles are robotic handlers that come in contact with the back sides of the wafers

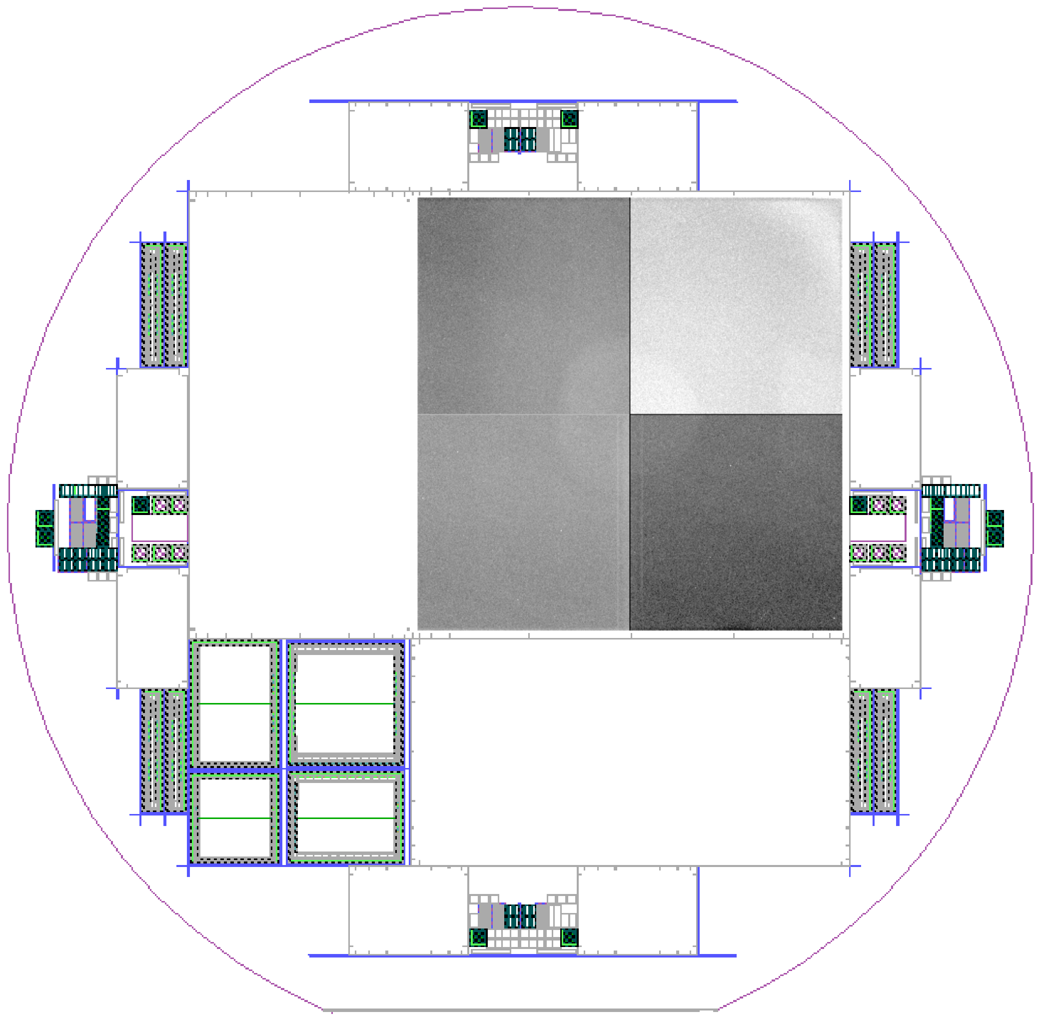


Cold probe result on 4k x 4k with new process flow

127298-1
60 sec dark
-45C cold probing
DALSA control wafer

Elevated Vsub
and Vclock

New lot with modified
process flow to eliminate
contamination seen
on previous 4k x 4k lot



COLD PROBE SUMMARY

Device: 127298.1.4
Format: SNAP, 4 corner readout
Test Date: 2008-08-26T11:55:08.000
Temperature: -45C.
Operator Initials: JE.

1. Summary of Bad Columns

No hot columns in 1 s dark image.
No hot columns introduced by increasing clock voltages.
No hot columns introduced by increasing Vsub.
No blockedcolumns.

There are no bad columns in this device

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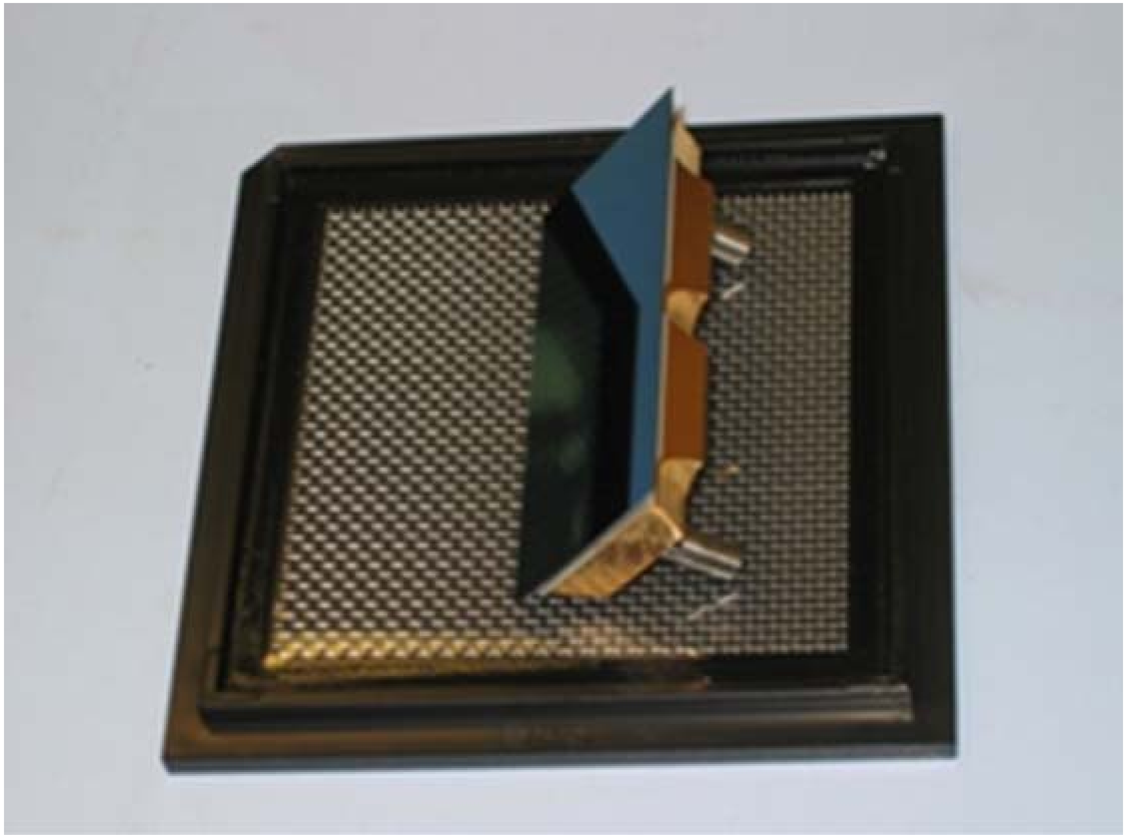
Dark Energy Survey Camera (FNAL)

LBNL provides cold probed die

Packaging and final testing done at FNAL

The camera requires 62 science-grade, 2k x 4k (15 μm pixel) CCDs

The camera will be installed at CTIO



2k x 4k CCD in FNAL 4-side buttable package

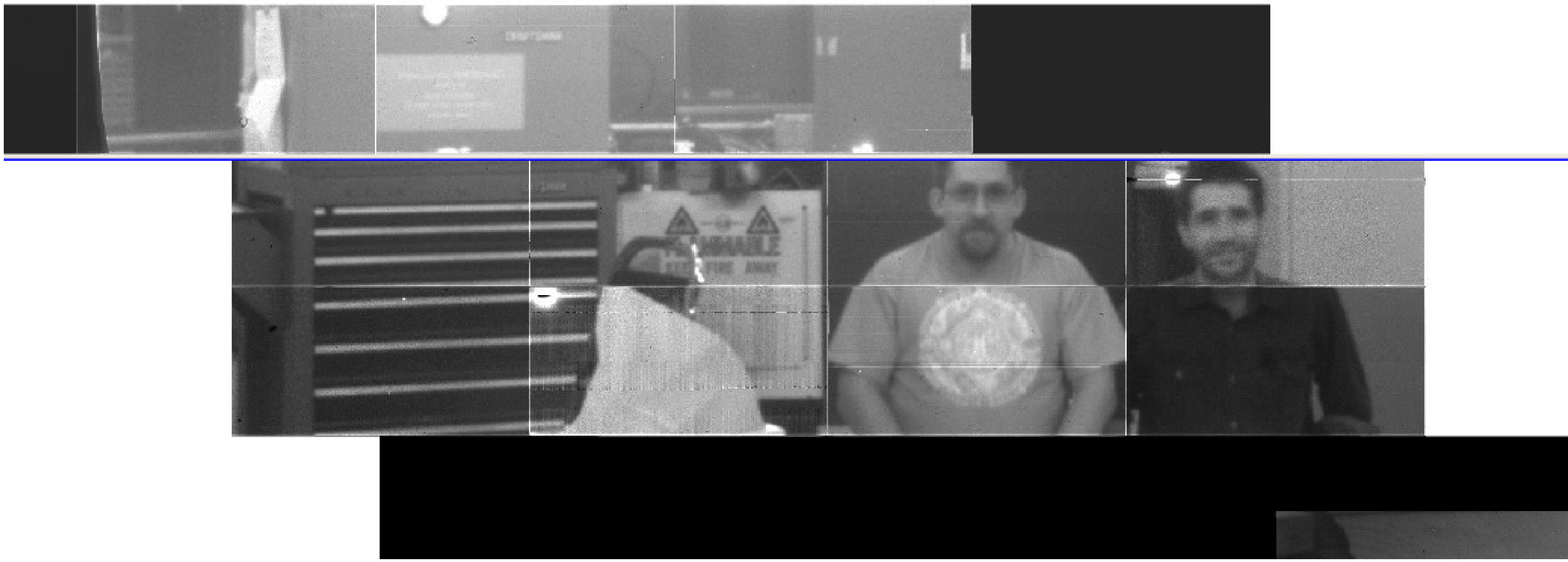
Image courtesy of T. Diehl (FNAL)

Dark Energy Survey efforts at FNAL

FNAL multi-CCD test vessel: Currently reading out 12 engineering grade CCDs

Picture on the right shows a Monsoon crate with high-density boards developed by collaborators from Spain

Pin hole image

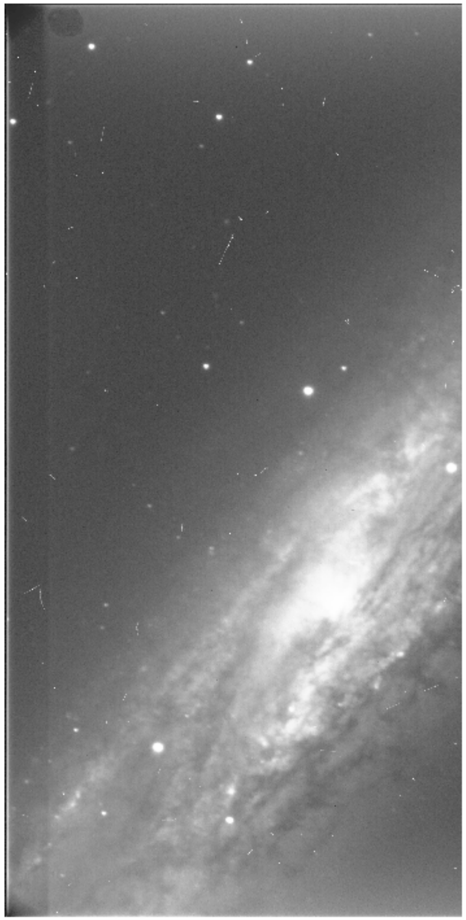


Dark Energy Survey Camera (FNAL)

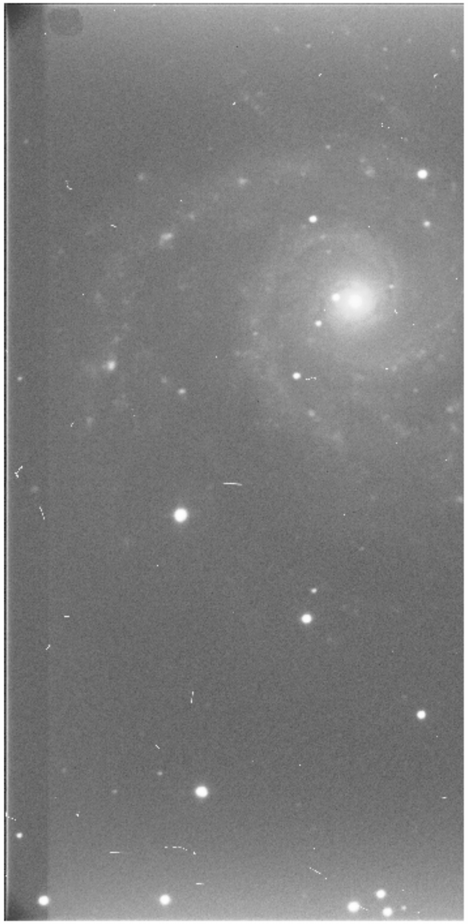
Crab Nebula
10/3/2008

2k x 2k from CTIO 1-m telescope
Image courtesy of D. Kubik (FNAL)

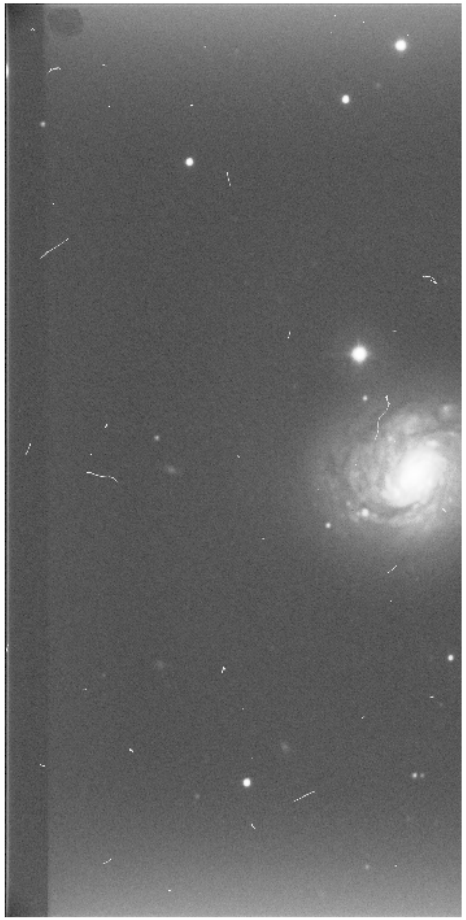
Dark Energy Survey Camera (FNAL)



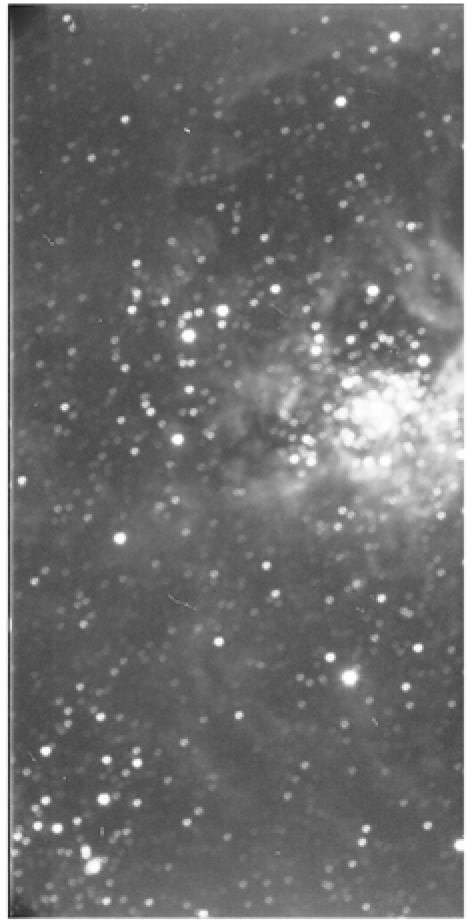
NGC 253
10/3/2008



NGC 628



NGC 1068



NGC 2070

2k x 1k images from CTIO 1-m telescope

Images courtesy of D. Kubik (FNAL)

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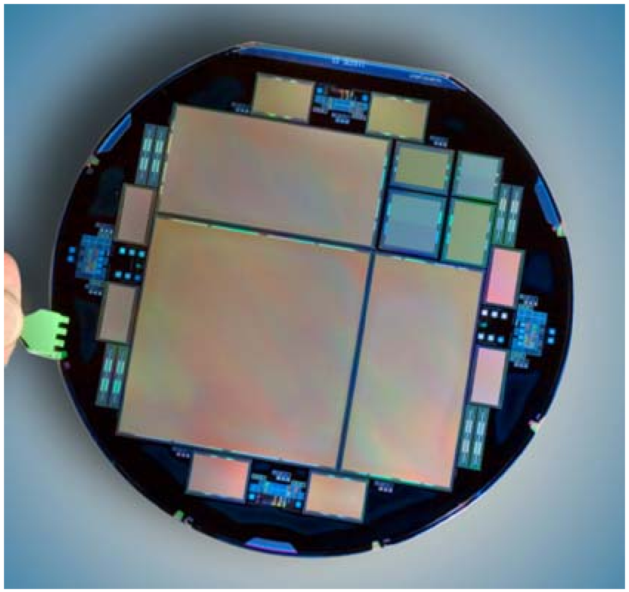
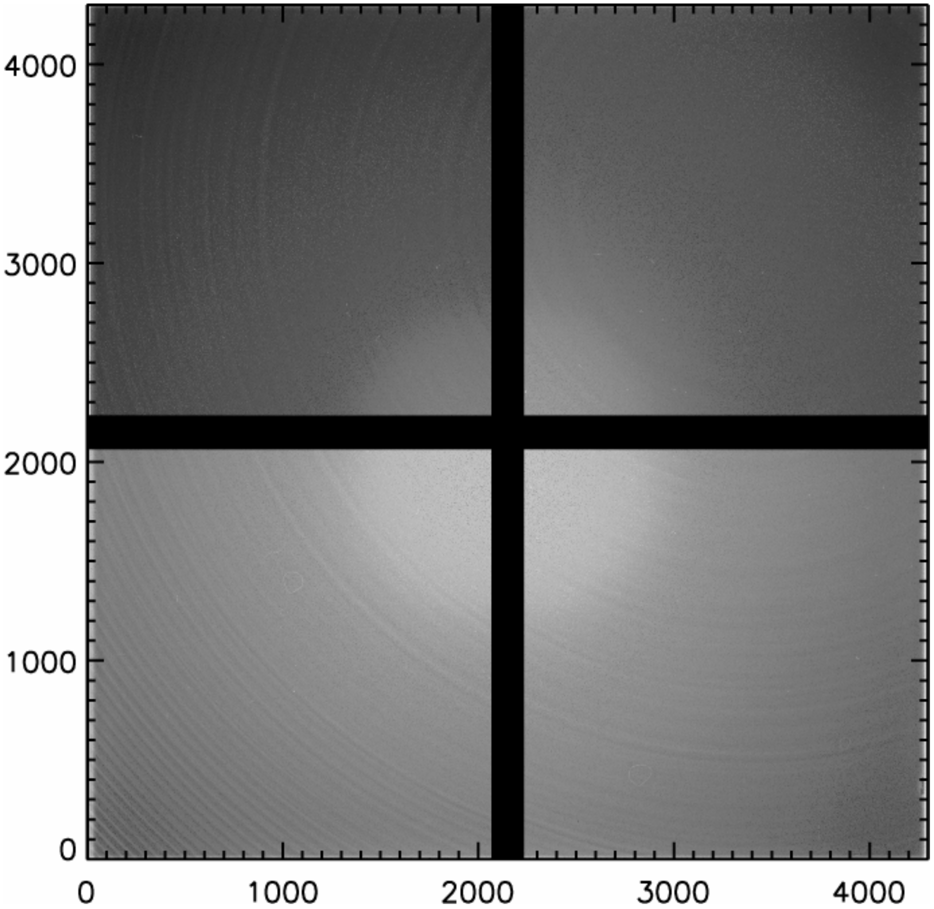
4k x 4k development

- We are fabricating 4k x 4k (15 µm pixel) CCDs for ground-based spectroscopy
  - —Baryon Oscillation Spectroscopic Survey (BOSS) at Sloan
  - —Possible Keck LRIS upgrade

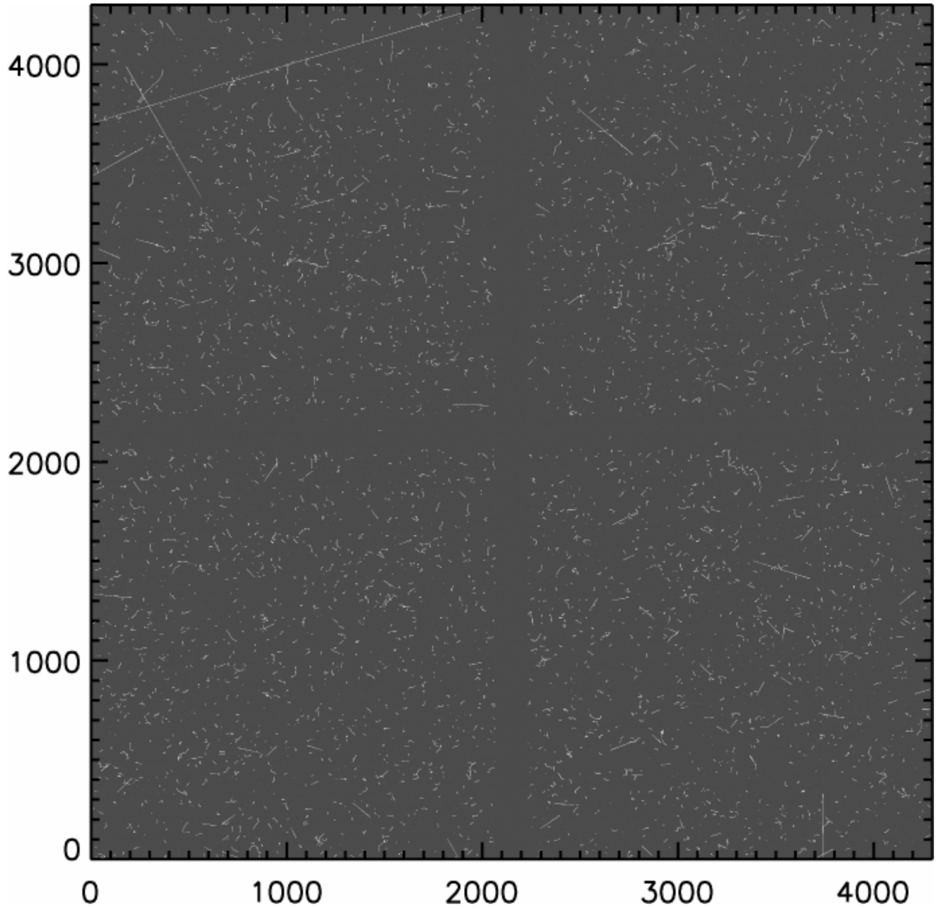
- Have also delivered 4k x 2k (15 µm pixel) CCDs for SWIFT (Palomar)



Packaged 4k x 4k at -140C with new process flow and after LBNL backside defect yield improvement



Flat field image (slightly non-uniform light source)



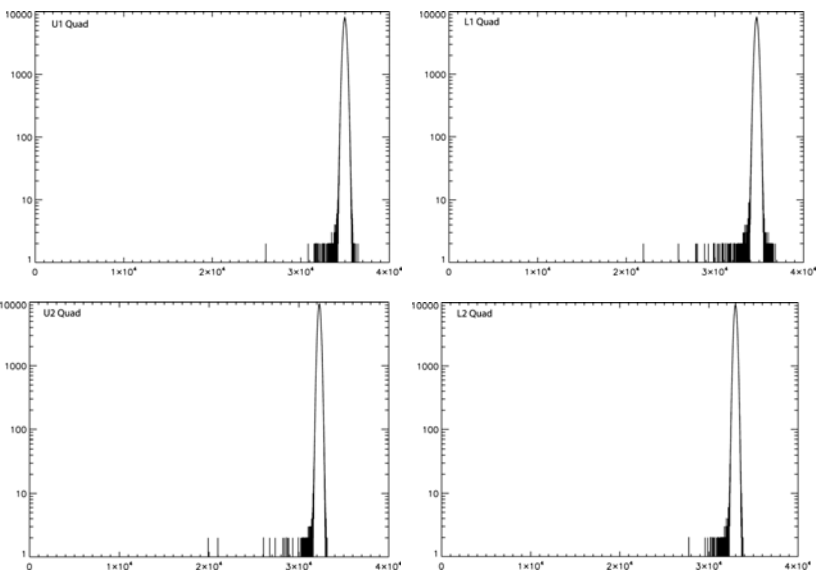
Dark current (30 minute exposure)
0.7 electrons/pixel-hour at -140C

Science-grade CCD to be installed at the Sloan Digital Sky Survey telescope

Test summaries for BOSS 4k x 4k's

Transistor	Gain (ADU/e-)	Noise (e-)
U1(LL)	1.569	3.0
U2(UL)	1.450	3.1
L1(LR)	1.566	2.9
L2(UR)	1.499	3.3

Observed Traps with Depth 50% or more			
Quadrant	Forward Traps	Reverse Traps	Trap Density
U1 (LL)	59	23	2.11E-05
L1 (LR)	59	18	1.98E-05
U2 (UL)	44	39	2.14E-05
L2 (UR)	33	28	1.57E-05

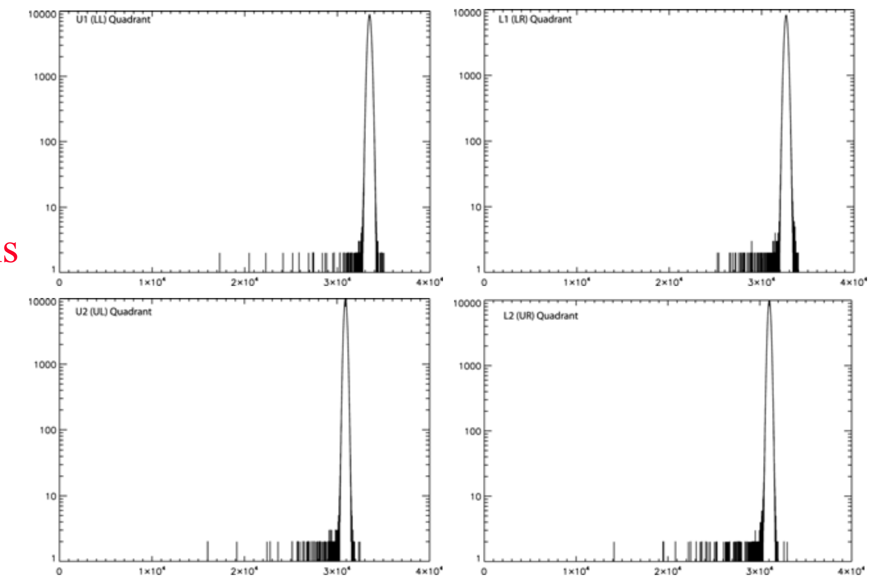


127298-14-4: 0.7 e-/pixel-hr at -140C
0 hot columns 0 blocked columns
0 hot pixels 5 dark pixels
Hot/dark pixels exceed 20% from median

Flat Field Histograms

Transistor	Gain (ADU/e-)	Noise (e-)
U1(LL)	1.556	3.4
U2(UL)	1.468	3.2
L1(LR)	1.525	4.0
L2(UR)	1.385	3.5

Observed Traps with Depth 50% or more			
Quadrant	Forward Traps	Reverse Traps	Trap Density
U1 (LL)	122	97	5.64E-05
L1 (LR)	90	58	3.81E-05
U2 (UL)	118	83	5.18E-05
L2 (UR)	95	86	4.66E-05



127298-8-4: 0.7 e-/pixel-hr at -140C
2 "warm" columns 0 blocked columns
1 hot pixels 29 dark pixels
Hot/dark pixels exceed 20% from median

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Summary

- Fully depleted operation is preferable in order to maintain good spatial resolution for back-illuminated CCDs

- This puts stringent demands on the backside layer
  - —Hot pixels can result when the depletion region reaches the back surface
  - —For scientific CCDs used in astronomy, cryogenic operation greatly reduces the effect
  - —Backside layer is critical
    - ISDP works well but is not compatible with aluminum metallization
    - For our application we are able to process 200–250 μm thick wafers with standard semiconductor fabrication equipment, allowing for batch-mode fabrication

Summary

- Much effort has gone into the fabrication model used at LBNL, but the process is now fairly routine and stable
  - — Thinning technology development
  - — Low damage plasma etch development
  - — Gettering issues
  - — Robotic wafer handling to minimize backside damage
- We look forward to commercially available, back-illuminated imagers

Acknowledgements

- LBNL CCD group: N. Roe (Group leader), C. Bebek, J. Emes, D. Groom, A. Karcher, W. Kolbe, J. Lee, N. Mostek, N. Palaio, J. Thacker, C. Tran, G. Wang
- Lick Observatory: W. Brown, R. Stover, M. Wei
- FNAL DES group: T. Diehl, J. Estrada, B. Flaugher, D. Kubik
- JPL: S. Nikzad, J. Blacksberg, M. Hoenk, S. T. Elliott
- DALSA Semiconductor: R. Groulx, F. Dion
  - References: http://www-ccd.lbl.gov