Back Side Illumination

History and Overview

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IISW 2009 Bergen

Outline

- Focus on overview of scientific BSI detectors
- Overall need for back-side illumination
- Historical overview of back-side illumination
- Backside processing technologies
- Backside QE enhancement physics
- Recent BSI detector progress
- Outlook for BSI imagers

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Overall Need for BSI Detectors

- Increase quantum efficiency (QE)
  - no frontside absorption/reflection
  - silicon reflection limited response is possible with good backside processing
- Broaden spectral response
  - silicon detectors capable of very good X-ray through near-IR response

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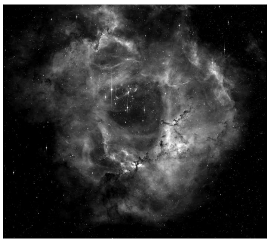
BSI Imaging



2x2 mosaic of BSI 4kx4k CCDs

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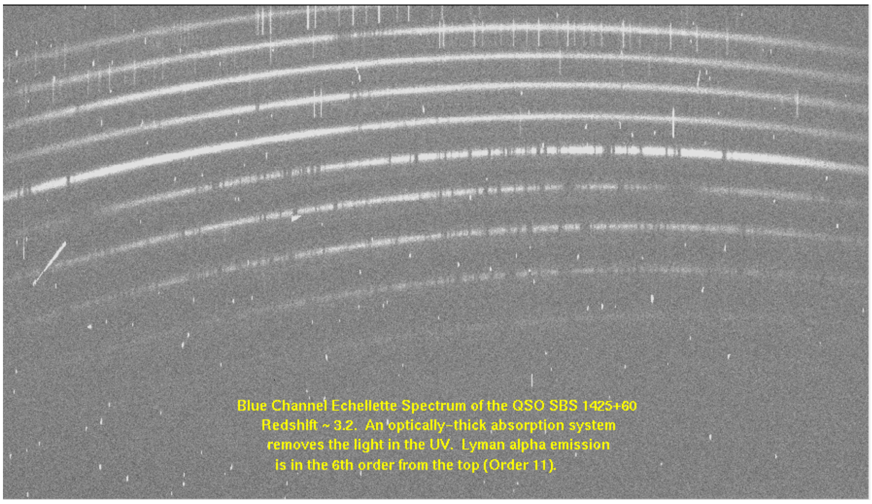
BSI Spectroscopy



long exposures, require low dark current and low noise

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BSI QE

- Goals for optimal BSI detectors
  - minimize reflection loss at back surface
    - optimize antireflection coatings for desired measurements
  - maximize internal QE
    - stop all photons in active silicon
    - collect all photogenerated electrons in appropriate pixel
  - reduce BSI related noise sources
    - minimize induced cosmetic defects
    - minimize charge diffusion
    - maintain optimal Charge Transfer Efficiency (CCDs)

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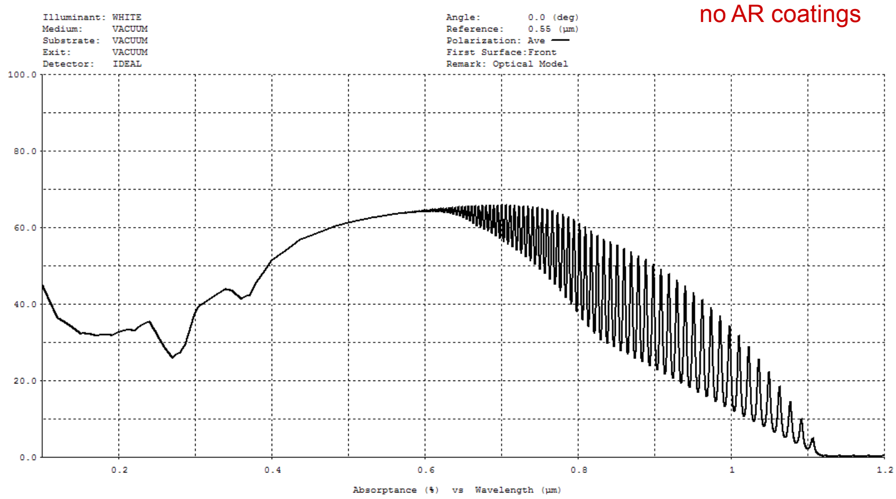
Ideal Silicon QE
10 μm Silicon

no AR coatings



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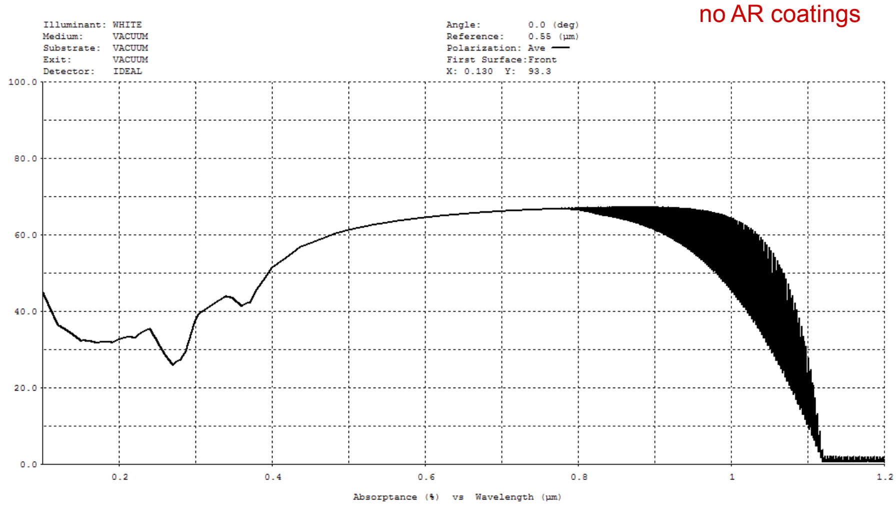
Ideal QE
50 μm Silicon

no AR coatings



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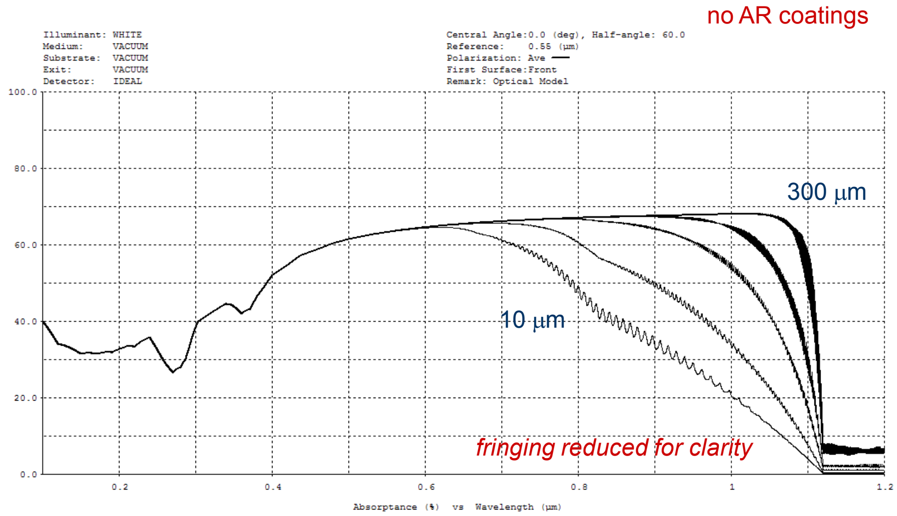
Ideal QE
10, 20, 50, 100, 300 μm Silicon



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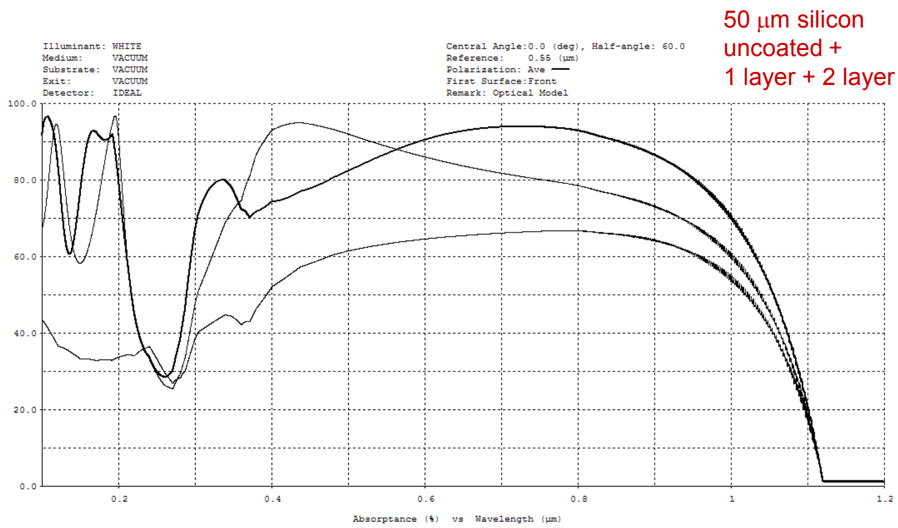
Ideal QE with AR Coatings



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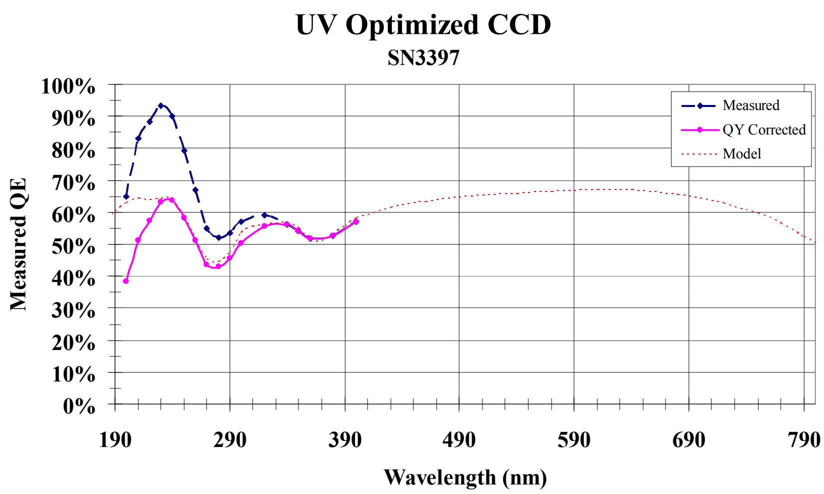
Example: UV 193 nm laser



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Example: Visible / Near-IR

- STA1920A 4kx4k CCD (16 outputs)
  - ~ 100 μm thick detector for LSST project
- Transparent and conductive backside contact applied to backside after thinning
- Coatings applied in thermal evaporation chamber
- Backside bias from guard rings around die (STA design)
- Final version is buttable

see Steve Holland's talk on thick, fully depleted backside detectors

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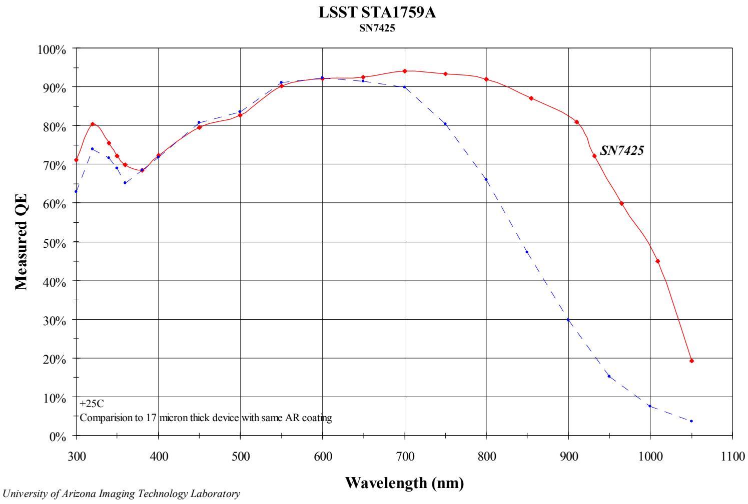
LSST CCD - 93 μm thick



University of Arizona Imaging Technology Laboratory
M. Lesser 16Jan08

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Obtaining Optimal QE in Visible

- Use appropriate thickness silicon for red applications
- Design AR coating for application and actual silicon thickness
- Consider internal fringing
  - reduced with low red reflectance and thicker silicon
- Use blue/UV transparent AR coating materials as needed

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Obtaining Good MTF for BSI

- Modulation Transfer Function (MTF) strongly influenced by charge spreading due to undepleted silicon
- Depletion $\propto$ (Si resistivity)$^{1/2}$
- Must use proper Si for imager fabrication
  - standard epi has been < 100 Ω-cm, 5 – 20 µm thick
  - preferred backside epi is 100 – 5,000 Ω-cm, up to 50 µm thick
  - fully depleted devices are 5k – 10k Ω-cm, 100 - 300 µm thick

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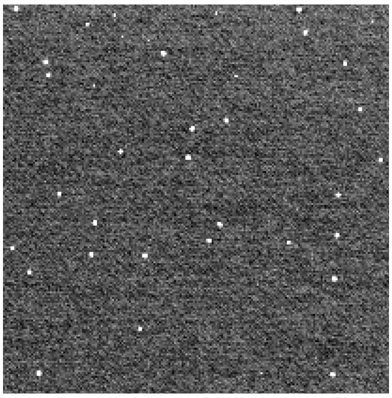
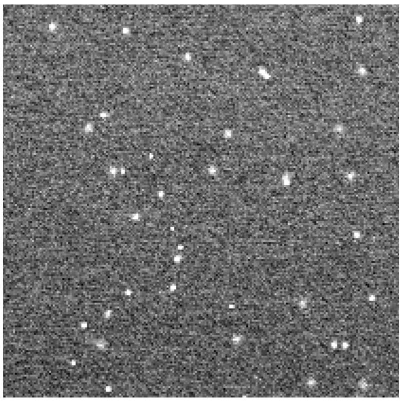
Depletion – MTF – 93 µm thick CCD

Fe-55 X-ray events

-50 V backside bias





no backside bias

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Historical Overview of BSI

- First BSI devices in mid 1970's
  - improve blue response of broadcast cameras
- Commercial
  - RCA ⇒ Sarnoff
  - Texas Instruments (first Hubble work)
  - EEV/GEC ⇒ E2V
- R&D
  - JPL/NASA
  - MIT/LL
  - University of Arizona

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BSI for Scientific Devices

- E2V
- Sarnoff
- Fairchild Imaging
- STA
- Hamamatsu
- MIT/LL
- JPL
- LBNL
- University of Arizona

…and recent BSI CMOS vendors

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Backside Processing Technologies

- Processing overview follows using the UA ITL Die Level backside process
- Each BSI detector manufacturer has their own process in which these steps vary greatly
- Both die level and wafer level process are used
  - wafer scale most common commercially
- CCD BSI processing is very similar to CMOS imager BSI processing

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BSI Process Steps at ITL

- Receive wafers from foundry
- DC wafer probe @ RT
- AC wafer probe @ -60 C
- Device selection
- Stud bump application
- Backside grind (vendor)
- Dice
- Hybridize
- Epoxy underfill
- Acid protection
- Selective acid etch
- Epitaxial acid etch
- Oxidize back surface
- Chemisorption/AR coating
- Package
- Characterize
- Install in camera

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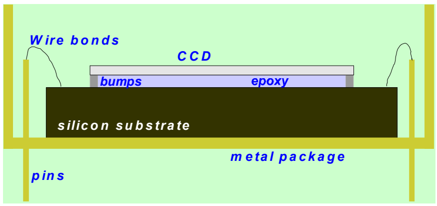
Example: STA0500A BSI Scientific CCD

- typical hybridized large format CCD
- detector hybridized to thick silicon substrate
- indium bumps, epoxy underfill
- die attached & wire bonded to Kovar package



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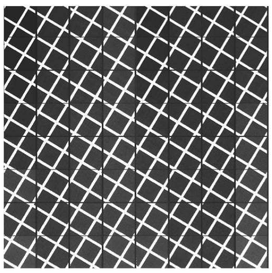
Wafer Probing for Scientific BSI

- DC defects get worse when backside thinned
- Test shorts to 20 MΩ
- AC image (-60 C)

STA2200 Orthogonal Transfer Array CCD @ -60 C



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Hybridization to Silicon

- Silicon substrate used for commercial processing
- Substrate wafer is indium bumped
- Typically hybridize a 250 μm thick detector (CCD or CMOS) to a 1400 μm thick silicon substrate
  - exact thermal expansion match
  - flatness spec on Si substrate can be < 5 μm over 150 mm
- Diced substrate die typically flat to ~2 μm

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Hybridization to Ceramic

- Aluminum nitride replaces silicon as substrate, 1-2 mm thick
- Multilayer, vias, polished
- Traces metallized and indium bumps applied
- Fabricated for die or wafer level
- Standard backside processing
- Mechanical/cooling frame and connectors attached to underside

combination of hybridization and packaging

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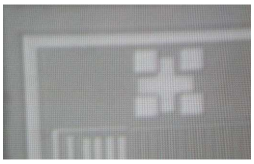
Hybridization

- Flip chip bonders used to align and bond detector and substrate
- Infrared aligner for silicon substrates
- Split field aligner for ceramic substrates



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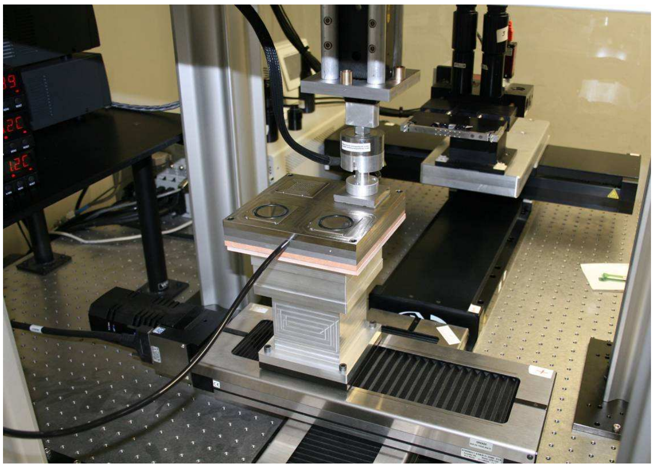
Large Area Hybridization Bonder



250 mm bonding area

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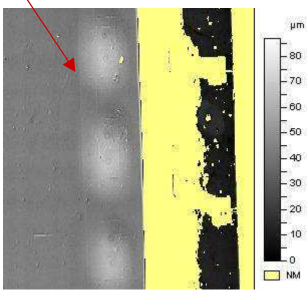
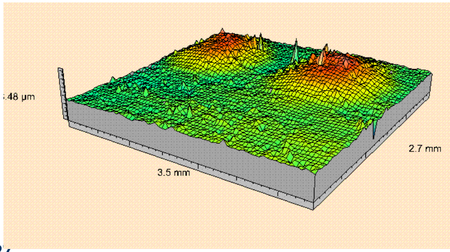
Hybridization Bumps

- Bumps mainly on wire bond pads, not in imaging area
- Regions around bumps (welts) may affect imaging, depending on geometry
- Bumps have been placed under pixels for enhanced fill factor





~ 3 microns tall

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Epoxy Underfill

- Epoxy underfill used to mechanically bond CCD and substrate after bump bonding
- Heat used for viscosity control
- Chip Flatteners hold device surface shape during epoxy cure

4 underfill stations

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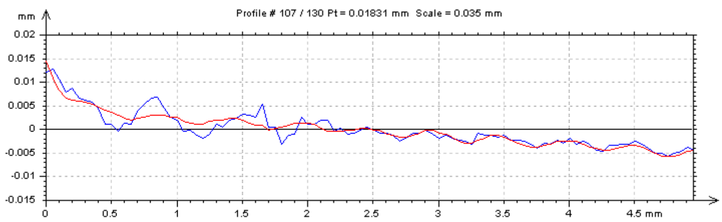
Epoxy Underfill Ripples

- We sometimes see 'ripples' in underfill material associated with edges of device and layout of bumps
  - stress related
  - ~5 μm variations



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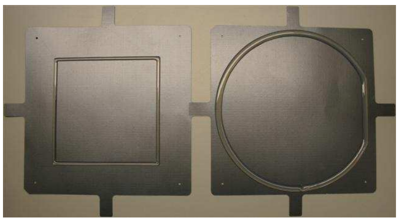
Acid Protection

- Die/wafer edges and substrate must be protected from etching
- Wax used as an acid resist



automated

manual

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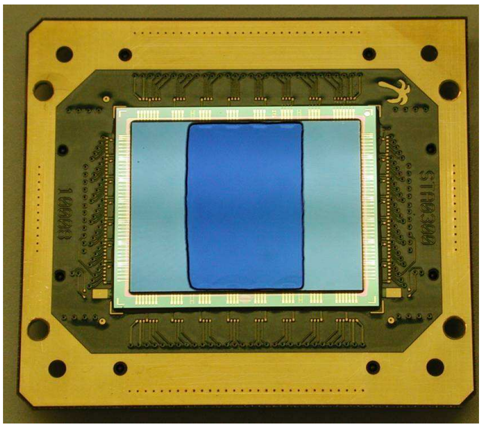
STA Lightning Mapper CCD



Experimental thick frame store region for improved high speed clocking

Selective Acid Etch

- 1:3:8 HF:HNO_3:CH_3COOH acid solution used to etch p+ substrate to epitaxial interface
- Etch selectivity critical to achieve uniform final device thickness
- Bulk silicon is harder to etch uniformly
  - used for some project which need high red QE
- Typical doping levels
  - $p^+ = 10^{18}$ cm^{-3}, $p = 10^{15}$ cm^{-3}
  - 10 – 10,000 Ω-cm verified

Epitaxial Acid Etch

- Etch into epitaxial layer to clear all p^+ material
- Tailor device thickness for MTF optimization
- Excessive etching decreases yield and increases cosmetic problems
- Removes surface stains generated during selective etch

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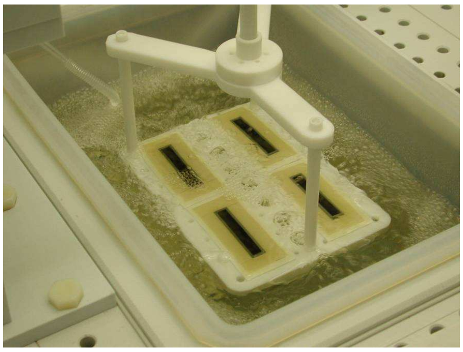
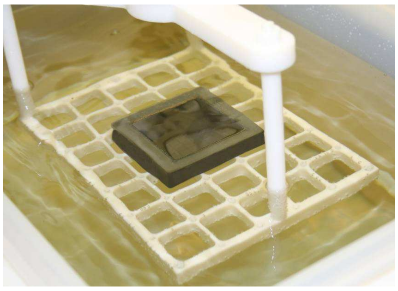
Acid Etching

2 etching stations



4 hybridized die



pinned package

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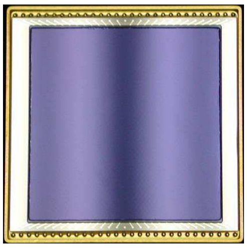
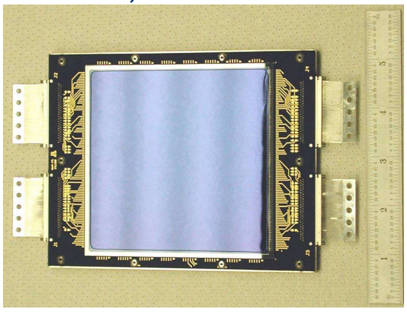
BSI Detector Packaging

- Commercial packages
  - usually not flat (~100 µm)
  - not buttable
  - ~$50 (Kovar, Al_2O_3)
- Custom ceramic, invar, molybdenum, aluminum nitride
  - very flat (<5 µm peak-valley)
  - more stable with temperature
  - better thermal transfer
  - >$500





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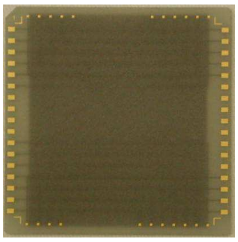
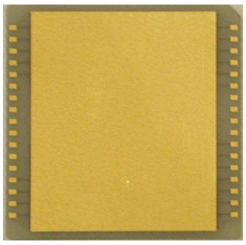
Custom BSI Packaging

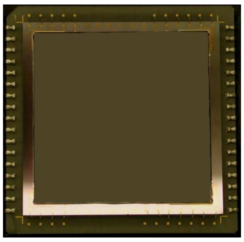
- Customer required backside pinout to match an existing frontside pinout
(Kodak KAF-16801E 4kx4k CCD)
- Multilayer aluminum nitride packages to swap signals underneath detector



top



bottom



CCD

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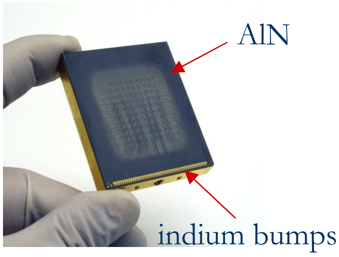
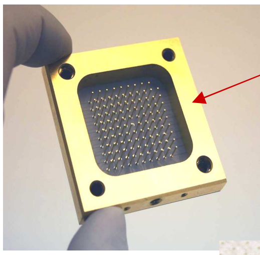
Buttable Imager Example



AlN

indium bumps

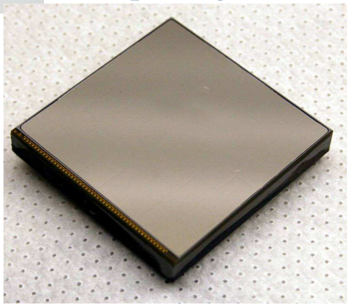
top



CE5 frame

bottom

packaged CCD



package for WIYN One Degree Imager 64 CCD mosaic

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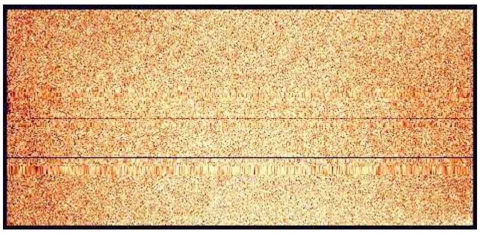
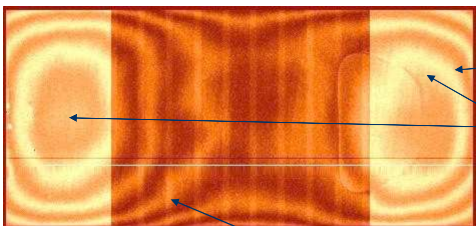
Packaging – Be Careful!

400 nm



structures under CCD may appear in images

900 nm



fringing

frontside metal

traces under CCD

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Backside QE Enhancement Physics

- Several techniques are used to produce high QE with BSI devices
- Surface Charging
  - Chemisorption Charging (ITL)
  - Flash gates and UV flooding (Janesick)
- Internal Charging
  - Implant and anneal (most common commercially)
  - Delta Doping (see Shouleh's talk today)

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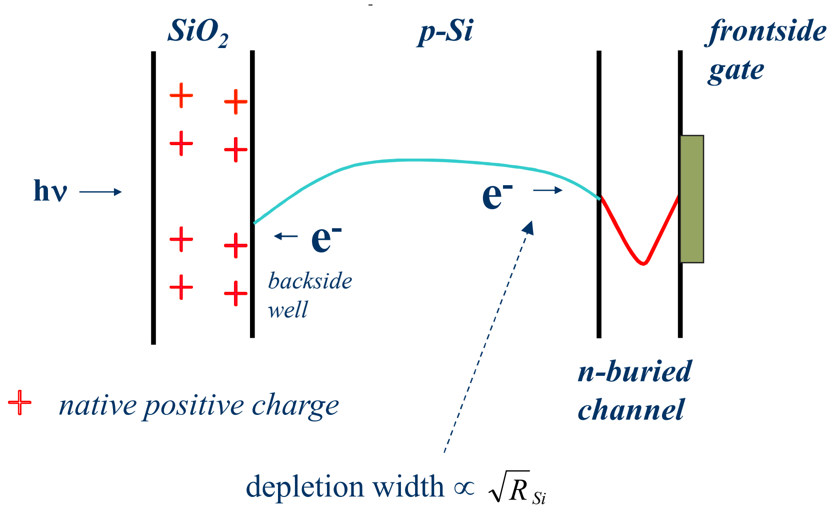
Backside Illumination Potentials



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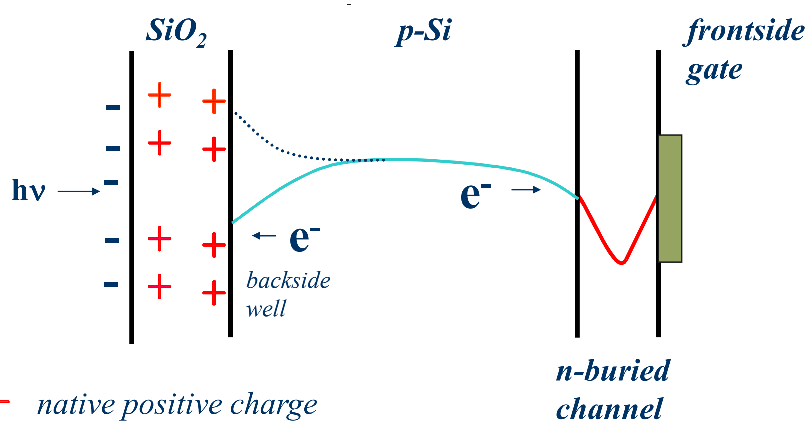
Surface Charging



+ *native positive charge*

- *desired negative charge*

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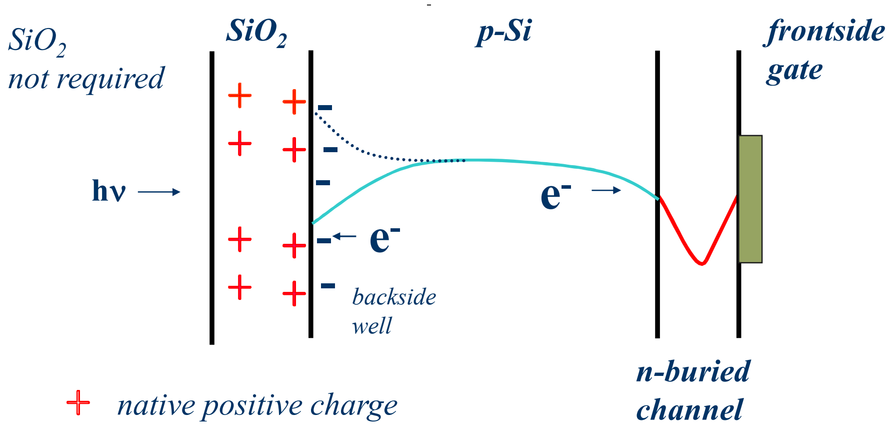
Internal Charging – most common



+ *native positive charge*

- *desired implant*

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Chemisorption Process Steps

- Oxidize backside of thinned CCD to reduce interface trap density
- Apply thin metal film (10A silver) to promote negative backside charge
- Apply antireflection coating optimized for spectral region of interest

low temperature oxidation chamber

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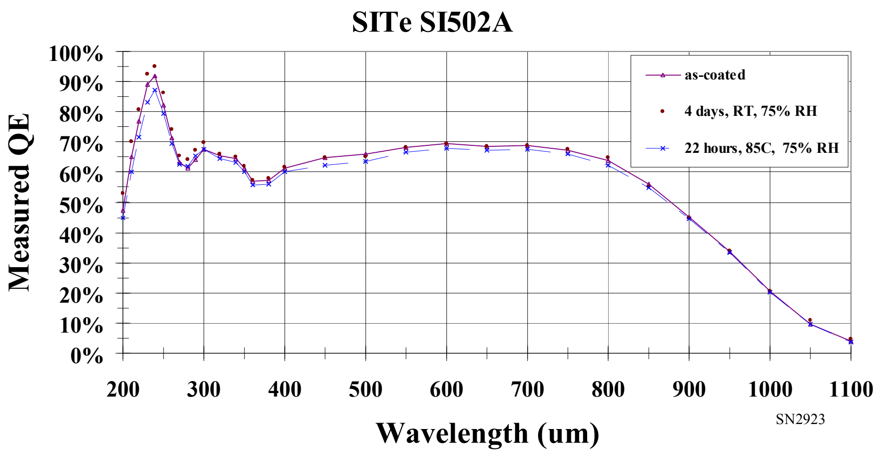
QE Stability Critical



QE Stability should be tested for all backside processes
QE vs. time, environment, and temperature

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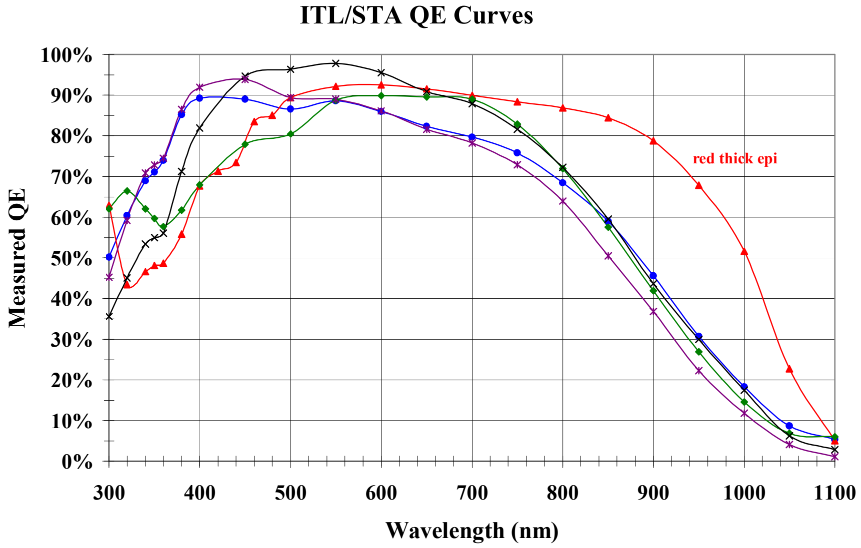
Antireflection Coatings

- Optimize QE for application
- Broadband applications require multiple layers
- UV difficult as need high index, low absorbing materials
- Some materials are radioactive!
- Common silicon BSI AR materials
  - Hafnium oxide, magnesium fluoride, SiO, SiO_2, Ta_2O_5

Typical Visible QE



Recent BSI Detector Progress

- Bigger and bigger devices
  - 10kx10k CCDs (1 die per wafer)
- Orthogonal Transfer Arrays (OTA)
  - WIYN ODI, PanStarrs
- Extended spectral response
  - UV (193 nm and below), X-ray, direct electron bombardment
  - 800 – 1000 nm QE > 80%, reduced fringing

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Recent BSI Detector Progress

- Extremely tight mechanical specifications
  - 5 um peak-valley flatness
- Large mosaics with buttable detectors
  - ~100 devices now, 200+ in next few years
- CMOS imagers
  - on-chip logic, lower voltages and power, radiation hard, recent low noise results

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Detector Characterization

- Careful characterization is critical for BSI scientific imagers
- Most scientific devices are cooled (-40 to -120 C) for reduced dark current during long exposures (1-30 minutes)
- Important parameters are QE, noise, dark current, photoresponse uniformity, cosmetics, MTF, QE stability, and CTE (CCDs)

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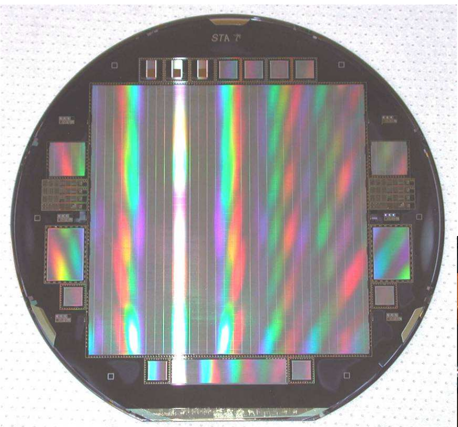
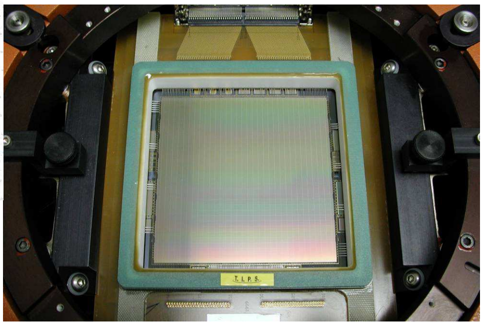
STA1600A 10kx10k CCD



- 1 die per 150 mm wafer
- 9 µm pixels
- 16 high speed outputs
- probing challenge!



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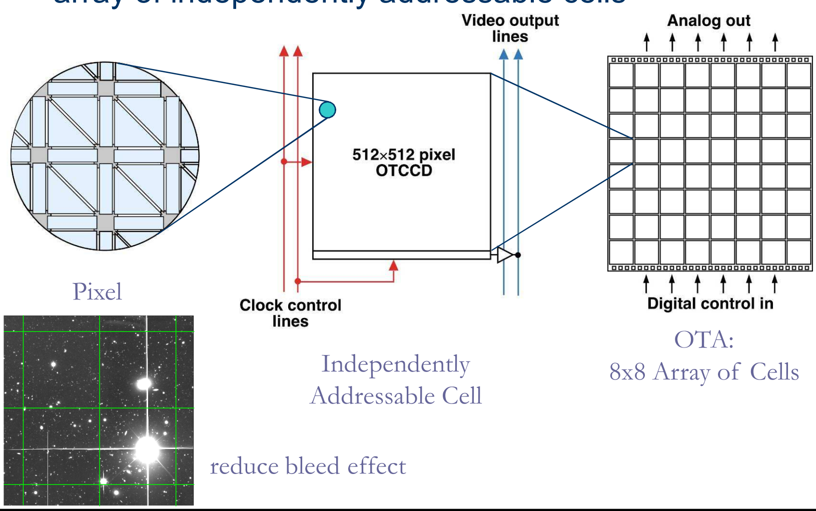
UV Semiconductor Inspection

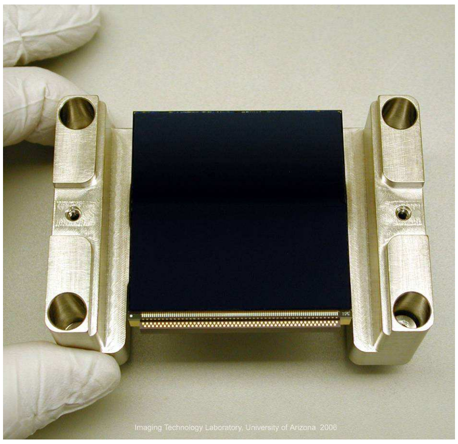
- Detectors are BSI as UV laser illumination required for imaging of submicron line widths
- Laser wavelengths 193.5 nm, 198.5 nm, 257 nm, and 266 nm
- Long-term stability against high intensity UV illumination is required and may be difficult to achieve

The Orthogonal Transfer Array

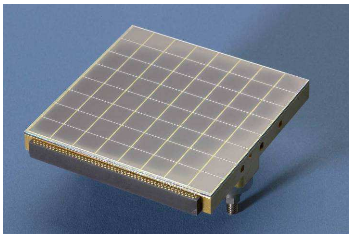
Partition a conventional large-area CCD imager into an array of independently addressable cells



STA1000 OTA CCD



ITL backside device



frontside showing 64 cells

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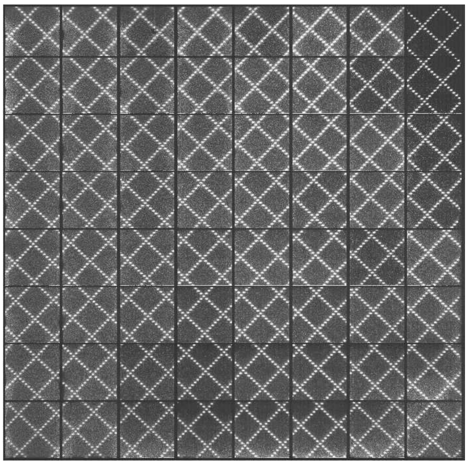
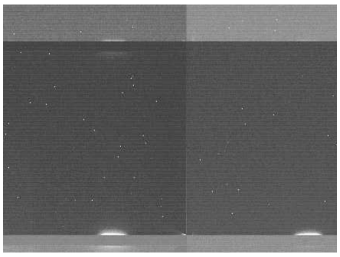
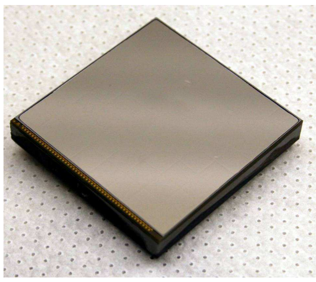
WIYN ODI – STA2200A Backside



grid projection



Fe55



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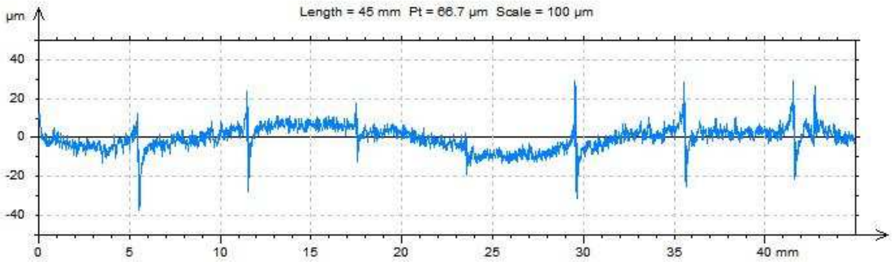
Detector Flatness

- Flatness at operating temperature is critical for many scientific applications
- This BSI device in final package is ~10 μm peak to valley at -100 C, internal structures affect surface profile



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Scientific Imager Read Noise

- Backside read noise is often higher than frontside
- Noise < 3 electrons very important
- < 2 is useful for some applications
  - lowest noise measured at ITL is 1.8 e^- @ 40 kHz for a MIT/LL CCD

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BSI CMOS

- Early ITL CMOS thinning was 1998
- Early devices used very thin epi, difficult to back illuminate without damage
  - latch-up issues
- Typical “CCD silicon” used for CMOS devices can be back illuminated without issue
- QE is the same as for CCDs

See following talks today

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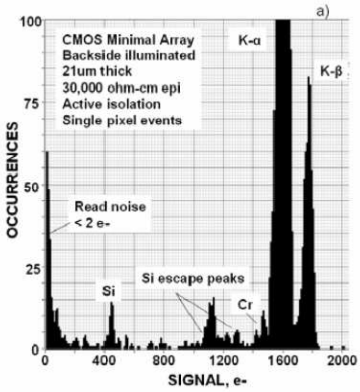
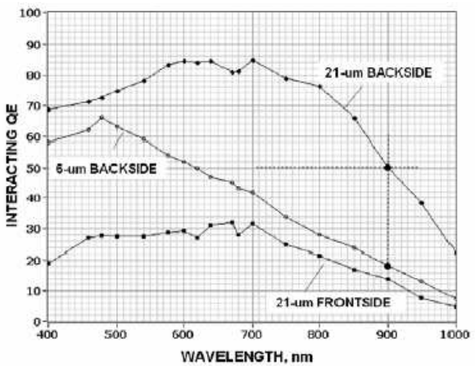
BSI CMOS – Sarnoff/ITL





data from Jim Janesick

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Outlook for Scientific BSI Imagers

- New scientific instruments usually require bigger formats, faster readout, higher QE over broad spectral range, and lower noise detectors
- Commercial trend seems to be toward smaller pixels and very high gain
  - bad for many scientific applications
  - full well capacity (dynamic range) very important
  - large optical components are difficult and expensive to fabricate with very small point spread functions

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Outlook for Scientific BSI Imagers

- Scientific detectors like to remain expensive as typically not in line with commercial trends
- Commercial CMOS BSI processing is growing rapidly and will likely push all costs lower
  - and advance new technologies?

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Summary

- BSI CCD detector technology is well established and well characterized
- Most scientific applications require BSI for QE and spectral range coverage
- Several commercial vendors produce very high quality BSI devices
- R&D BSI CMOS has shown processing can be similar to BSI CCDs
- Commercial BSI CMOS is relatively new and expanding rapidly

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The End

Thank You!