A Four-Side Tileable Back Illuminated, Three-Dimensionally Integrated Megapixel CMOS Image Sensor

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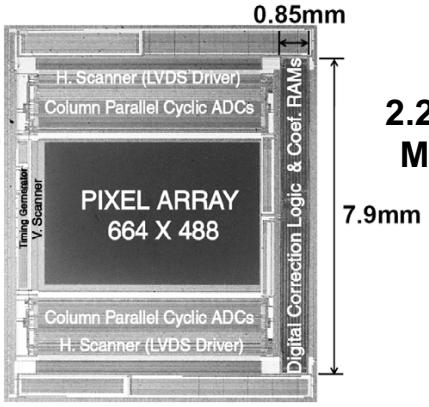
Outline

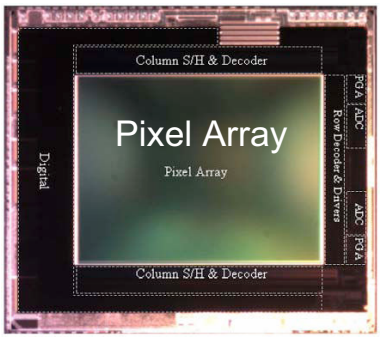
- State of the art and challenges
- 3-D Integration for image sensors
- Tile description
- Results
- Summary

CMOS Image Sensors at ISSCC 2008

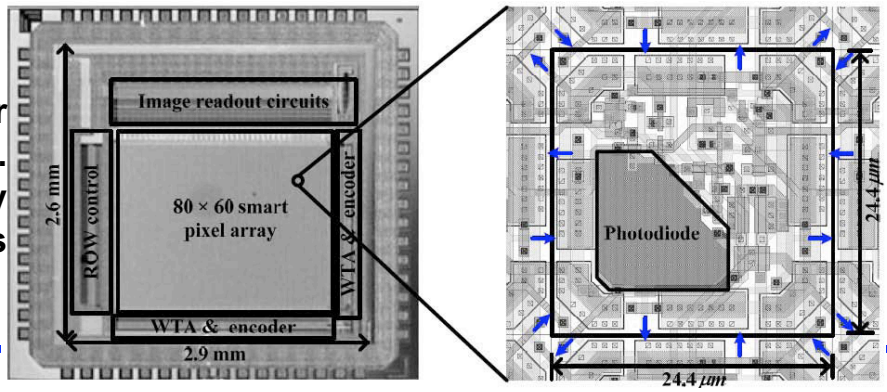
Hamamatsu
Kawahito et al.



Micron
2.2 µm pixels
Moholt et al.



Smart Eye Tracker
Kim et al.
Yonsei University
24.4 µm pixels

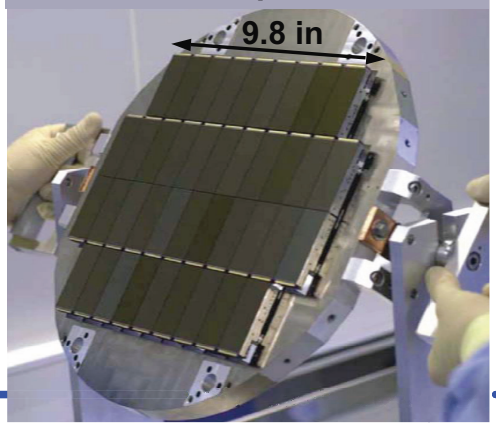


Large CCD Mosaic Cameras

- **Applications:**
  - Wide area persistent surveillance
  - Reconnaissance
  - Astronomy
  - Particle physics
- **Tiled mosaic focal plane arrays:**
  - Large pixel count
  - Exceed wafer size
  - Piece-wise linear fit to spherical focal surface

Canada-France-Hawaii Telescope
(Mauna Kea, HI)

Megacam: 40 e2V CCDs
377 Mpixel



Pan-STARRS Gigapixel Camera

60 Orthogonal-Transfer CCD Tiles
1.35 Gpixels

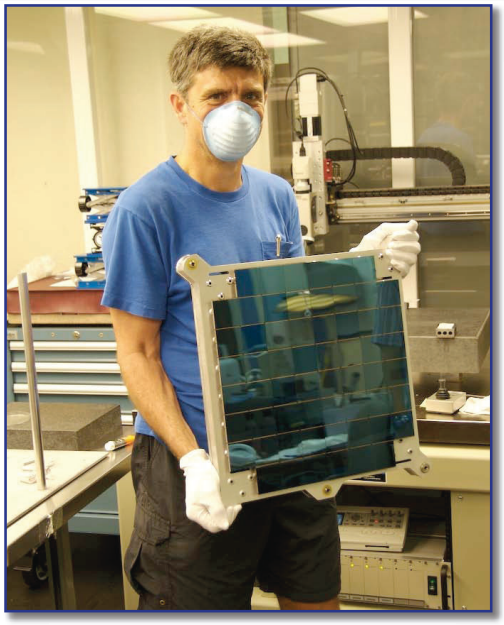
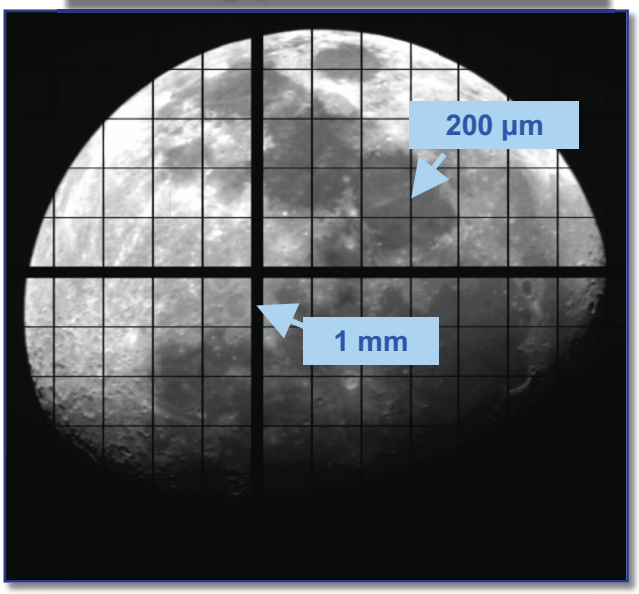


Image from Portion of
Gigapixel CCD FPA

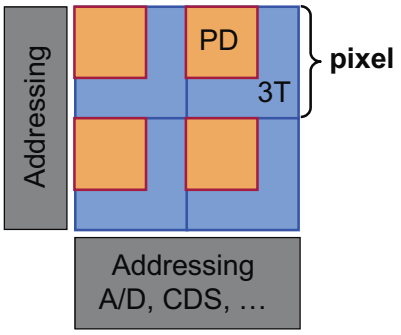


Design Goals and Challenges

- Stacked vertical structure from pixels to connector
  - High quality active pixels close to edge
- Architectural flexibility
  - Potentially radiation hard
  - Minimize pin count
  - Support fast burst data rates
- Removable system connector for testing

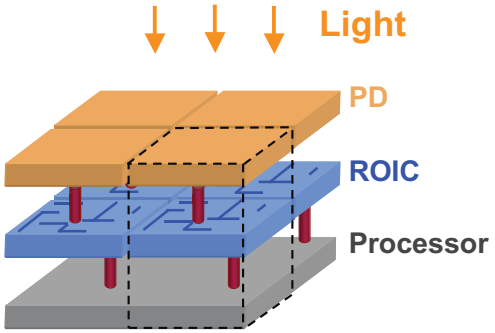
Advantages of Vertical Integration

Conventional Monolithic APS



- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
- Control and support electronics placed outside of imaging area

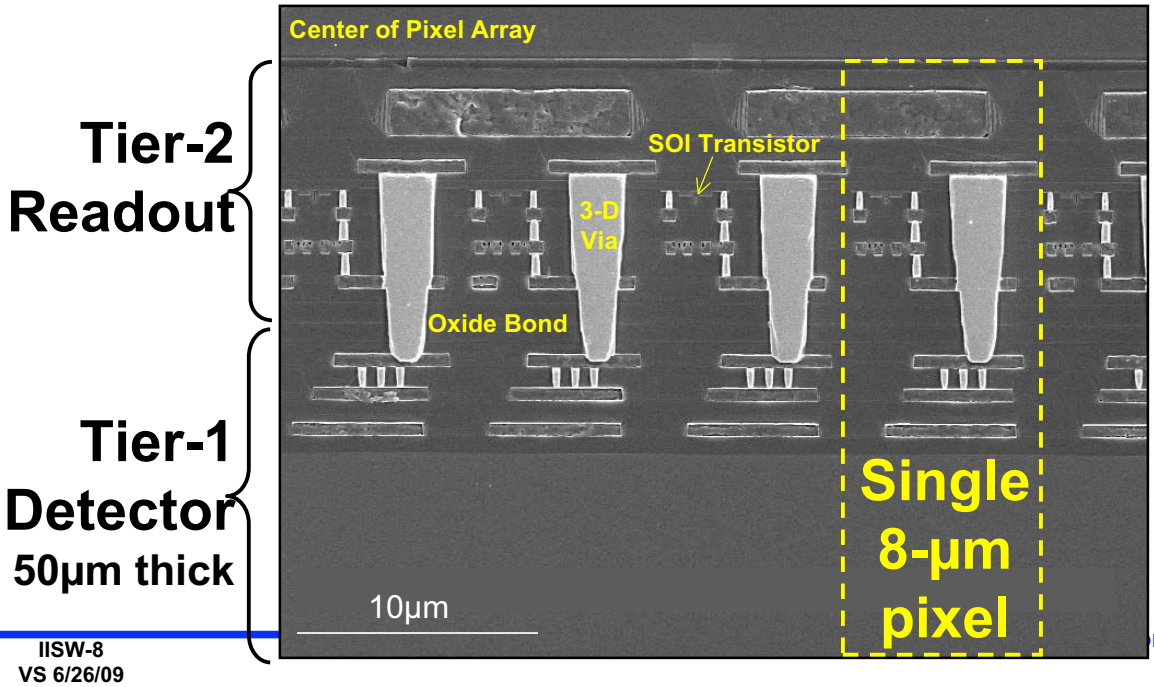
3-D Pixel



- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
  - Power and noise management
- Scalable to large-area focal planes

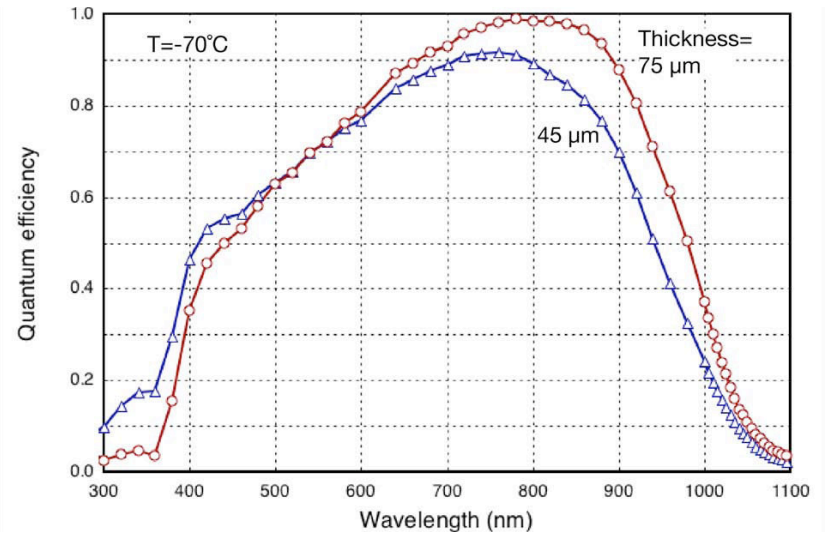
Oxide-Bonded 3D-I Technology

- Smaller pixels than bump bonding
- 100% Fill Factor for Back Illumination



High Near-IR Quantum Efficiency

Weak near-IR photoelectric effect in silicon => thicker silicon



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Tile – Top Level Functionality

Vertically stacked SOI-CMOS Imager

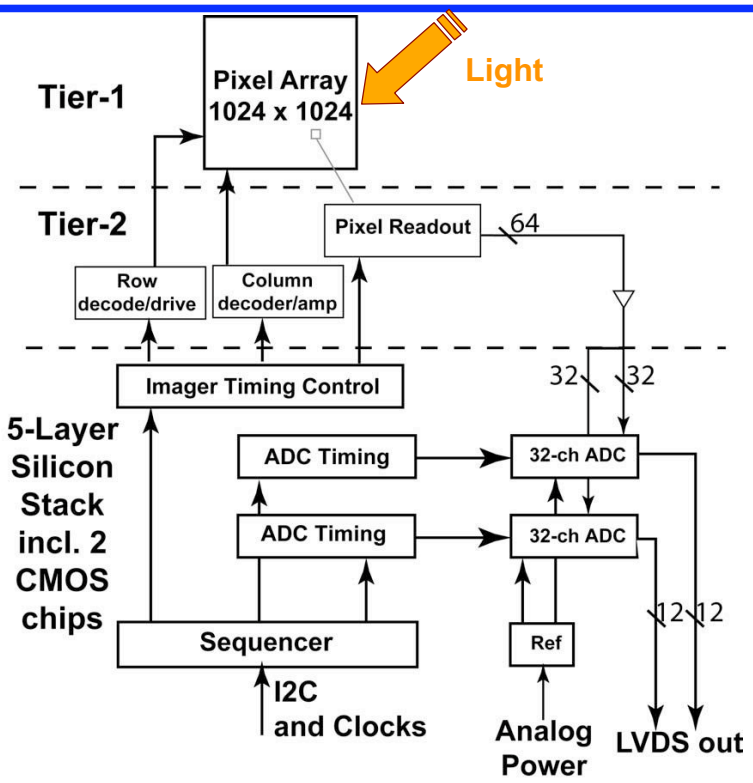
Pixel Array	1024 x 1024 silicon photodiodes
Pixel Size	8.3 μm x 8.3 μm, 100% Fill Factor when Backside Illuminated
Architecture	4-transistor Active Pixel
Electronic Shutter	Charge storage node in pixel
Analog Mux	Pixel output, Row Decoders, Column Decoders
Analog Output	64 output amplifiers, 16 columns per output

ADC/Control Chipset at 10 frames/sec

Analog/Digital Conversion	64, 12-Bit Pipelined ADCs, 1% duty cycle
Digital Mux	768 Bit SRAM
Digital Output	24 Channels of LVDS @ 512 Mbit/sec/channel
Imager Control	Programmable through I^2C serial interface
ADC Control	Programmable through I^2C serial interface
Bias Generators	Programmable Voltage and Current reference through I^2C

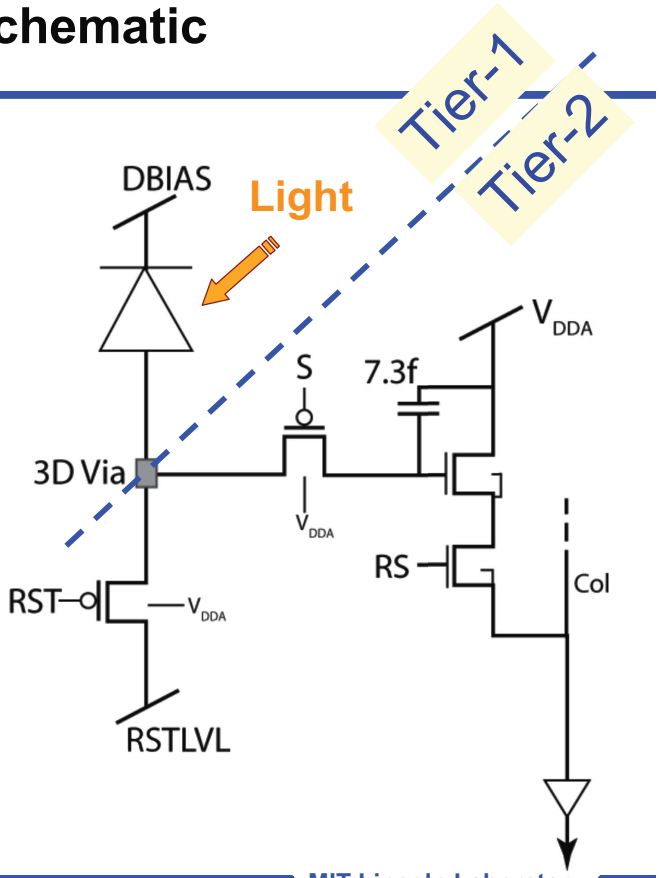
Tile Block Diagram

- Vertically stacked
- Pixel readout on Tier-2
- Timing control in Stack
- 64-ch 12-b pipelined ADC
- Digital output



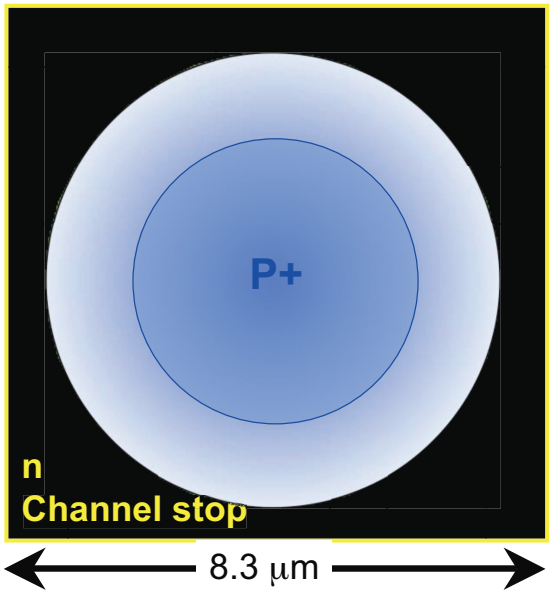
Pixel Schematic

- Global electronic shutter
- In-pixel storage capacitor
- Detector bias through back illumin. process
  - 12V to deplete 50µm detector

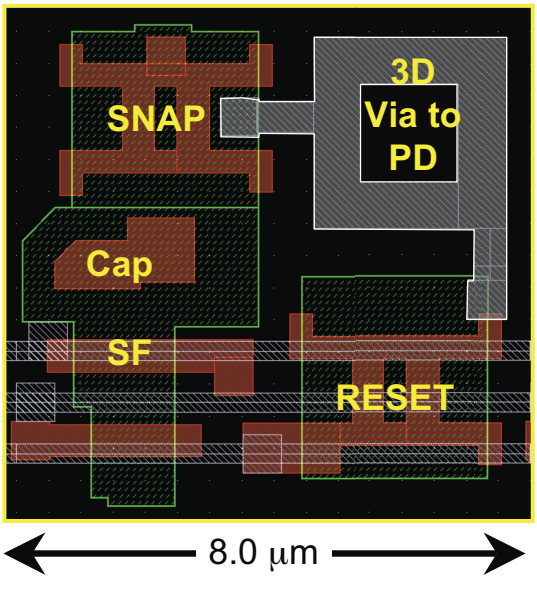


Pixel Layout

Diode Tier-1

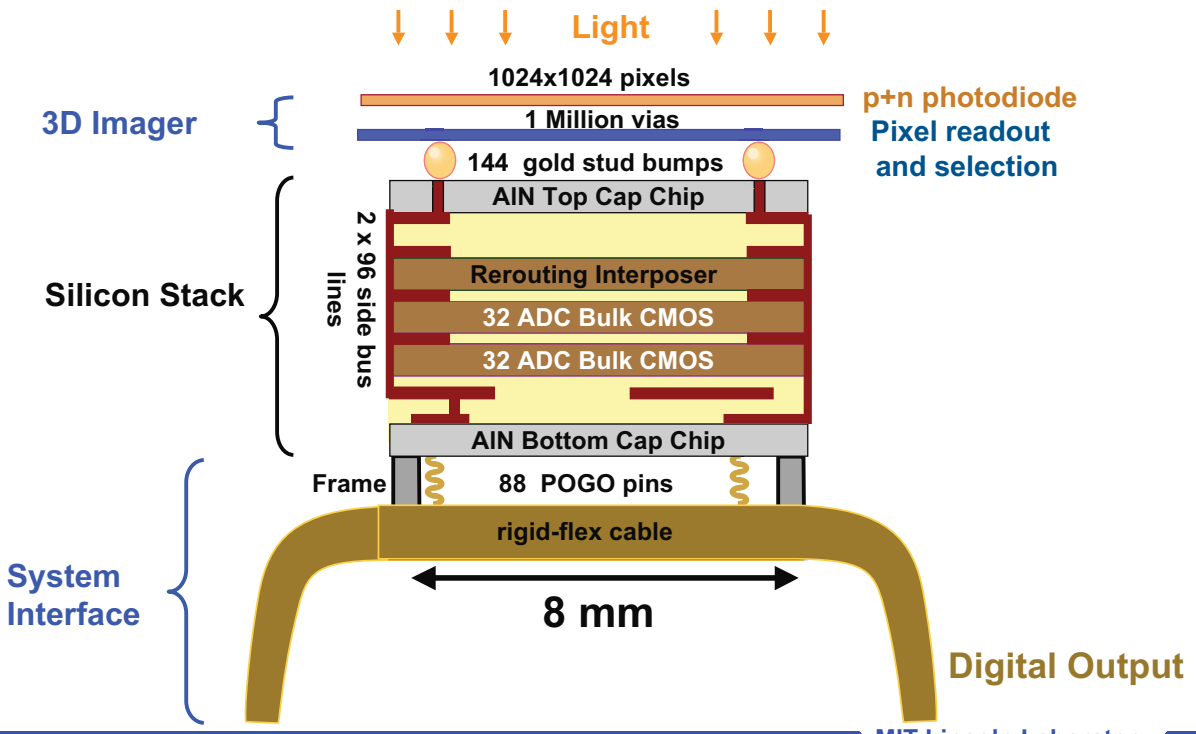


SOI Tier-2

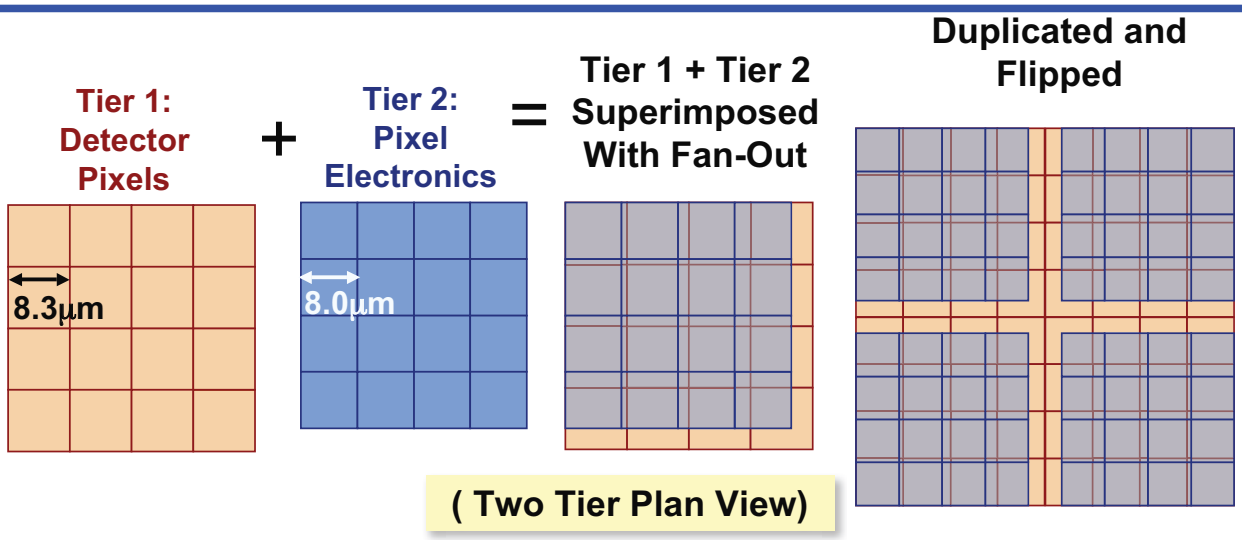


Active Poly Metal

Digital Tile Stack and Signal Flow



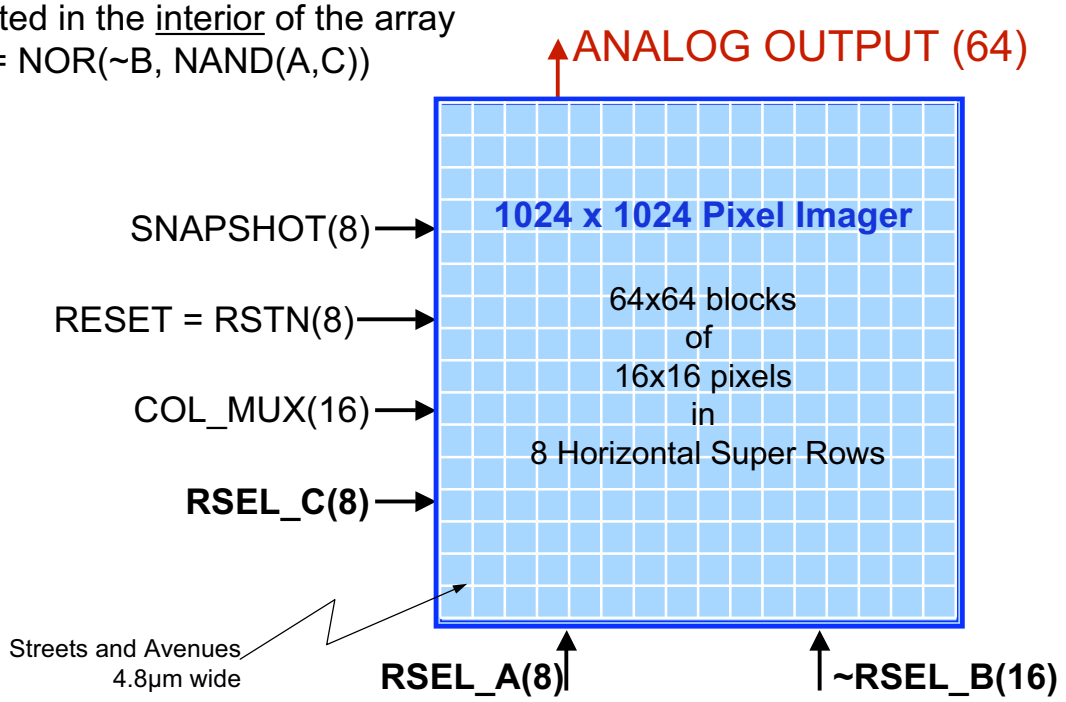
Edge-Free Layout Concept



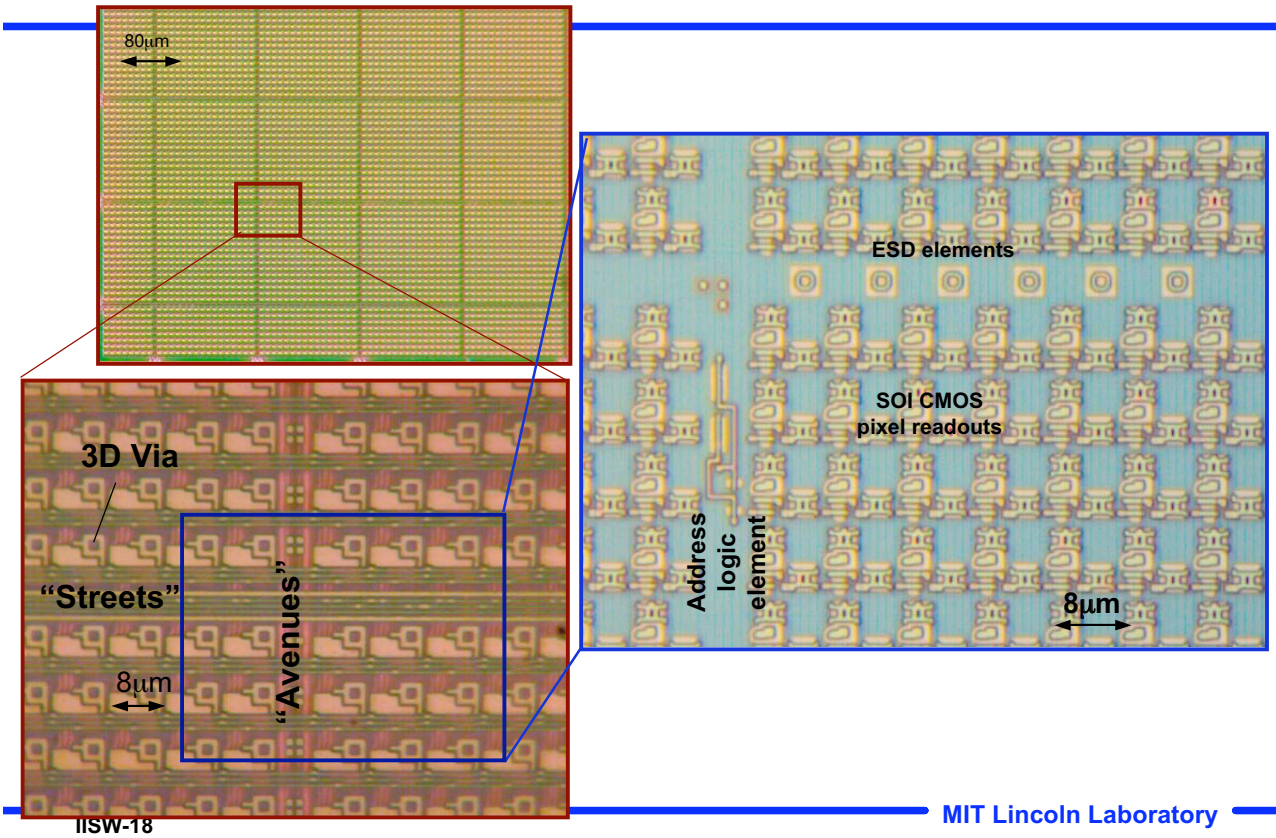
- Tile design driven to minimize perimeter circuitry
  - Active pixel circuit is smaller than the 100% fill factor photodetector
  - Access circuits placed into aggregated excess space

Utilization of 128 Signal Ports

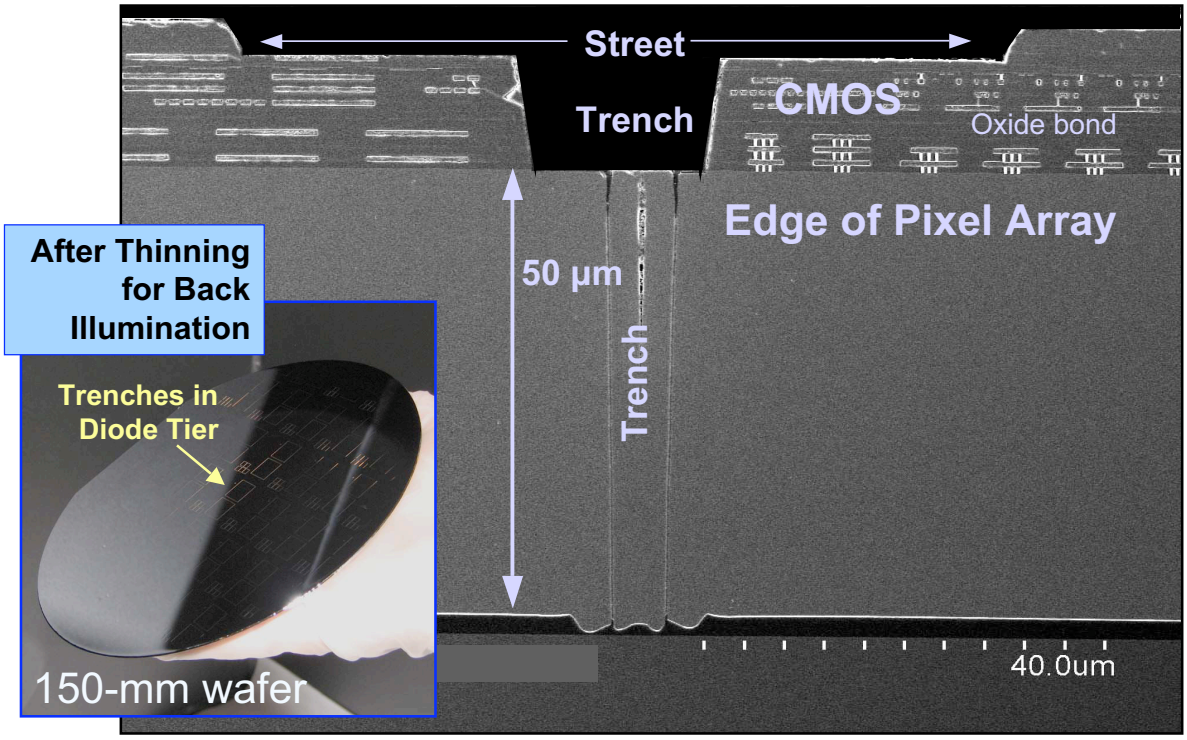
Pixel selection algorithm
implemented in the interior of the array
A*B*C = NOR(~B, NAND(A,C))



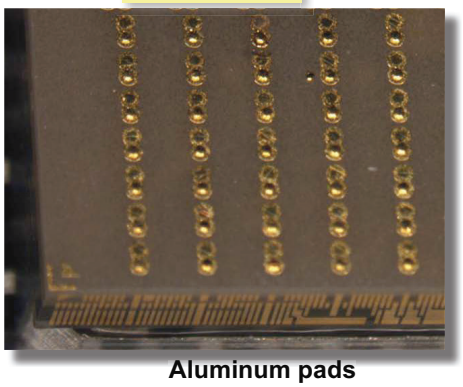
Embedded Control Circuitry in Tier-2

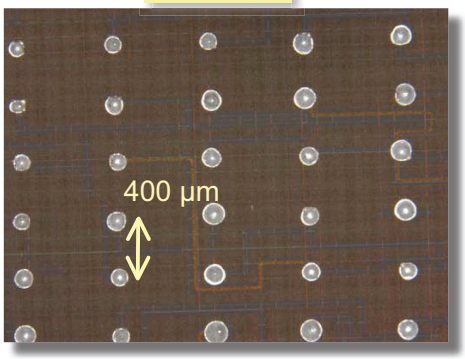


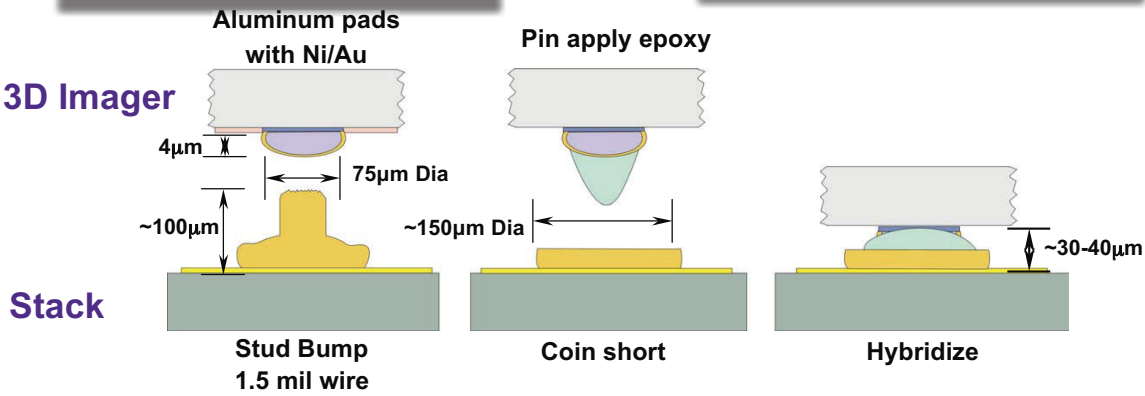
CMOS Circuits Extend to Tile Edge



3-D Integration Through Stud Bumps







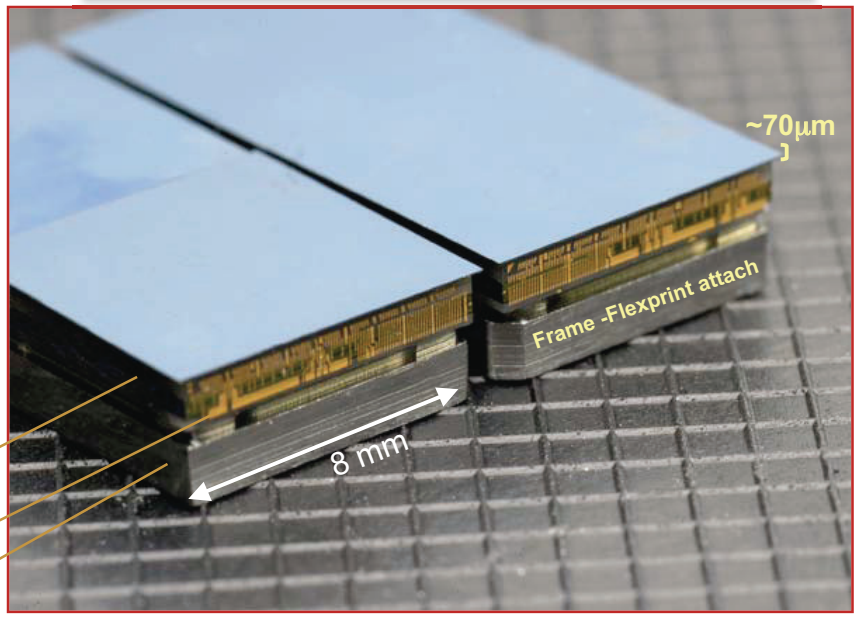
Finished Tile Stack Appearance

Back Illuminated 3-D CMOS Imager
1024 x 1024 pixels
8.3 x 8.3 μm^2 pixel
64 analog outputs

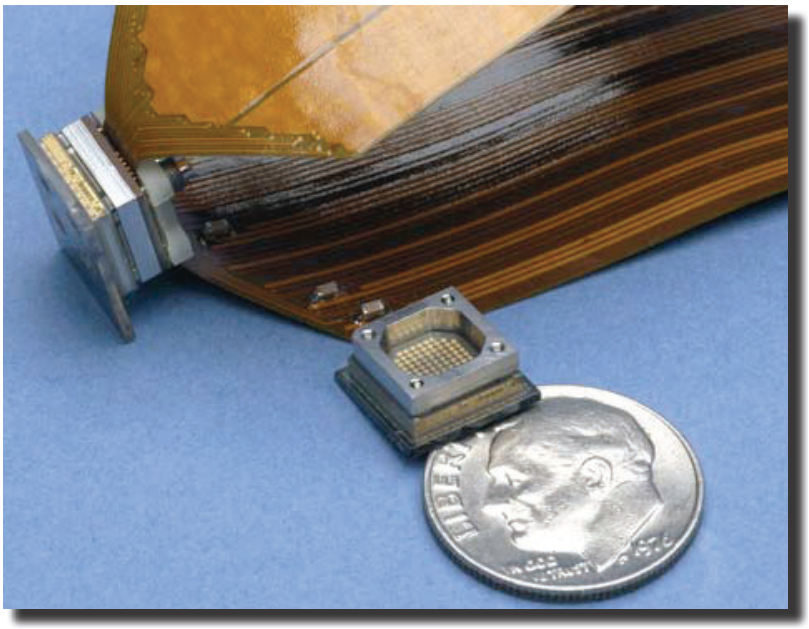
5 layer stack
64 A/D converters
Timing & Control

1024x1024 pixels
>1 Million vias
144 gold stud bumps
2 x 96 side bus lines
88 POGO pins

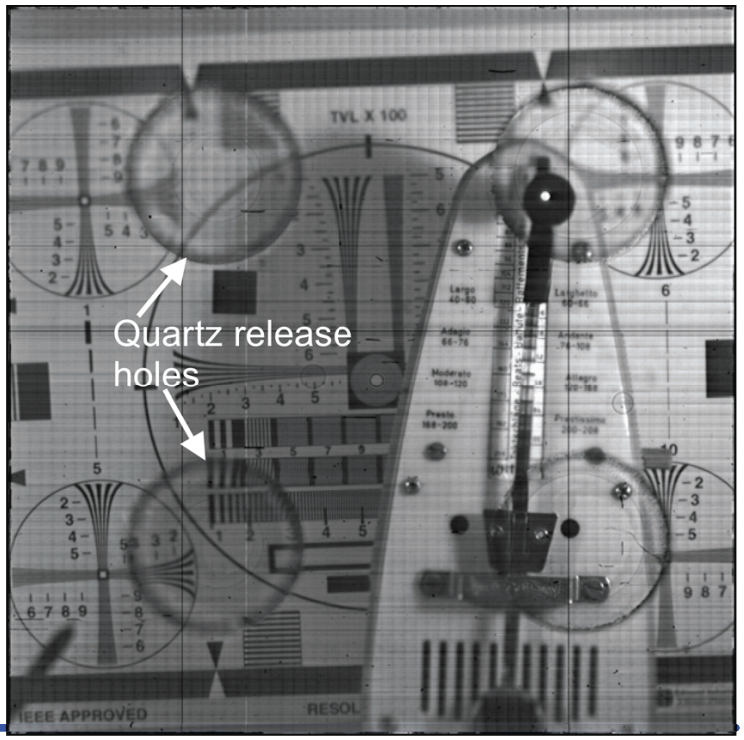
Programmable Digital Imaging Tile



System Connector for Testing



Captured Raw Imagery

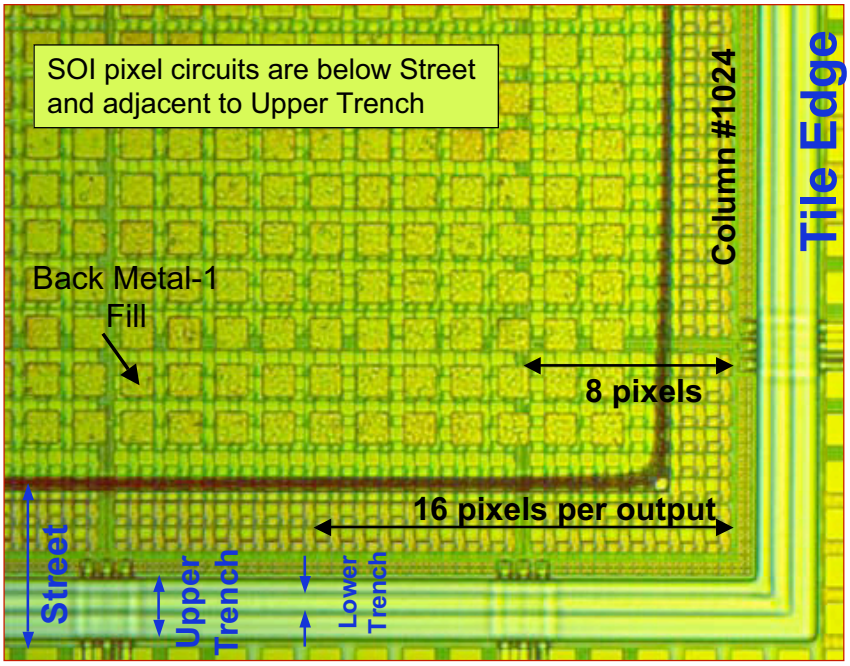


Imagery after FPN correction

(sub-optimal)

Edge Pixel Response

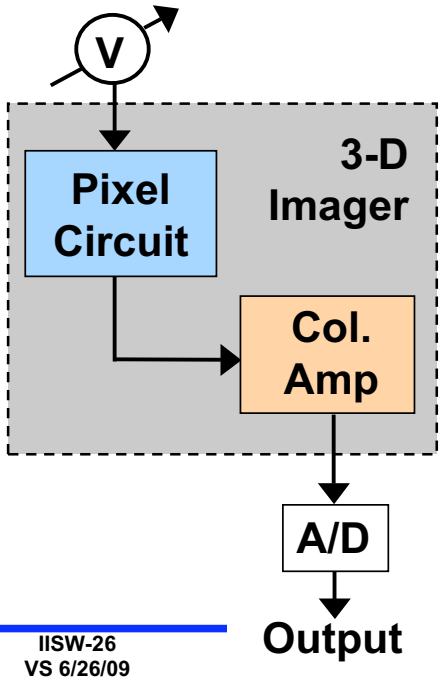
- Last pixel (row 1024) is within a few pixels of silicon edge



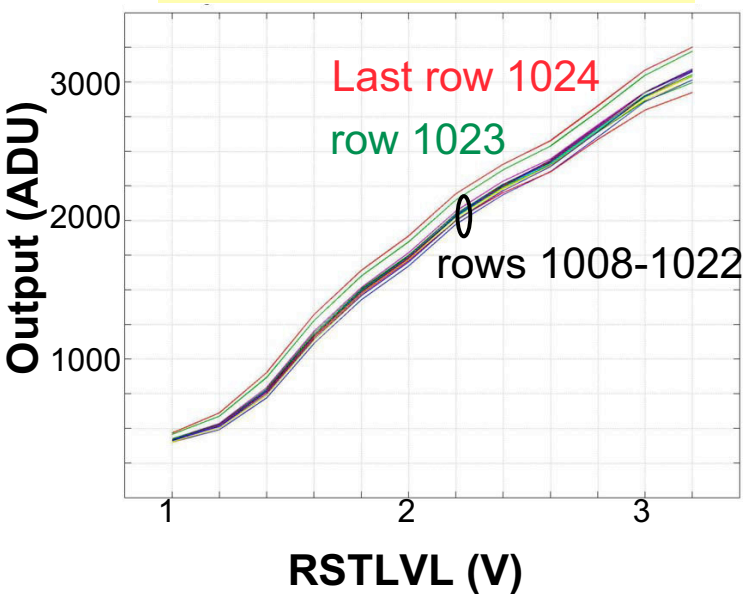
In-Process Photomicrograph: Edge of 3D Integrated Imager

Edge Pixel Response

- Tier-2 SOI CMOS performance
  - Pixel held in reset and RSTLVL swept
  - Linear response expected

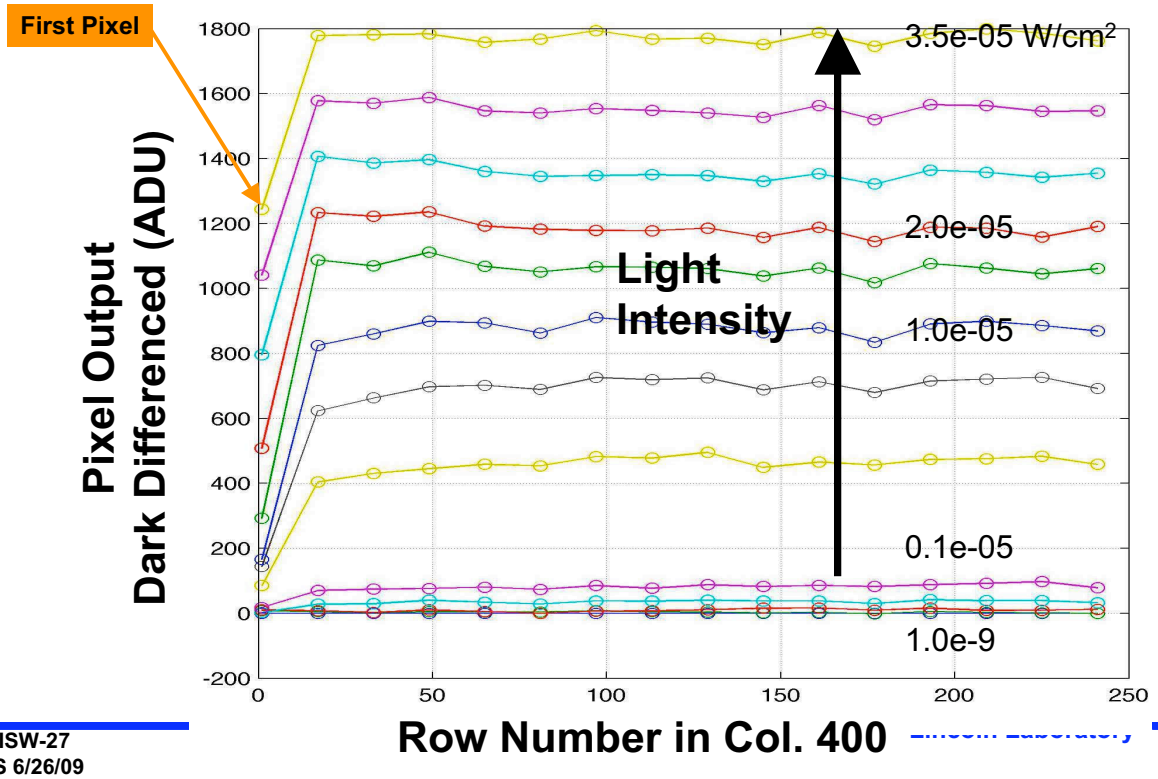


64 pixels in Column 523

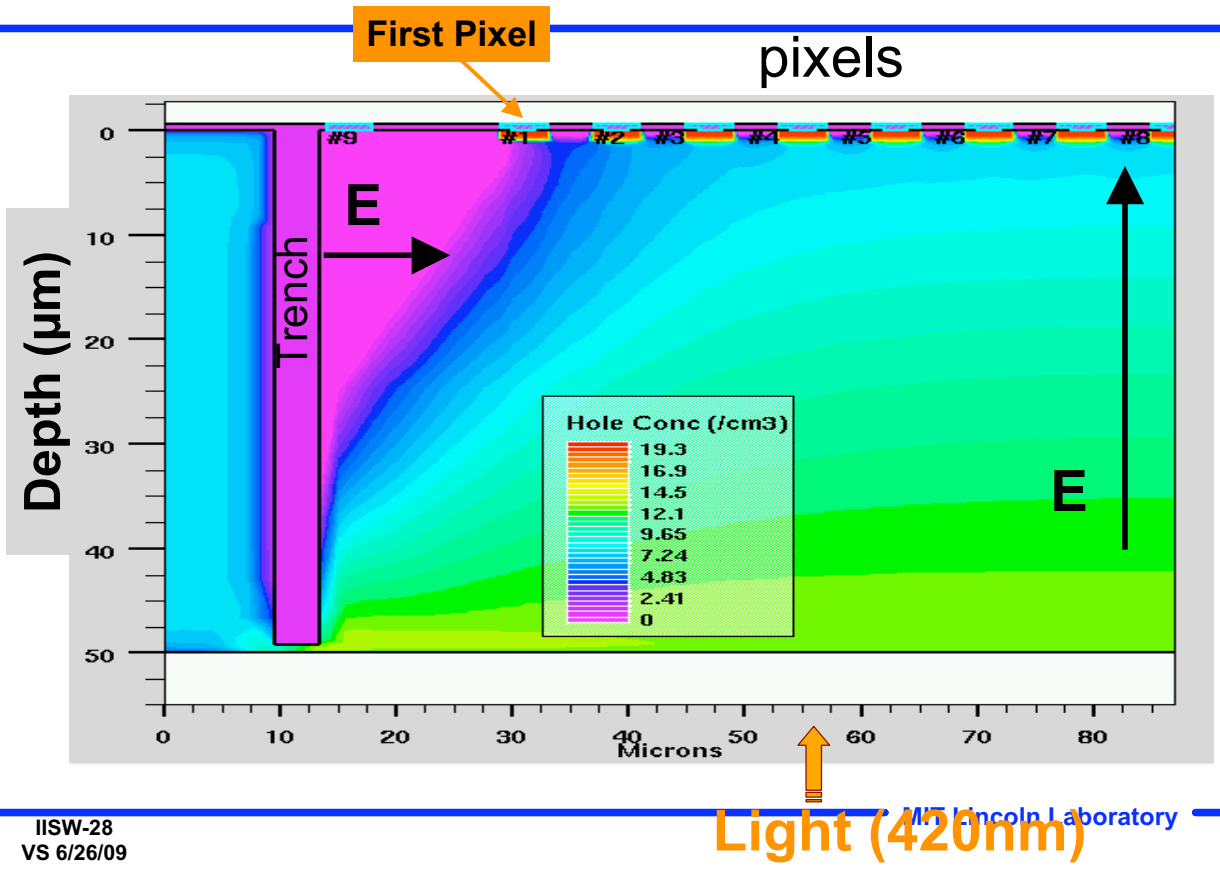


Edge Pixel Response

- Tier-1 Diode Test — Uniform White Light



Edge Pixel Response – Simulation



Physical Summary

Process Technology	**Tier-1: p+n diode in 3000 Ω-cm FZ-Si (Back Illumin.)** **Tier-2: 0.35µm MIT-LL SOI-CMOS 3.3V** **Stack: 0.35µm Tower 2P4M 3.3V Bulk CMOS**
Pixel Array size	**8.5 mm x 8.5 mm**
Chip stack size	**8.0 mm x 8.0 mm x 1.27 mm**
Pixel Array format	**1024 x 1024**
Tier-1: Diode thickness	**50 µm**
Tier-1: Diode pixel size	**8.3 µm x 8.3 µm**
Tier-2: Readout pixel size	**8.0 µm x 8.0 µm**
Pixel Fill Factor	**100 %**
Tile Fill Factor	**99.7 %**
Tile edge to 1st pixel	**Few pixels**

Performance Summary

Parameter	Value
Pixel Type	4-Transistor
Shutter	Global or local electronic shutter
Pixel operability	> 99.6 %
Saturation Voltage	2 V measured (130 ke- est.)
Responsivity	(16 µV/e- est.)
Diode dark current at RT	< 5 fA/pixel @ RT
Pixel temporal noise	5.5 mVrms
Spatial noise	63.4mVrms meas. across array 34.5mVrms meas. within column
Frame rate	10 fps
Digital data rate	512 Mbit/sec LVDS
3-D Imager power	0.23 mW/Mpix/sec
ADC/Control power	6.65 mW/Mpix/sec

Summary

- **3-D IC CMOS image sensor Tile demonstrated**
  - **1024 x 1024 Imager sensor with 8 µm x 8µm pixels**
  - **100% fill factor, back-illuminated, deep-depletion detector layer**
  - **Two-layer, oxide-bonded device**
  - **Per-pixel vertical interconnection to readout circuit**
- **Layout and design targeted four-side tiling**
  - **Pixels extend to Si-edge with 8-µm pitch 3D connections**
  - **CMOS control circuitry embedded within pixel array**
  - **FPN dominate image uniformity**
  - **Edge pixels contribute to image scene and behavior is consistent with simulation**
- **3-D bump-bonded Readout Controller/ADC integrated into Tile**
  - **64-channel A-to-D with LVDS output**
  - **Fast readout of all pixels**
- **Technology is scalable to larger format devices**
  - **Improvements in spatial and temporal noise in design**

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