Stratified Photodiode a New Concept for Small Size-High Performance CMOS Image Sensor Pixels

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ABSTRACT
With continuing trend of pixel size reduction in CMOS Image Sensors from 2.8um through 2.2um down to 1.4um and beyond it becomes increasingly difficult to maintain an adequate pixel charge storage capacity and achieve the required DR and SNR. This paper addresses this problem and describes in detail a solution where charge is collected and stored in two layers located above each other in the silicon bulk in a stratified fashion. An excellent performance is achieved with about 50% well capacity improvement without any penalty of dark current increase. This has been achieved using the pinned PD architecture for both stratified layers and with a careful control of electrical fields. The very low depleted (pinned) voltage, which is typically less than 1.0 V for this structure, allows using high FD voltage swing and this in turn results in an easier and more area efficient design of low noise ADC circuits. The stratified PD is easy to fabricate with high yield, can be incorporated with any 4T pixel readout scheme, and does not require any special clocking or biasing.

INTRODUCTION
CMOS Image Sensors (CIS) have been used in a wide range of applications such as the digital still cameras and cellular mobile phones having clear advantages over the CCDs in terms of low power consumption, on-chip functionality, low cost, and so on [1]. However, as the pixel size shrinks, CIS are facing some limitations in both the low Signal to Noise Ratio (SNR) and Dynamic Range (DR), which leads to a degradation of image quality and reduction of usable full range of illuminations in the real world applications. Both the DR and the maximum SNR can be improved simultaneously by increasing the well capacity of the pixel. The well capacity is represented by the following formula: \( Q_{PD} = (V_{pinning} - V_{blooming})C_{PD} \), where \( V_{pinning} \) is the pinning voltage and \( V_{blooming} \) is the blooming voltage of the pixel. \( C_{PD} \) is the capacitance of the PD. The reduction of \( V_{blooming} \) is limited by the minimum voltage required for stopping the photo-generated electrons from overflowing into the silicon substrate during high illuminations. Therefore, to increase the well capacity of the pixel, \( V_{pinning} \) or \( C_{PD} \) should be increased. However, it is very difficult to increase the charge storage capacitance as the pixel size shrinks, although some progress has been made by introducing the shared pixel concept to maximize the geometrical fill factor [2, 3]. Another problem typically encountered with the pixel size reduction is the image lag due to the increased n-type doping of PD. The higher doping is necessary to compensate for the reduction of full well capacity caused by the smaller PD area. In general, \( V_{pinning} \) is proportionally increased with the increase of the full well capacity. This requires reduction of the maximum voltage swing on the Floating Diffusion (FD) in order to achieve a complete charge transfer of charge stored in the PD. Therefore, to improve or preserve the image lag performance and to obtain higher FD voltage swing resulting from higher full well capacity, \( V_{pinning} \) should not be increased.

STRATIFIED PD CONCEPT DESCRIPTION
In this paper, a new PD structure is introduced as a solution to the above mentioned limitations resulting from the smaller pixel size. The new PD structure, called the stratified PD, has two n-type implant regions located above each other in the silicon bulk in a stratified fashion where charge is collected and stored. The drawing in Fig.1 shows the concept of the stratified PD structure. The surface of the PD is covered with a high p+ doped implant layer similarly as in the conventional pinned photodiode. This is necessary for minimizing the dark current generation from the interface states present at the Si-SiO2 interface. The conventional underlying n-type region is divided in this PD into two n-type regions (DN1, DN2) by a highly doped p+ layer (Insertion-p), which is implanted using an additional mask. The new mask is aligned to the edge of the transfer gate at a distance (X) and overlaps the STI region at the PD edge. The distance X is optimized to minimize the electric field at the interface of the PD with the transfer gate and to provide the electrical connection between the DN1 and DN2 regions. The DN1, the Insertion-p, and a portion of the DN2 are implanted using the same Insertion-p mask. The rest of the DN2 is implanted using the conventional n-type PD mask. The two stratified n-type regions, which are electrically connected through the additional n-type implant, also help to extend the PD depletion depth without any degradation of image lag. In the stratified PD, the Insertion-p layer plays a very important role to increase the full well capacity and to increase the
depletion region depth. The structure can be modeled by two parallel connections of storage sites in a silicon substrate [4]. The Insertion-p layer essentially acts as an electrode between the two n-type PD regions and thus it has to have adequate electrical connections to the channel stop (NCST) p+ doped region and to the surface p+ doped region. The layer also cannot be depleted of holes when the transfer gate is turned on. For these reasons it is fabricated using a relatively high dose p-type implant, which covers both the PD and STI regions. The DN2 region contributes the major portion of the PD capacitance. The DN1 region adds PD capacitance and is formed using high implantation energy of 300keV–500keV with a medium dose. The simulated doping profile in the direction of the Si depth at the center of the stratified PD is shown in Fig.2. The electrostatic potential profiles after 1.0usec from the time when Tx gate is turned on (V_{op} = 2.8V) for the conventional and stratified PDs are shown in Fig.3. This is calculated using the 2D transient simulation. The Insertion-p layer occupies a very small region and does not deplete of holes at V_{op} = 2.8V as indicated by the narrow potential line in Fig.3. The profile also does not indicate any potential barriers for the electron transfer from the PD to FD. This is due to a careful optimization of all implants. Implementation of the PD with extended depletion region is important for minimizing of electrical crosstalk induced by the minority carrier diffusion and for maximizing of Quantum Efficiency (QE). The depth of the maximum potential of conventional PDs has an inverse relation to the maximum Qsat for the minimum image lag performance. So, in general, the high full well capacity and high depletion depth are mutually contradicting requirements. The stratified PD structure makes it possible to overcome this trade-off. The simulation results show the depletion depth of the stratified PD to be 0.3-0.4 um deeper than that of the conventional PD with about 50% improvement in full well capacity. The pixel sensitivity and crosstalk tend to degrade as the pixel size shrinks. The optical diffraction and the minority carrier diffusion are the major contributors to this trend. In order to improve the electrical crosstalk a thinner epi is usually very effective for this purpose. However, the sensitivity in this case is also reduced since both the crosstalk signal and the intended signal are lost. The deeper electrical isolation of pixels can be a solution to this problem, but this suffers from the reduction of PD depletion area in the pixel in horizontal direction and the corresponding loss of saturation well capacity. The increased depletion region of the stratified PD contributes to the improvement of both the electrical crosstalk and the sensitivity at the same time. The electrical crosstalk and the pixel response were simulated using a group of pixels where the center one was illuminated and the adjacent ones were blocked by a metal layer. As shown in the graphs in Fig.4 the total response of the stratified PD is about the same as that of the conventional PD, but the response of the illuminated pixel has a significant improvement in longer wavelengths. This is mainly due to the reduction of electrical crosstalk.

**EXPERIMENTAL RESULTS**

The pixel level performance of the stratified PD pixels was evaluated by characterizing the MagnaChip 2.0 Mega-pixel CMOS image sensor that has 2.2um x 2.2um pixel size and two-way shared pixel architecture. The sensor is being fabricated using the 0.13um technology node. Fig.5 shows the graphs of the measured photon transfer curve for each PD structure. The full well capacity of the stratified PD is approximately 50% higher than that of the conventional PD. Linear Qsat of the conventional PD is about 9800e- and that of the stratified PD is about 14600e- without any help from the pixel bias boosting circuits. Conversion gain is approximately 75uV/e-. The pinning curve of the stratified PD is shown in Fig.6. The curve is obtained from the test structures where the transfer gate bias is swept. V_{pinning} of the stratified PD is about 0.9 V, which is significantly lower than 1.35 V of the conventional PD. The high Qsat and low V_{pinning} of stratified PD improve the FD voltage swing and thus increase the maximum SNR without any degradation of image lag. Fig.7 shows the graph of the photo-electric conversion characteristics of the stratified PD for low light illumination levels. In comparison with the conventional PD the stratified PD shows no difference in the charge transfer efficiency or image lag despite of having much higher full well capacity. Good photo-electric conversion linearity and no image lag suggest that a complete charge transfer is achieved. In Fig.8 the graphs of the dark signal distribution for the integration time of 100msec and 450msec are compared for the conventional and stratified PDs. The temperature of the test is 60°C. The hot pixel count of the stratified PD is lower than that of the conventional PD although the maximum levels are the same. The reduction in hot pixel count results in the improvement of the average dark current. The measured dark current is 103e-/sec@60°C for the stratified PD and 125e-/sec@60°C for the conventional PD. This improvement is mainly due to the reduction of high electric fields at the boundary of the PD and the transfer gate and the presence of the high dose Insertion-p layer, which strengthens the isolation between the n-type PD and STI. Fig.9 shows the graph of measured spectral response of the conventional and stratified PDs. As it is expected from simulations, the wider depletion region of the stratified PD results in a lower crosstalk with enhanced quantum efficiency particularly in the longer wavelength region. The measured overall crosstalk of the stratified PD is approximately 4% lower than that of the conventional PD. The improvement of QE for each B/G/R is approximately +1% / +2% / +3% respectively.

The key optical and electrical characteristics of the conventional and stratified PDs are summarized in Table I.
CONCLUSIONS

In this paper, we have introduced a new PD structure called the stratified PD as a solution to overcome the limitations of small size pixels. High full well capacity, improved SNR, very low $V_{\text{pinning}}$, and low crosstalk performance were achieved simultaneously without any degradation of dark current and image lag performance.

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REFERENCES


Fig.1. Schematic diagram of the stratified PD structure

Fig.2. Doping profile at the center of the stratified PD

Fig.3. Electrostatic potential profiles after 1.0usec from the Tx turned on for a Conventional PD and Stratified PD

Fig.4. Simulated pixel response and electrical crosstalk (Conventional PD_CPD vs. Stratified PD_SPD)
Fig. 5. Measured photon transfer curves for the conventional PD and for the stratified PD.

Fig. 6. Pinning curve for the stratified PD.

Fig. 7. Photo-electric conversion under low illumination.

Fig. 8. Dark signal distribution @ Temp = 60°C.

Fig. 9. Measured spectral response of conventional and stratified PD.

Table I: MagnaChip 2.2um 2 Mega pixel sensor key optical and electrical characteristics.

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<tr>
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<th>Conventional PD</th>
<th>Stratified PD</th>
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<tr>
<td>G Responsivity (FD)</td>
<td>~650 e-/lux/sec</td>
<td>~850 e-/lux/sec</td>
</tr>
<tr>
<td>Quantum efficiency (G)</td>
<td>35%</td>
<td>37%</td>
</tr>
<tr>
<td>Pixel capacity (linear range)</td>
<td>9800 e-</td>
<td>14800 e-</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>39.9 dB</td>
<td>41.6 dB</td>
</tr>
<tr>
<td>noise floor @max gain</td>
<td>6e-</td>
<td>6e-</td>
</tr>
<tr>
<td>Pixel dynamic range</td>
<td>64.3 dB</td>
<td>67.7 dB</td>
</tr>
<tr>
<td>Dark current (60°C)</td>
<td>125 e-/sec</td>
<td>183 e-/sec</td>
</tr>
<tr>
<td>Pinning voltage (V)</td>
<td>1.35 V</td>
<td>0.9 V</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>75 uV/e- (Cfd = 2.15 fF)</td>
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