Dynamic Quenching for Single Photon Avalanche Diode Arrays

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SUMMARY

We propose the use of dynamic circuits for quenching avalanche events in single photon avalanche diode (SPAD) arrays. Two area-efficient, circuit solutions are presented in 0.35µm CMOS technology. These circuits contain no passive elements and consume shoot-through current only at triggering instants. The resulting reduction in power consumption and supply noise is essential to formation of large imaging arrays of SPADs.

I. INTRODUCTION

The quest for low-cost, high-performance SPAD arrays with integrated on chip signal processing for both time correlated and uncorrelated applications is now being driven by emerging markets such as biotechnology, automotive and 3D-imaging. Demand for increased accuracy and time resolution is shifting the focus of research from passive to active detector quenching mechanisms. This is due to the requirement that the two primary noise sources in single photon imaging systems, dark count rate (DCR) and pulse jitter be minimized. The former results in false triggering or arrival events while the latter causes ranging errors in 3D imaging systems. Both noise sources require averaging which is expensive in die area and processing speed.

Quenching is the process of halting a detector's avalanche breakdown and priming the device ready for the next photon arrival, and may be done passively[1], actively or a hybrid approach[3-8]. Active quenching employs feedback to improve system linearity due to the reduction of after-pulsing probability as well as reducing power consumption and crosstalk[3]. Quenching circuits with passive elements suffer from static consumption during quenching which is particularly undesirable for a large imaging array.

In this paper we present two circuits which exhibit purely dynamic power consumption ensuring reduced supply noise and SPAD self-heating effects. In the solutions presented here the detector is effectively isolated from the supply, thus reducing the potential for nonlinearities introduced by variations in excess bias voltage or inter-device crosstalk

II. QUENCH CIRCUITS

Various integrated quench circuits are proposed in the literature:
Most quenching solutions attempt to minimize the avalanche current duration due to self heating, afterpulsing probability and crosstalk issues [3].
A passive quench approach is employed in [2] using a MOS transistor for compactness. Passive quenching suffers from long recharge time. Such methods consume power for the duration of this period, and therefore can suffer self heating effects and longer dead times. In large uncooled detector arrays this may dramatically increase DCR.
References [3],[5] discuss hybrid approaches for larger single detectors, utilising a passive quench resistor and monostable based active quench/reset control. This circuit would be unsuitable for large arrays due to decreased fill factor and power consumption.
References [4], [5] [6] begin to introduce the concept of using the basic CMOS thyristor [2] in a SPAD based detector concept, with logic control being done externally. Again a hybrid quench approach is used.
Reference [7] utilises a passive/active quench hybrid with fixed built in delay active reset, although the active reset path uses some passive components so may suffer from higher power consumption.
Reference [8] has no passive elements and a feedforward active avalanche control, but consumes static current for the duration of the breakdown pulse and requires external logic for precharging.
Most work on integrated quench circuits apart from [1,6] addresses single detector systems. In general these are unsuitable for arrays of detectors with fully integrated readout and programmable active quench mechanisms where low power consumption and high fill factor is of primary concern.

III. OPERATION

The quench circuit proposed in this paper is based on a CMOS thyristor delay cell approach[3], the basic building block of which is shown in Fig. 1.

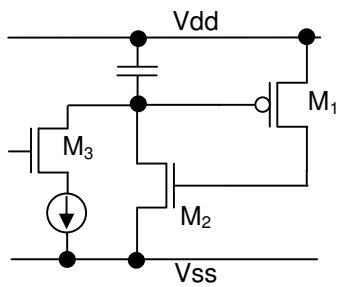

Figure 1: CMOS Thyristor Delay Cell

Referring to Fig. 2, the power supplies are *Vop* at the magnitude of the reverse breakdown voltage of the SPAD structure, and *Vdd* of magnitude of the excess reverse

breakdown (*Ve*) voltage selected to satisfy photon detection probability (PDP) and dark count rate (DCR) specifications. Under quiescent conditions *midpoint* and *Vcathode* nodes are high impedance and power consumption is minimized. When the detector fires the positive feedback loop of M_1 and M_4 promotes the discharge and clamps the SPAD cathode to 0V. A delay time later the latched condition is reset via the dominant drive strength PMOS M_3 and disabled through NMOS M_2. Capacitive elements are MOS gates thus providing a purely CMOS transistor solution. Simulation results are shown in Fig. 3.

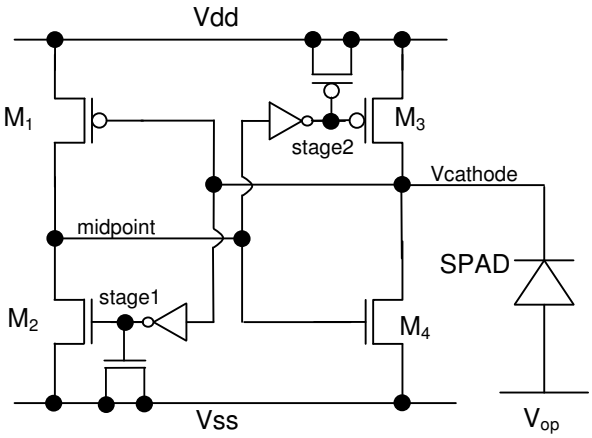

Figure 2: Dynamic Quench Circuit A

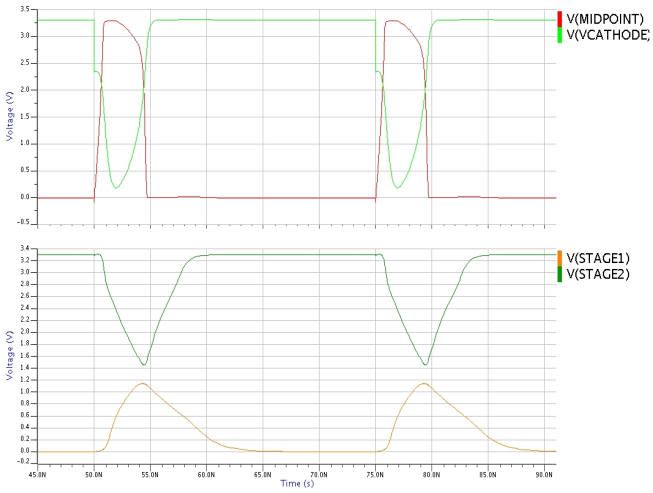

Figure 3: Simulation Results for Circuit A: two consecutive detector firings.

Alternatively, Fig. 4 shows a development of Fig. 2, still using the feedforward principle but employing an unbalanced threshold inverter delay chain which provides a well defined quench pulse duration but a fast subsequent reset. Using such a scheme also provides opportunity for integrating enable/disable and global pulse duration adjustment functions via the introduction of appropriate logic and current starved inverters respectively.

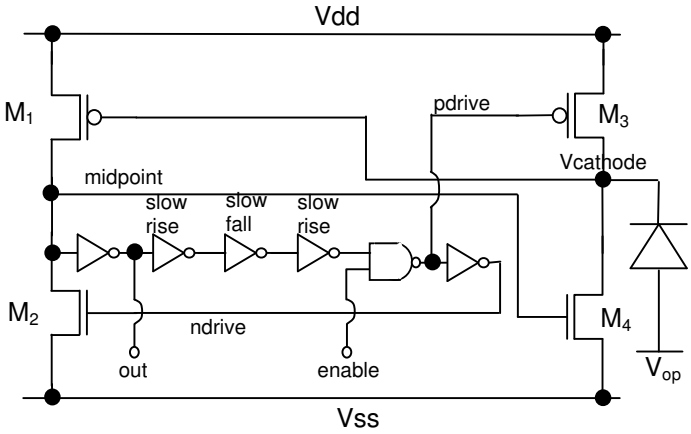

Figure 4: Dynamic Quench Circuit B

Simulation results for circuit B are given in Fig. 5. The circuit operation has been verified over all process corners from -30 to +70°C.

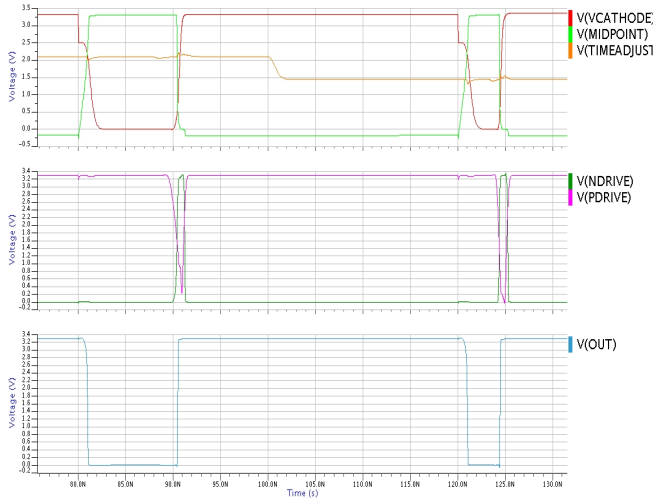

Figure 5: Simulation Results for Circuit B: two detector firings with different quench times

IV. Effects of Leakage

We omit a quench resistor altogether relying on the dominant subthreshold leakage of PMOS M_3 over NMOS M_4 to maintain the SPAD at a high potential between avalanche events (~8:1 width). Similarly, the M_2/M_1 sizing relationship (2:1 width) contributes to correct quiescent potential on node *midpoint* so avoiding erroneous leakage induced triggering. The charge injection on the *Vcathode* and *midpoint* nodes via control signals *pdrive*/*ndrive* respectively is also in the correct sense to provide gate overdrive on the M_4 pull-down and M_1 pull-up devices to minimize sub-threshold leakage in those devices and thus promoting the correct dominant current path. This must be maintained over process corners and temperature. Should the conditions be violated DCR will increase at ~20Hz/pA of unbalance, for our detectors.

Note there is a device sizing trade off between the thyristor feedforward loop delay and the creation of the correct leakage relationships.
A tabulated performance summary is shown in Table 1.

Technology	0.35µm 4ML CMOS
Transistor Count	20T
Area	130µm^2
Supply Voltage	1.7 - 3.6V
Power Consumption	60µW average @ 25MHz firing rate.
Quench duration	2 – 30ns
Arming (enable) Time	300ps
Feed fwd trigger time	100 - 500ps

Table 1: Circuit B Performance Summary

V. Circuit Implementation

A current starved inverter chain is used for the purposes of tuning the quench delay time. The basic slow rise-fast fall cell used in the delay generator is shown in Fig. 6.

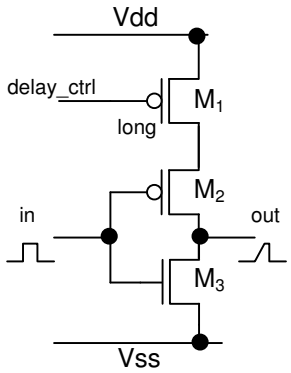

Figure 6: Slow Rise-Fast Fall Current Starved Inverter Cell

The control signal delay_ctrl is used to vary the duration that the SPAD stays in its avalanched state, and hence can be used to set the resolution of event counting in time uncorrelated photon counting mode. It is also known that the quench duration and SPAD afterpulsing are related [3] and so this may be traded off against PDP.

Power Consumption

Disregarding the SPAD recharge consumption, circuit B standalone consumes an average of 60µW from a 3.3V supply at a detector firing rate of 25MHz. This is comparable to passively quenched systems with the advantage of reduced local heating effects plus in built gating and logic output levels.

Layout

The area of circuit B is approximately 130µm^2, and is designed such that large arrays of detectors/quenchers may be formed by abutment, allowing distribution of power supplies and 'global' control signals.

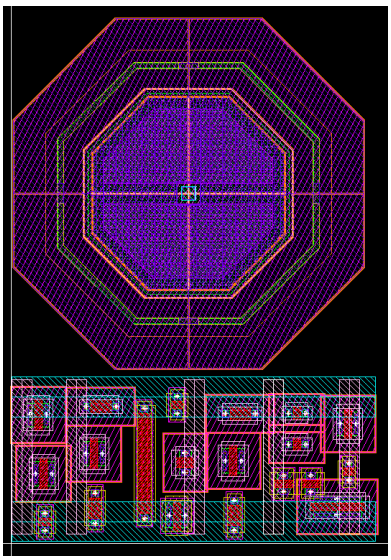

Figure 7: Layout of Circuit B plus Detector

VI. Conclusions

We have reported two novel SPAD active quenching circuit solutions exhibiting advantages over conventional passive/hybrid element approaches, enabling VLSI with detector arrays and on-chip processing for improved performance single photon counting systems.

References

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