Abstract -- The Timepix is a single quantum processing chip capable of event counting, energy or arrival time measurements. The chip contains a 256 x 256 square pixel matrix covering a sensitive area of ~2 cm². It is controlled by an externally applied Shutter. Each pixel can be independently configured in one of four different modes: masked mode: pixel is off, counting mode: 1-count for each signal over threshold, TOT mode: the counter is incremented continuously as long as the signal is above threshold, and arrival time mode: the counter is incremented continuously from the time the first hit arrives until the end of the shutter. The chip uses an external clock with a frequency of up to 100 MHz as a time reference. Each pixel contains a Charge Sensitive Amplifier (CSA) which is sensitive to positive and negative charge, a discriminator with hysteresis and 4-bit DAC for threshold adjustment, synchronization logic and a 14-bit counter with overflow control. The pixel cell contains ~550 transistors, its dimensions are 55 x 55 μm² and the static power consumption is 13.5 μW per pixel. First measurements result in a sensitivity for a signal down to 750 e⁻ corresponding to 2.7 keV energy deposition in a Si sensor.

I. INTRODUCTION

The Medipix2 hybrid imager [1] has shown great potential in a range of applications with single quantum processing. When coupled to gaseous electron multiplication grids such as GEM [2] or Micromegas [3] the chip could be directly used to image events initiated by a single electron. The Timepix chip is an evolution from the Medipix2 which allows for measurement of arrival time, such as needed in a Time Projection gas Chamber (TPC), “time-over-threshold” (TOT) and/or event counting independently in each pixel. An external reference clock (Ref_Clk) is used in each pixel to increment the counter depending on the selected operation mode. The chip has the same size, readout architecture and floorplan as the Medipix2 allowing backward compatibility with the existing Medipix2 readout systems [4,5]. The architecture and functional behavior of the Timepix chip are described in this paper together with first electrical measurements and first images.

II. CHIP DESCRIPTION

Figure 1 shows the floorplan of the Timepix chip. To minimize non-sensitive area when butting together several chips, the peripheral circuitry is placed at the bottom of the chip and the sensitive area is placed at the top, with less than 50 μm of non-sensitive area between the last pixel and the chip edge. The sensitive area (top box) is arranged as a matrix of 256 x 256 pixels of 55 x 55 μm² resulting in a detection area of 1.98 cm² (87% of the entire chip area).

The analog part of the periphery contains one bandgap circuit [6] which generates a stable reference voltage for the 13 on-chip global DACs. There are eight 8-bit current DACs, four 8-bit voltage DACs and a single 14-bit voltage DAC which is used for the precise setting of the global threshold. The threshold DAC LSB corresponds to ~25 e⁻. The digital part of the periphery contains all the Input/Output control logic, the IO wire-bonding pads and a 24-bit fused blown register for...
unique chip identification. A full frame contains 917504 bits of data. At 100 MHz the LVDS serial read out takes <9 ms, or <300 µs in parallel through the 32-bit CMOS port. Independent 2.2 V analog (440 mW) and digital (450 mW) power supplies are used. The chip contains approximately 36 million transistors and is fabricated in a commercial 6 metal CMOS 0.25 µm technology.

III. THE PIXEL CELL

Figure 2 shows the schematic diagram of the Timepix pixel cell. Although the cell clearly resembles the Medipix2 pixel it has three main differences: there is only a single threshold with 4-bit adjustment, each pixel can be configured in 3 different operation modes, and the counting clock is synchronized with the external clock reference \( \text{Ref}_\text{Clk} \). As can be seen in Figure 3 the pixel is divided into two blocks. The analog side is made up of a Charge Sensitive Amplifier (CSA) and a discriminator (with polarity control pin) and 4 bit threshold adjustment. The digital side formed by the Timepix Synchronization Logic (TSL), a 14-bit shift register, a overflow control logic, the \( \text{Ref}_\text{Clk} \) pixel buffer, and an 8-bit Pixel Configuration Register (PCR). The PCR contains 4 bits for the pixel threshold equalization, 1 bit for Masking \( (\text{MaskBit}) \), 1 bit for enabling the test pulse input \( (\text{TestBit}) \) and 2 bits for selecting the pixel operation mode \( (P0 \text{ and } P1) \). The pixel cell contains ~550 transistors and the static power consumption per pixel is ~13.5 \( \mu \text{W} \) (in acquisition state and \( \text{Ref}_\text{Clk}=80 \text{ MHz} \)).

The externally applied Shutter defines two working states and is applied to all the pixels of the matrix simultaneously with a precision of ~5ns. If Shutter is high, an external clock is used to shift data from pixel to pixel. Either the 8-bit configuration register (PCR) is programmed or the 14-bit shift register is read out. For the exposure state the Shutter is low and the 14-bit shift register behaves as a linear feedback shift register counter with a single XOR tap with a dynamic range of 11810 counts. During exposure the pixel counter is incremented by the \( \text{Ref}_\text{Clk} \) depending on the settings of the pixel operation mode bits \( (P0 \text{ and } P1) \):

- **Event counting mode \( (P0=0 \text{ and } P1=0) \):** Each event above threshold increments the counter by 1.
- **TOT mode \( (P0=1 \text{ and } P1=0) \):** The counter is incremented continuously while the input charge is over threshold.
- **Arrival Time mode \( (P0=1 \text{ and } P1=1) \):** The counter is incremented from the moment the discriminator is activated until the global Shutter signal is set high.

![Figure 2: Timepix pixel cell schematic.](image)

![Figure 3: Timepix pixel cell layout: 1) CSA, 2) Discriminator with 4-bit threshold equalization, 3) 8-bit PCR, 4) \( \text{Ref}_\text{Clk} \) buffer and TSL and 5) 14-bit shift register and overflow control. Each pixel contains ~550 transistors.](image)

A. **Pixel analog section**

Any charge either positive or negative collected on the octagonal 20 µm width pixel anode is integrated and compared to a global threshold. If the CSA output voltage crosses the threshold the output of the discriminator generates a pulse whose width corresponds to the length of time the CSA output remains over threshold. The CSA follows the scheme proposed by Krummenacher [7] based on a cascaded differential CMOS amplifier. Global DACs control the front end. The CSA output peaking time can be set from 90 ns to 180 ns by the Preamp DAC. The return to zero of a ~10 ke- input charge can be adjusted from 500 ns to 2500 ns depending on Ikrum DAC settings. The DC output level of the CSA is controlled by the Vfbk voltage DAC and it is used to maximize the output voltage dynamic range depending on input charge polarity. Detector leakage currents in both
polarities, of up to 1krum/2 per pixel, are compensated by the feedback loop of the CSA. The amplifier gain in the default DAC settings is ~16.5 mV/keV with a linear voltage dynamic range up to ~50 keV. The CSA output is DC coupled to the discriminator. The discriminator contains an input multiplexer with Polarity control, a transconductance amplifier, four independent selectable current sources for threshold equalization, and a current discriminator with hysteresis. Total analog power is ~6.5 μW and area is 55 x 25 μm².

B. Pixel digital section

The analog output from the discriminator (Hit) is buffered and gated with the Maskbit at the entrance of the Timepix Synchronization Logic (TSL). The pixel operation mode bits (P0 and P1) configure each pixel TSL in three different modes. In the acquisition state (i.e. Shutter is low) the TSL synchronizes the Hit and the Shutter with the Ref_Clk to generate a glitch free counting clock signal depending on the operation mode. The counter is stopped if the number of counts reaches the overflow limit of 11810 counts. The TSL core uses an asynchronous network of SR flip-flops with race-free state assignment designed with controlled initialization. The TSL core is only active when a Hit is present. The pixel digital part contains ~500 minimum-sized transistors and occupies an area of 55 x 30 μm².

C. The reference clock

The Timepix chip uses an externally generated tunable clock reference (Ref_Clk) as counting clock which is distributed throughout the pixel matrix. To reduce the effects of capacitive coupling and to optimize the digital power balance of the Ref_Clk distribution into the full matrix, each pixel includes a minimum-sized inverter to buffer the Ref_Clk to the next pixel up in the column. Furthermore, to minimise the digital coupling and to uniformly distribute the digital power, the Ref_Clk phase is alternated between columns. With a simulated propagation delay of 195 ps per pixel buffer the Ref_Clk is distributed to all the pixels in less than 50 ns. With a Ref_Clk of 80 MHz the measured digital power consumption due to clock distribution into the pixel matrix is ~450 mW.

IV. Threshold Equalization

Threshold equalization is used to compensate the pixel to pixel threshold variations due to local transistor threshold voltages and current mismatches and/or more global effects like chip power drops. This compensation is done by means of a 4-bit current DAC placed in the discriminator chain of each pixel. The current range of this DAC is controlled by the THS global DAC with a LSB range of 0-40 nA. The measured INL of this 4-bit DAC in the full pixel matrix is less than 0.8 LSB. To determine the equalization mask the threshold distribution for each of the 16 threshold adjustment codes is measured. Then the adjustment code is selected for each pixel to make its threshold as near as possible to the average of the threshold distribution mean values. The threshold variation before equalization is ~240 e⁻ rms and after equalization the achieved threshold variation is ~35 e⁻ rms for both polarities. The minimum detectable charge is defined as the smallest input charge which all pixels are able to resolve when the global threshold is set just over the noise. This depends on the electronic noise and the uncorrelated threshold variation. Before equalization the minimum detectable charge for the full pixel matrix of a naked chip (i.e. without sensor material) is ~1600 e⁻ and after equalization is ~650 e⁻ for both polarities. This compares favorably with the ~900 e⁻ measured in Medipix2 [8].

V. Characterization using radioactive sources

Recently the first Timepix chips bump bonded to a 300 μm high resistivity Si sensor became available. An absolute energy calibration of a Timepix chip was realized using X-ray quanta from ¹⁰⁹Cd and a ⁵⁵Fe sources as shown in Figure 4.

![Figure 4: Energy calibration of a Timepix bonded to a 300 μm high resistivity Si sensor. ¹⁰⁹Cd (with 22.1 and 24.9 keV emission lines) and ⁵⁵Fe (with a main 5.9 keV emission line) X-ray sources are used as energy references. On the right figure, the measured calibration slope is ~87 eV per THL DAC step with a full chip minimum detectable charge of ~2.7 keV.](image)

The effective energy threshold is calculated by scanning the THL DAC over the main emission lines of both X-ray sources (i.e. 22.1 and 24.9 keV for ¹⁰⁹Cd and 5.9 keV for ⁵⁵Fe). The pixel matrix is configured in event counting mode in order to exploit the linear response of the measured effective threshold. The measured slope is linear with a gain of ~87.1 eV or, in
electrons, ~24.2 e\textsuperscript{−} per THL DAC step. The minimum detectable charge for the full chip is ~2.7 keV or ~750 e\textsuperscript{−} for this setup. The measured ENC is ~113 e\textsuperscript{−} rms for the chip bump bonded to the sensor which is ~16% higher compared with a naked chip.

VI. FIRST IMAGES

First images have been taken with different pixel operating modes, both collection polarities and detector types. Figure 5 shows a recorded event in TOT and arrival time mode being the chip coupled to a GEM gas gain grid in electron collection polarity (positive input). The image in Figure 6 is realized with a chip bonded to a 300 µm thick Si sensor working in event counting mode in hole collection polarity (positive input).

The TOT functionality has been further explored with a calibrated chip bonded to a Si sensor using a 241Am radioactive source. The 241Am source emits α radiation with an energy around 5.5 MeV together with γ radiation (i.e. photons) with main energy lines at 13.9 and 59.5 keV. Figure 7 shows on the left a full 2D image using a Shutter time of a 100 ms at a threshold of ~3.1 keV (THL=850). Large pixel clusters, with typically ~25 pixels, are the result of the charge deposition by single α particles due to its high energy. The small pixel clusters (1-4 pixels) are the result of the detection of gamma radiation. The 3D plot on the bottom right of Figure 7 shows the charge information measured with the TOT method. The central pixel in the large clusters has typically ~4000 counts which correspond to a pulse width of ~85 µs at Ref\textsubscript{Clk} = 47.3 MHz and Ikrum\textsubscript{DAC}=5. As each large cluster corresponds to depositions of single α radiation of ~5.5 MeV, the measured charge in the central pixels is then ~2.3 MeV or ~635 ke\textsuperscript{−}.

VII. REFERENCES