1.4Gpix/s, 2.9Mpix CMOS image sensor for readout of holographic data memory

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This paper presents a high speed CMOS image sensor for a high-end holographic data storage application. For this emerging application, high performance primarily translates into a high data throughput which requires a high frame rate. A high frame rate requires both a short readout time and a short integration time, which implies high sensitivity. This performance needs to be obtained at a moderate power consumption to limit the self heating of the sensor.
The presented sensor is a high sensitivity image sensor of 1696 by 1710 pixels that operates at 485 fps. The sensor contains 64 on-chip 8 bit ADCs operating at 26 Msamples/s each, resulting in an aggregate pixel rate of 1.4 Gpix/s. The outputs of the 64 ADCs are multiplexed onto 32 LVDS serial links operating at 416 Mbit/s each resulting in an aggregate date rate of 13.3Gbit/s. The sensor is designed in a standard 0.25µm CMOS process and consumes 1.1W in normal operation.

1. Introduction

Contrary to traditional optical data storage devices like e.g. CDROM, that read one bit of data at a time, holographic storage devices obtain a high data transfer rate by reading complete holograms containing over a million bits in a single operation. At the same time they achieve a high storage capacity as hundreds of these holograms can be stored in the same volume of material. Holographic data storage is expected to be a huge step forward in both speed and storage capacity of optical storage devices.

A high speed image sensor is the key component for building such a holographic data reader. The most important specification for the sensor is the high data throughput, which relates directly to the data read throughput of the holographic memory. A high data throughput requires both a short integration time and a short readout time. A short integration time requires high quantum efficiency and a high conversion gain since typically the amount of incoming light is small. A short readout time is obtained by having a high number of parallel readout paths. On the other hand, holographic data storage poses only moderate requirements on the image quality as it is basically reading a binary image.

This paper presents, to our knowledge, the first image sensor that is custom designed for emerging market of holographic data storage. It achieves 485 fps for an array of 2.9Mpix resulting in an aggregate pixel rate of 1.4Gpix/s. Given the massive data rate, the power consumption needs to be kept at a reasonably low level to avoid performance degradation due to self heating. The sensor contains on-chip all required functionality for easy system integration, but stays targeted to its key specification: high frame rate, high sensitivity and low power.

The next sections discuss the sensor architecture, the pixel, the ADC, the high speed serial link and the measurements.

2. Sensor architecture

The sensor is an autonomous system that interfaces with its host through a 10Mbit/s bi-directional serial command interface, a 208 MHz LVDS input clock signal, an output clock signal, a synchronization channel and 32 416 Mbit/s LVDS data downlink channels with an aggregate date rate of 13.3Gbit/s. LVDS is emerging as an interface of choice for image sensors [1,2] since it allows a very high data rate with a limited number of pins. All required clock, control and bias signals are generated on-chip. The incoming high speed clock is divided to generate the different low speed clocks required for the operation of the sensor. The sensor generates all its bias signals from a bandgap reference. An on-chip sequencer generates all the required control signals for the image core, the ADCs and the on chip digital data processing path. The settings of the sequencer are stored in registers that can be programmed through the serial command interface. The sequencer supports windowed readout at frame rates up to 10000 fps. The sensor operates in slave mode where the exposure is triggered by the host.

Figure 1 shows the floorplan of the sensor.

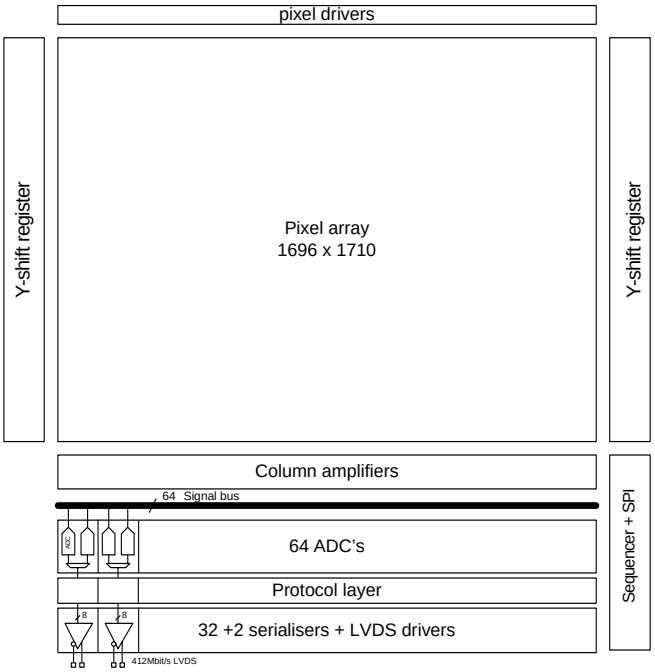

Figure 1: Floorplan of the sensor. The global pixel array control signals are driven from the top, while the high speed read-out related signals are driven from the two sides in parallel. The ADCs and serial links are organized in 32 identical blocks, each containing two ADCs together with the one serial link on which their outputs are multiplexed.

3. 6T pixel

The sensor has 6T pixels with an N-well photo diode and a storage capacitor. Figure 2 shows the pixel schematic.

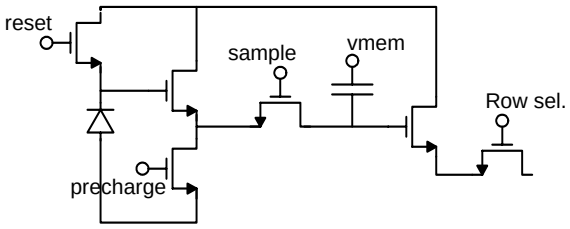

Figure 2: Schematic of the 6T pixel. The pixel consists of an n-well photo diode with its associated reset transistor. The first source follower with its load transistor connects to the storage capacitor through a sample switch. The second source follower connects to the column through the select switch.

The capacitor can sample and hold the photo diode signal for readout at a later time. This type of pixel supports three different operating modes. It allows correlated double sampling in rolling shutter mode, where the reset signal is stored at the beginning of the exposure time and read together with the signal at the end of the exposure time to cancel both FPN and reset kT/C noise. It also allows double sampling in snapshot shutter mode, where the signal is stored at the end of the exposure time and the reset signal is generated during readout to cancel the FPN. The reset kT/C noise is not cancelled as the signal and reset values originate from different reset operations. Finally the pixel supports pipelined snapshot shutter mode where the signal is stored at the end of the exposure time and it is read out single ended, so without reading the reset signal. This mode ensures maximum data throughput as it allows integrating the current frame while still reading the previous frame. A drawback of using a 6T pixel in this operating mode is that there is no on-chip FPN correction. As maximal data throughput is a key specification for the presented sensor, the pixels operate in pipelined snapshot shutter mode.

A key performance measure of a pixel used in pipelined snapshot shutter mode is its parasitic light sensitivity (PLS), which expresses the ratio of the sensitivity of the pixel during readout relative to the sensitivity during integration. It expresses the influence of the current image on the previous image which is still being read-out. This influence should be as low as possible and here the 6T pixel performs better than e.g. a 5T buried diode pixel that can also be used in pipelined snapshot shutter mode. The PLS of the used pixel is better than 1/4000.

The pixel is used in hard reset mode which maximizes the signal swing and avoids the non-linearity problems typically associated with soft reset. The disadvantage is a slight increase in temporal noise, which is not critical for this application.

Considering the sensor is built in a 0.25µm technology, the 6T pixels are at a small pitch of 8µm. Thanks to the use of micro lenses they maintain a good quantum efficiency (including fill-factor) of 37% at 600nm (Figure 3). Their high conversion gain of 40 µV/e^- minimizes the required integration time.

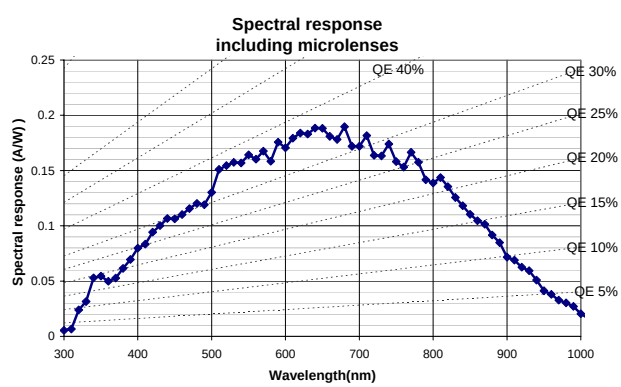

Figure 3: Spectral response as a function of wavelength for a sensor with microlenses.

4. ADC

The pixel output signals are digitized by 64 on-chip pipelined 8 bit ADCs operating at 26 Msamples/s each. The ADCs are designed using fully differential circuits to improve their performance and noise immunity. A redundant signed digit (RSD) architecture with 1.5 bit /stage and digital error correction ensures a good DNL and no missing codes, even in the presence of mismatch between the comparators. The inter-stage ADC gain errors are reduced by a commutation technique for capacitor matching and auto-zeroing removes the offsets. Data from the 64 ADCs is multiplexed on 32 high speed serial links.

5. High speed serial link

The sensor accepts a 208 Mhz LVDS input clock. This incoming high speed clock is divided to generate the different low speed clocks required for the operation of the sensor. It is also used to generate the serial output streams at 416Mbit/s. The outputs operate in double data rate (DDR) mode, which means a new data bit is put on the output at each clock transition (twice per clock cycle).

Synchronization between the sensor and the host requires a means to send control information across. This can either be done by embedding the control information in the data e.g. by employing the industry standard 8B/10B encoding or by adding a separate data channel, just to send the control information. Apart from 256 data words, 8B/10B encoding also has a set of additional control word available, which allow embedding control information into the same data stream as the payload while still allowing to distinguish it as control information at the receive end. 8B/10B has a number of other advantages such as DC balancing the data stream and guaranteeing minimum number of transitions per data word, both of which facilitate clock recovery on the receive-end. However, 8B/10B does introduce a 25% overhead in the amount of data that needs to be sent across the link. Taking into account that the control information is redundant between all channels, this is not an acceptable solution in a system with 32 data channels. That is why this sensor uses the alternative approach of simply adding two channels: one output clock channel and one synchronization data channel, which brings the total to 34 output channels. The output clock signal can be used to recover the data on the receive end without the need for clock recovery on the data channels themselves. However, the receiver should have per-channel skew correction to account for on-chip mismatches and intrinsic delays as well as for interconnect medium mismatches. The sensor has a training mode where it sends a known training pattern over each of the links to allow the host to do that calibration.

The synchronization channel sends start-of-frame, start-of-line, end-of-frame and end-of-line information the host. The current line number is also transmitted over the synchronization channel at the beginning of each line. To allow error detection at the receive-end, the sensor inserts a cyclic redundancy check (CRC) word into the data stream on each date channel at the end of every line.

The physical layer of the high speed link uses LVDS drivers. These drivers are designed in compliance with the ANSI/TIA/EIA-644-A-2001 standard for “Low Voltage Differential Signaling”. The circuit consists of a programmable current sink that defines the drive current, a dynamically controlled current source, a 4-transistor bridge that steers these currents to the differential outputs and a common-mode feedback circuit to balance the sink and source currents. The drive current can be changed by a register setting to allow operation outside the specified ANSI standard to reduce power and/or enhance speed.

6. Package and measurements

The sensor is processed in a 0.25µm 1P3M CMOS process. It is packaged in a custom made ceramic package with a 399 ball BGA. The package is made as small as possible to minimize the system size and at one side the pixel array is placed as close as possible to the edge of the package to relax the optical design. Figure 4 shows a picture of the packaged sensor.

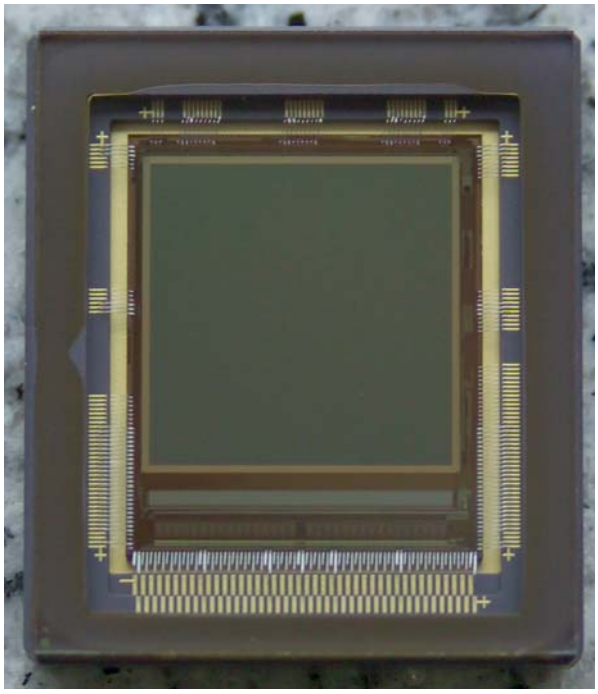

Figure 4: Photograph of the packaged sensor. The orientation of the sensor is identical to the floorplan shown in Figure 1.

Table 1 shows the key specifications and measurements of the sensor. The sensor has an on-chip reference photo diode for measuring photo current and a temperature diode for die temperature monitoring.

7. Conclusion

This paper presents a high speed image sensor design that fulfills the needs of a holographic data reader: high sensitivity and maximal data throughput at a moderate noise level and power consumption. This custom image sensor is suited for use in a high-end consumer holographic data reader.

Technology	0.25µm 1P3M CMOS process
Die size	16.0 mm (H) x 19.0 mm (V)
Packaged chip size	25.0 mm (H) x 29.0 mm (V)
Array size	1696 (H) x 1710 (V)
Frame rate	485 fps at full resolution
Shutter type	Pipelined snapshot shutter
Supply voltage	2.5V and 3.3V
Power consumption	1.1 W
Operating temperature	0ºC to 60ºC
Color	Monochrome only
Pixel type	6T N-well
Pixel size	8.0 µm x 8.0 µm
Peak QE	37% 600nm, with micro lenses
Sensitivity	2800 V m²/Watt s @600nm, with microlenses
Conversion gain	40 µV/e^-
Temporal dark noise	21 e^-
Pixel saturation charge	27000 e^-
Dark current	277mV/s at 40ºC
PRNU	2.5 % @ half saturation
FPN	17mV
PLS	<1/4000
ADC DNL / INL	0.31 LSB / 0.56 LSB
ADC resolution	8 bit
Data rate	208MHz input clock, 416Mbit/s data rate per channel 13.3Gbit/s aggregate data rate 1.4Gpix/s aggregate pixel rate
Interface	LVDS
Package	Ceramic package with 399 ball BGA

Table 1: key specifications and measurements.

References

[1]N. Bock, et al., “A Wide-VGA CMOS Images Senosr with Global Shutter and Extended Dynamic Range“ Proc. of IEEE Workshop on CCDs and AIS, Karuizawa, pp. 222-225, 2005

[2]Alex Krymski, Kenji Tajima, “CMOS Image Sensor with Integrated 4Gb/s Camera Link Transmitter”, in ISSCC Dig. Tech. Papers, San Francisco, CA, Feb. 2005