# CONSIDERATION OF DARK CURRENT GENERATION AT THE TRANSFER CHANNEL REGION IN THE SOLID STATE IMAGE SENSOR

Yoshihisa Kunimi[†], Bedabrata Pain[‡]
[†]Asahi Kasei EMD Corporation. 5-4960, Nakagawara-cho, Nobeoka, Miyazaki, 882-0031, JAPAN
Tel.: +81-982-22-5528, Fax: +81-982-22-5509, e-mail: kunimi.yb@om.asahi-kasei.co.jp
[‡]Jet Propulsion Laboratory, California Institute of Technology. 4800 Oak Grove Drive, Pasadena, CA 91109

## Abstract

One interesting CMOS image sensor structure is proposed, which can suppress the inflow of dark current from the transfer channel region into buried photodiode. In this structure, P-type polysilicon is partially formed in the N-type polysilicon of transfer gate electrode. This structure becomes operative when dark current is drastically generated at the transfer channel region due to insufficient passivation of Si/SiO2 interface levels.

## Introduction

CMOS image sensors are attractive devices because of their low power consumption and applicability for on-chip signal processing [1]. During the several decades, intensive researches focus on the improvement of their performance, especially dark current reduction. And nowadays, high quality images can be taken by putting a buried photodiode to use [2]. When buried photodiode structure is optimized for usage in each process technology, much attention has to be paid on the achievement of complete charge transfer. One of the solutions to accomplish it is to set down the threshold voltage of transfer transistor [3]. To make threshold voltage lower indicates lower doping concentration in the channel region. Generally, lighter impurity dope leads longer lifetime of minor carrier. Therefore, if dark current is generated in the channel region where doping concentration is low, it can easily flow into buried photodiode because of its longer mean free path. Fortunately, it is well known that one of the most effective ways to suppress the dark current generation in the transfer channel region is to passivate the interface levels at the Si/SiO2 interface by hydrogen or deuterium [4]. This passivation of interface level surely promises the reduction of the amount of dark current generation. But, if this passivation is insufficient or if desorption of hydrogen/deuterium occurs, dark electrons easily generate at Si/SiO2 interface and, again inflow into photodiode.

This paper proposes an interesting structure which can keep dark current lower even if interface levels are insufficiently passivated. Especially, one structure which can suppress the inflow of dark current from channel region into buried photodiode is proposed. Additionally, it also suggests that this structure has potential to make charge transfer period shorter.

## Structure and Experimental

Prototype chip (Figure 1) was fabricated based on 0.35μm process technology. Its outline is listed in Table 1. Notable point in the proposed structure is that p-type polysilicon partially exists at the edge of n-type polysilicon of the transfer transistor's gate electrode. Process sequence is shown in Figure.2, and cross section of transfer gate electrode was observed by both Scanning Capacitance Microscopy (SCM) and Tunnel

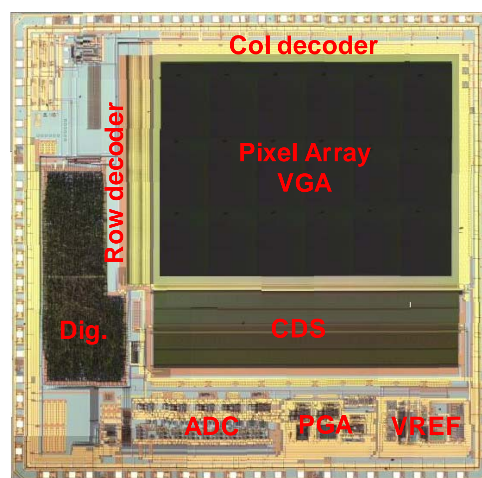


**Figure.1**, Photograph of VGA CMOS Image Sensor. (ES chip)

Electron Microscopy (TEM), as shown in Figure 3, simultaneously. For the consideration of dark current at the transfer channel region, 2 kinds of transfer gate electrodes were prepared; (S1) transfer gate consists of entire all n-type polysilicon, (S2) transfer gate polysilicon has partially p-type polysilicon in n-type one. Then, these 2 kind structures were treated under the 3 different process conditions, respectively; (A) interface level passivation process wasn't done, (B) interface level passivation treatment was done, but it was insufficient, (C) interface level was sufficiently passivated by hydrogen. Measurement results are summarized in Table.2. These results indicate that, if interface level at Si/SiO2 interface is insufficiently passivated, the amount of dark current generated at transfer channel region is larger, but partially p-type polysilicon gate can suppress the inflow of dark current into photodiodes to make dark current lower. In contrast, if interface level is sufficiently passivated, obvious suppression of dark current inflow can't be observed because the amount of dark current generation around transfer channel region is very small. Next, potential profile along the transfer channel was simulated by process / device simulators. Process simulation was done by TSUPREM-4, and device one by Medici. Simulated potential profiles in the silicon substrate, especially potential profiles around transfer channel region, are shown in Figure.5; (P1) is potential profile when the width of P-type polysilicon region in gate electrode is narrower, (P2) is when that is wider. These results indicate that the existence of P-type polysilicon in the N-type polysilicon gate electrode causes the potential gradient in the transfer channel region. Furthermore, the width of p-type polysilicon region is wider, potential gradient is widespread. In other word, wider p-type electrode can make dark electrons tend to flow away from photodiode region. Therefore dark current accumulated in buried photodiode can be kept lower. This is also explained by using illustrations shown in Figure.6. This structure

**Figure.2**, process sequence for parital p-type polysilicon formation in the transfer gate.

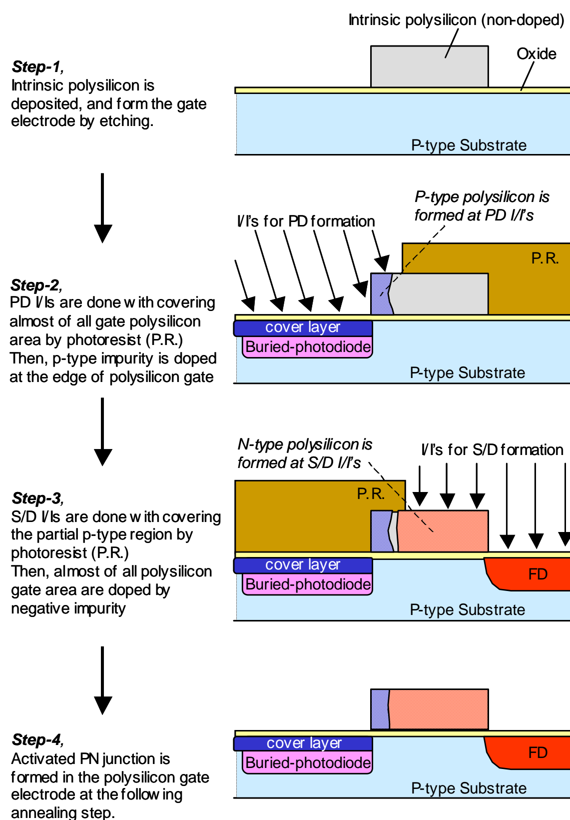


**Table.1** Outline of prototype chip

| Sensor Technology | CMOS / 4T |
|---|---|
| Optical format | 1/4-inch VGA |
| Pixel pitch | 5.6 μm x 5.6 μm |
| Color filter array | R,G,B, Bayer pattern |
| Process rule | 0.35 μm 2P3M CMOS |
| Frame rate | 30 fps |
| Shutter | Electric rolling snap |
| ADC | On-chip 10-bit |
| Supply voltage | Analog: 2.7 V to 3.6 V |

**Table.2** Measurement results of dark electrons at 25C

| Transfer gate poly | Entire all N+ polysilicon (S1) | Partially P-type (S2) |
|---|---|---|
| (A); No passivation | 197 e-/sec. | 176 e-/sec. |
| (B); Insufficient passivation | 123 e-/sec. | 115 e-/sec. |
| (C); Enough passivation | 43 e-/sec. | 45 e-/sec. |

can give us a help to reduce the amount of dark current in cmos image sensor, and can give us better quality image, as shown in Figure.4.

But, if the width of P-type polysilicon region is too wide, the extraction of electrons from buried photodiode to transfer channel during the charge transfer period becomes more difficult. It leads big image lag. It is necessary to optimize not only the width of p-type region but also the impurity profile of buried photodiode, carefully.

Additionally, potential gradient in the transfer channel region might also contribute to making the charge transfer faster. Specifically, potential gradient causes the drift diffusion of electrons in the transfer channel region. Therefore charge transfer can be done during the shorter period. Furthermore, when transfer channel is turn ON into OFF, this potential gradient can push the signal electrons in transfer channel toward FD region. That is, this structure can also contribute to the reduction of image lag; especially suppression of spill back of electrons from transfer channel to photodiode.

## Conclusions

Partial existence of P-type polysilicon in N-type transfer gate polysilicon electrode is considered in this paper. Measurement results imply that it might contribute to the suppression of the inflow of dark current generated at transfer channel region into buried photodiode. It is due to the potential gradient in the transfer channel. And this unique structure has potential to make charge transfer faster. Additionally it might suppress the spill back of the signal electrons into photodiode when the transfer channel turns ON into OFF.


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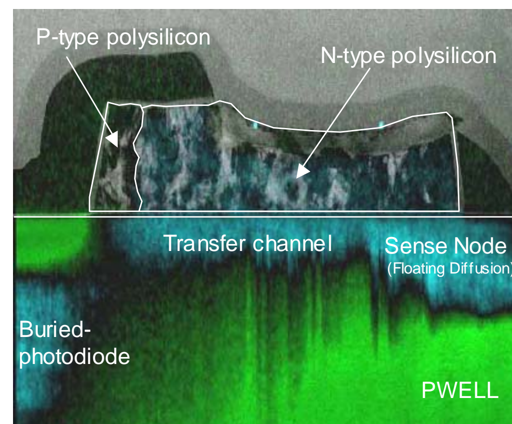


**Figure.3**, Cross-sectional image of Transfer-Transistor in 4T/CMOS image sensor. This image was obtained by combining a TEM image with a SCM (Scanning Capacitance Microscopy) image.

**Figure.4**, A captured image.

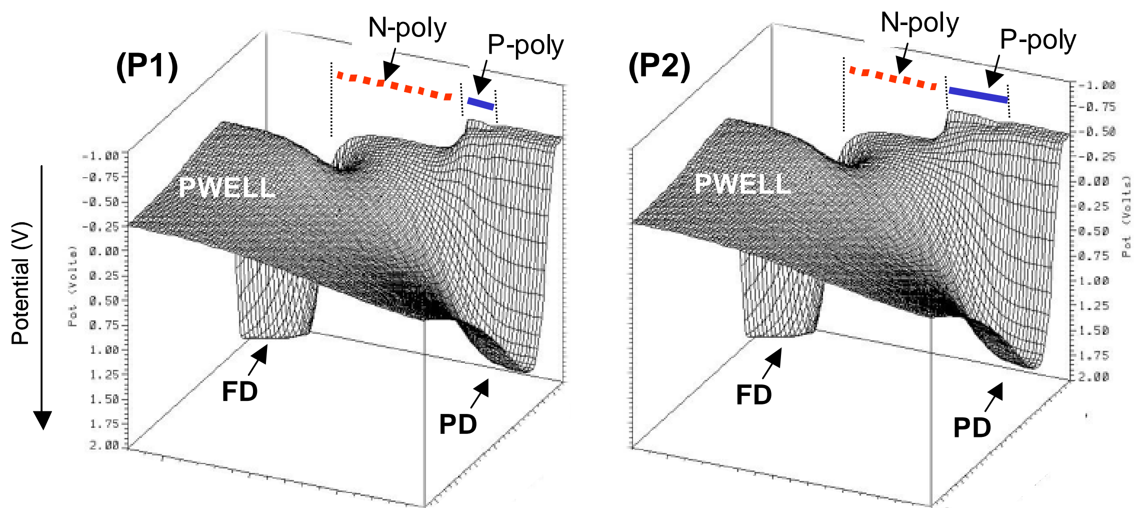


**Figure.5**, Simulation results of potential distribution in the Si-substrate, especially around the transfer channel region. (A) Potential distribution when the width of P-type polysilicon in the transfer gate electrode is 0.05 μm. (B) Potential distribution when width of P-type polysilicon is 0.30 μm.

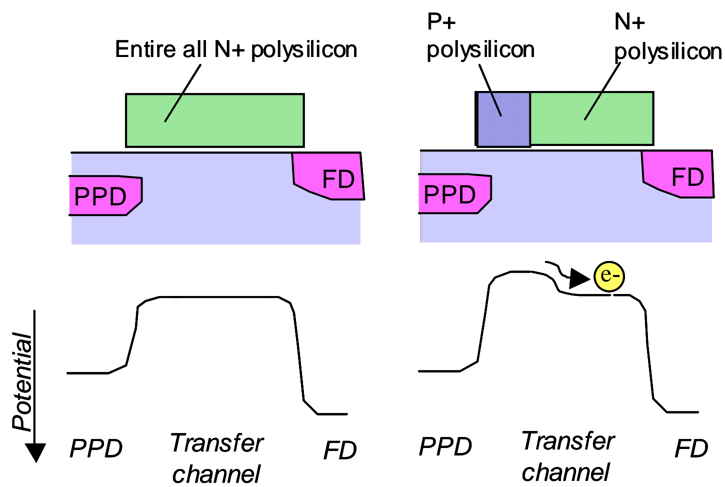


**Figure.6**, The upper left is a cross sectional image of transfer transistor whose gate electrode consists of entirely N+ polysilicon, and the lower left is horizontal potential profile image in transfer channel. The upper right is a cross sectional one which has partial P-type region in the N+ polysilicon electrode, its transfer channel potential is shown at the lower right.