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8.3 Mp, 4/3" Full-Frame CCD with Scaled LOD and Micro Optics

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Introduction

As the demand for higher and higher resolution within a given optical format pushes pixel sizes ever smaller, it becomes increasingly difficult to maintain other key performance aspects of the device. In particular, dynamic range and photoresponse of the pixel start to severely degrade as pixel size is reduced. This paper describes some novel device structures and scaling used to counteract these size effects for the next-generation 4/3" sensor. One such novel structure is a scaled lateral-overflow drain (LOD) where the drain is placed underneath the thick field oxide commonly used for isolation between the vertical CCDs. This under-the-field oxide LOD (UFOX LOD) structure takes up much less pixel area, resulting in improved charge capacity without sacrificing drain-limited blooming protection of the device. The other area of the pixel structure requiring attention is the scaling of the optical stack to maintain sensitivity and the angle response of the pixel. This is accomplished by direct scaling of the various over layers in the optical stack. In addition to a thinner microlens, planarization and CFA layers, a unique thin-light shield process is employed. In this process, the light shield layer is formed by using the bottom TiW layer of our standard two-layer TiW/Al metallization process, thereby eliminating the need for additional inter-metal dielectric layers to help minimize the overall stack height.

I. Device Overview and Pixel Architecture

We recently developed an 8.3 Mp, full-frame CCD image sensor with 5.4 mm pixels for use in 4/3" (optical) format digital still cameras. Like its predecessor (a 5.1 Mp, 4/3" CCD with 6.8 μm pixels), the imaging pixels consist of a two-phase CCD with a lateral-overflow drain (LOD) for blooming suppression. One of the CCD gate electrodes is formed out of indium-tin oxide (ITO), and the other is formed from conventional polysilicon. Light is focused through an overlaying R, G, B Bayer color filter array and microlens array into the more transparent ITO region for high sensitivity. A single, 28 MHz two-phase horizontal CCD register and conventional floating-diffusion amplifier are used for signal readout. Full (all pins), 200 V machine model (2 kV HBM) ESD protection is provided.

II. Charge Capacity and Blooming Protection - New UFOX LOD Strucuture

Kodak's full-frame CCD imagers use a lateral-overflow drain to suppress blooming [1], [2]. A cross section of this structure is shown below in Fig. 1a. As the area of this LOD structure is reduced, the charge storage area will increase for a given pixel size. Conversely, simply reducing the cross-sectional area of the LOD would increase its resistance, thereby resulting in a reduction in blooming protection. For short exposure times, it can be shown that the amount of blooming protection afforded by such a structure is limited by the resistance of the drain region, as given by the expression

$$X_{AB} \cong \frac{\left(V_{LOD} - \varphi_{acc,B3} - 0.5\right)\cdot \Delta t}{n \cdot m \cdot \left(1 - m/M\right)\cdot q \cdot N_{SAT} \cdot R_{PIX} \cdot \left(100/FF\right)} \quad (1)$$

where V_{LOD} is the LOD bias in volts, $\varphi_{acc,B3}$ is the accumulation potential of the overflow-barrier region (indicated as B3 in Fig. 1b below) in volts, Δt is the exposure time in seconds, M is the total number of pixels in the vertical CCD shift register, n is the spot size of uniform light incident on the sensor in number of pixels, m is the pixel index along the shift register corresponding to the center of the spot, N_{SAT} is the charge capacity of a single pixel in electrons, R_{PIX} is the LOD resistance of the pixel in Ω/pixel, FF is the ratio of charge collected in the storage regions of the pixel to the total charge collected in the storage regions and the LOD (this term allows for the effects of cross-talk to be taken into account), 0.5 is the energy barrier in volts for thermionic emission of electrons back over the B3 region from the LOD, and q is the electronic charge.

Given that R_{PIX} is inversely proportional to the width and integrated doping density of the LOD, its width could be reduced without a loss in drain conductance or blooming protection, simply by increasing its implant dose. However, for our conventional LOD structure wherein the heavy n+ drain is directly under the CCD gate electrodes (which are biased in accumulation to reduce dark-current generation during scene integration), we found that, as the LOD doping level is increased, sharp band bending occurs near the silicon surface within the drain region, which ultimately leads to breakdown via band-to-band tunneling [3]. This places an upper limit on the doping level that can be implanted for a given gate-to-LOD voltage difference (or vice versa). Hence, the drain conductance and blooming protection of this structure becomes limited. To overcome this doping-level limitation due to band-to-band surface breakdown, we devised a new structure where the drain is placed underneath the thick field oxide [3], [4] normally

used for column isolation as shown in Fig. 1b. The breakdown of the new structure is limited by the avalanche mechanism at the n+/p+ LOD-to-channel stop junction. Because this breakdown is limited by the lighter doped channel-stop side of the junction, the doping level of the LOD can be increased dramatically.

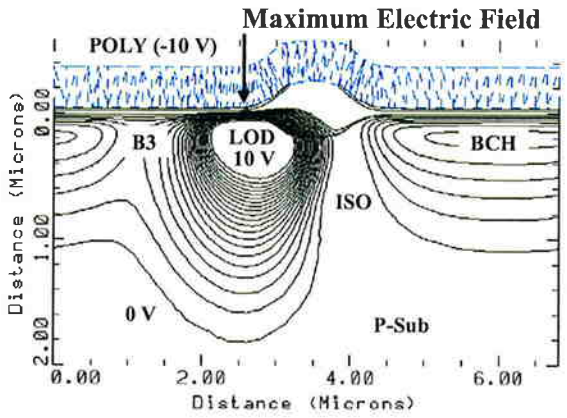

Fig. 1a: Cross section of conventional LOD structure used on 6.8 µm pixel device.

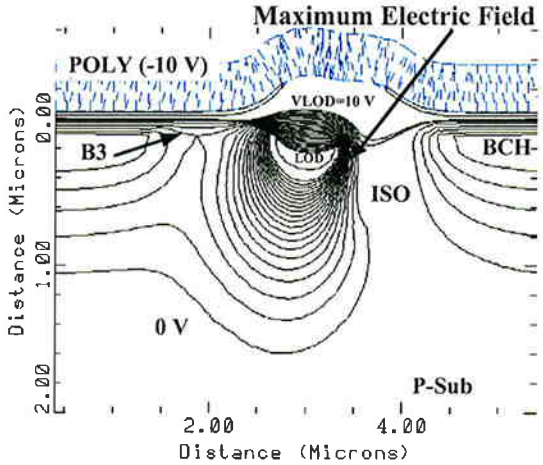

Fig. 1b: Cross section of new under-the-field oxide (UFOX) LOD structure used on 5.4 µm pixel device.

For the 5.4 µm pixel using this new UFOX LOD structure, the measured charge capacity is 35 ke- and blooming protection of well over 1000X has been measured for integration times as short at 1 ms. Without the use of the new UFOX LOD structure, the charge capacity would have been limited to approximately 20 ke- for this pixel owing to the blooming protection requirement. Therefore, this new technology has led to roughly a 75% improvement in N_{SAT} without sacrificing blooming protection. For comparison, the charge capacity of the 6.8 µm pixel using the old LOD technology is typically about 40 ke-. With a read noise of 17 e- rms and 16 e- rms for the 6.8 µm and 5.4 µm pixel devices, the resulting dynamic range works out to be 67.4 dB and 66.8 dB, respectively. Thus, dynamic range has been maintained despite reducing the pixel area by nearly 40%.

III. Quantum Efficiency, Responsivity, and Angle Response - Scaled Micro Optics Process

The other key aspects of device performance that become compromised with reduced pixel size relate to the light-gathering capability of the pixel. As the pixel size is reduced (in the absence of any other changes), the device's quantum efficiency, responsivity, and angle response are reduced. This is because all of the light rays may not be properly focused through the aperture into the more sensitive ITO region, if the micro optics are not scaled properly. To address this part of the problem, a simple scaling of the lens height (from the silicon) and lens thickness by the ratio of the pixel size was applied to the process. To scale the lens height down, a thin light-shield process was developed that uses only the bottom TiW layer of our standard Al/TiW bi-layer metallization process. The CFA and planarization layers were also thinned. This scaling also results in improved transmission through a thinner CFA and improved topography. The combination of these effects results in improved quantum efficiency and angle response. Cross sections of the 6.8 µm and 5.4 µm devices along the CCD are shown below in Fig. 2a and 2b, respectively.

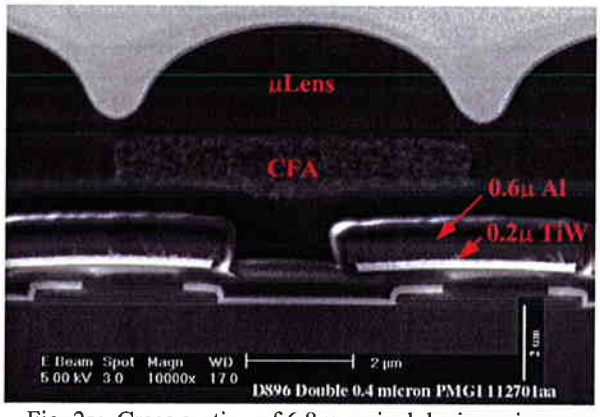

Fig. 2a: Cross section of 6.8 µm pixel device using our old micro-optics/CFA and thick aluminum light-shield process. T_{CFA} = 1.5 µm, T_{LENS} = 2.6 µm, T_{LTSH} = 0.8 µm.

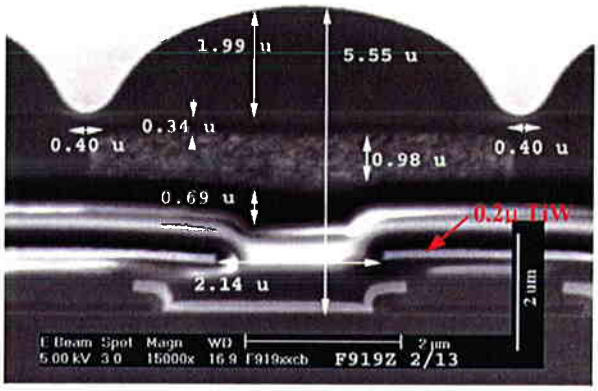

Fig. 2b: Cross section of 5.4 µm pixel device using our new, scaled micro-optics and thin CFA and light-shield process. T_{CFA} = 1 µm, T_{LENS} = 2 µm, T_{LTSH} = 0.2 µm.

Shown below in Figs. 3a and 3b, is a comparison of quantum efficiency and angle response between the 6.8 um pixel device built using our older process and the 5.4 um pixel device using our newer scaled process. Note how, in spite of the smaller pixel size, the new device has higher quantum efficiency and better angle response. The angle response of our devices was measured in the vertical direction whereas the other manufacturer's devices were measured in the horizontal direction. (These are worst-case conditions because of their respective aperture orientations.)

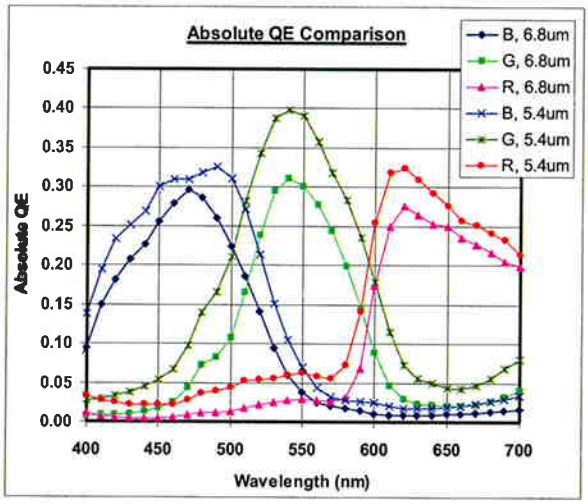

Fig. 3a: Absolute quantum efficiency comparison of new 5.4 μm and older 6.8 μm pixel devices.

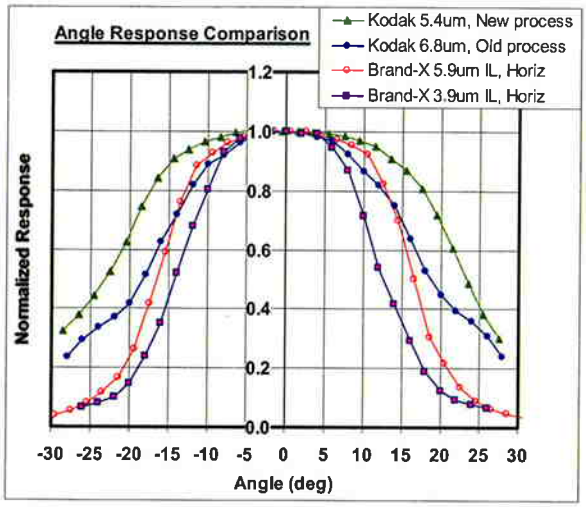

Fig. 3b: Angle response comparison of new 5.4 μm and older 6.8 μm pixel devices. Green illumination was used.

It is clear from Fig. 3a that the integrated response of the newer device will lead to good optical responsivity as given by the well-known expression,

$$\overline{R} = \frac{A_{PIX} \int QE \cdot T_{IR} \cdot H \cdot \lambda \cdot d\lambda}{hc \int H \cdot V \cdot d\lambda} \tag{2}$$

where A_{PIX} is the pixel area, QE is the absolute quantum efficiency, T_{IR} is the transmission of the IR filter used in conjunction with the sensor, H is the spectral power density of the source, λ is the wavelength, V is the luminous efficacy in lm/W, and hc is the product of Planck's constant and the speed of light.

Using this formula and the measured quantum efficiencies as shown in Fig. 3a, the responsivity for the two devices was calculated. These calculations assumed a 3200 K tungsten source and typical IR cut filter (at λ = ~650 nm). The results of these calculations are summarized below in Table 1.

Table 1: Comparison of Device Responsivity for 3200 K Tungsten Source

Pixel Size (μm)	Responsivity (ke/lx-s)		
	R_B	R_G	R_R
6.8	25.5	42.4	41.9
5.4	22.0	41.4	35.5

Note that, even though the pixel area was reduced by roughly 37%, high responsivity was maintained as the result of the newly scaled process. Using the responsivity values from Table 1, along with the measured charge capacity, the saturation-limited, or base-exposure index can be calculated by using the well-known expression (ISO Standard 12232),

$$EI_{SAT} = \frac{78 \cdot R}{N_{SAT}} \tag{3}$$

Therefore, for the 6.8 μm and 5.4 μm pixel devices, $EI_{SAT,6.8} = 83$ and $EI_{SAT,5.4} = 92$ for the green channel. The thinner CFA layers do result in less off-band rejection, however. From image simulations it was found that the color error was actually lower with the higher-off band response of the new device. Conversely, the noise introduced via the color-correction matrix was somewhat higher due to the higher off-diagonal matrix elements.

Conclusions

A comparison chart of the 5.1 and 8.3 megapixel, 4/3-inch image sensors is given below in Table 2.

Table 2: Comparison of 5.1 Mp and new 8.3 MP 4/3-inch Image Sensors

Parameter	KAF-5100CE	KAF-8300CE	Units	Conditions
Effective Pixels	2654 x 2006	3358 x 2536	H x V	
Pixel Size	6.8 µm	5.4	µm	
Charge Capacity,				60 °C
N_{SAT}	40 ke	35	ke	
V_{SAT}	730	780	mV	
Dark Signal,				
N_{DARK}	140	70	e/pix/s	60 °C
Read Noise, *Nee*	17	16	e rms	28 MHz
Dynamic Range, DR	67.4	66.8	dB	28 MHz, 60 °C
Charge-to-Voltage	18	22	µV/e	
Peak QE B,G, R	30, 31, 28	32, 40, 32	%	
Responsivity,				3200 K, Tung
R_B, R_G, R_R	25.5, 42.4, 41.9	22.0, 41.4, 35.5	ke/lx-s	
Sat Exposure Index				3200 K, Tung
Green, EI_{SAT}	83	92	-	
Blooming Protection				10% spot
Factor, X_{AB}	> 1000X	>1000X	*E_{SAT}	t_{INT} = 1 ms
Charge Transfer				
Efficiency, *CTE*	> 0.999995	> 0.999995		28 MHz

References:

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[4] E. K. Banghart and E. G. Stevens, "Lateral overflow drain, anti-blooming structure for CCD devices having improved breakdown voltage," *U. S. Patent 6,624,453*, September 23, 2003.

[5] E. G. Stevens, "Method for Forming Light Shield Process for Solid-State Image Sensor with Multi-Metallization Layer," *U. S. Patent 6,867,062*, March 15, 2005.

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