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A 9 Megapixel APS-size CMOS image sensor for digital still photography

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Abstract

We present a 9 Megapixel CMOS active pixel sensor for digital still photography. The focal plane array is 23.3 x 15.5 mm^2. The diagonal is 1.5x smaller than that of 35 mm film. The device is intended for SLR digital still cameras. In such camera, this reduced sensor size corresponds to a 1.5x focal length multiplication.
The device has 6.4 µm active pixels. It offers column gain (in steps of x1, x2, and x4), on-chip correlated double sampling and it has 2 differential output channels. Resolution is 3710 x 2434 pixels. Full well charge is 80,000 electrons, and temporal noise is 25 electrons, offering a linear dynamic range of 70 dB. Quantum efficiency * fill factor is 35%. Conversion gain is 8 µV/electron. Dark current is below 3 mV/sec at 30 C.
The imager has sub-sampling, binning and windowing capabilities. A full image is read out at 5 frames/s, windowed preview at smaller resolution up to 38 frames/s is possible. Dark references are available either through optical black pixels (with an optical black color filter) or through electrical black references.
The device is manufactured in a 0.15 µm technology. Metal stack thickness between the photodiode and the color filter is only 4 µm. Such thin metal stack is important to accept a large range of incident angles of light on the silicon, without causing color crosstalk. Because of the large range of optics used in this application, a thin stack is the only possibility to avoid color crosstalk.

1. Introduction

Digital Single Lens Reflex (SLR) cameras are becoming more and more popular. They make use of large area CCD or CMOS image sensors. Manufacturing economics drives the image sensor to smaller sizes; yet the desired the compatibility with film-based SLR cameras drives it to towards larger sizes, similar to 35 mm film. A compromise used by most manufacturers nowadays is the so-called APS format with a diagonal of 28 mm, which is 1.5x smaller than 35 mm film. These sensors are very large compared to point-and-shoot cameras, resulting in more and larger pixels.
This market has gradually moved towards CMOS [1] for various reasons.

- Pixel size is less critical than in point-and-shoot cameras. CCD sensors can not exploit their benefit of allowing smaller pixel sizes.
- Device area is so large that it becomes difficult to drive the CCD input clocks. The input capacitance of CCD input phases scales with the device area. Camera power dissipation is considerably lower with a CMOS sensor.
- Image quality of CMOS image sensors has considerably be improved by the use of buried photodiodes [2,3,4]
- Cost. Because of the relatively low number of dies on a wafer (54 in our case), the device is quite sensitive to the wafer price. The CMOS pixel architecture can be made less sensitive to wafer defects. This makes the CMOS sensors more economical.

This paper describes a 9 Megapixel APS CMOS image sensor. Section 2 describes the architecture of the device. The characterization results are described in section 3.

2. Architecture

The pixel is a 5-transistor buried channel photodiode (figure 1). The 5th transistor is used to increase the capacitance of the floating diffusion. Table 1 shows the key features of this device.

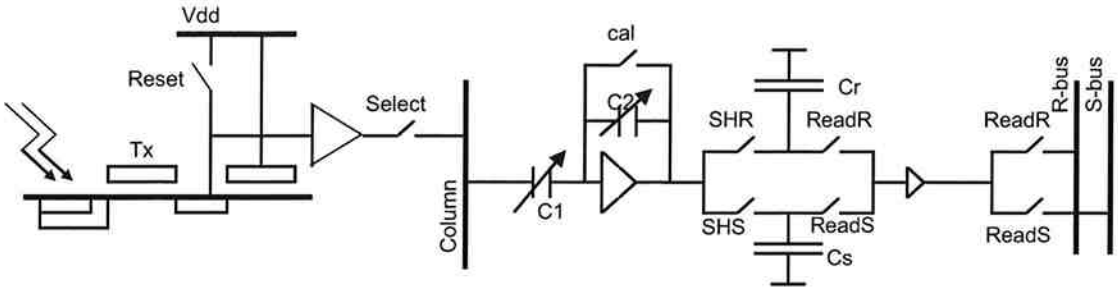

Figure 1: pixel and column amplifier architecture

Table 1: Key features of the sensor

Parameter	Specification
Pixel size	6.4 µm
Column gain stage	x1, x2, x3.2, x4
Output stage	Differential outputs 2 channels Adjustable DC offset 0.5..2.5V
Readout features	Windowing Subsampling 1820 x 1212 (Read 2, skip2) at 18 frames/s 1212 x 808 (Read 2, skip4) at 36 frames/s X Binning: 1820 x 2424 (Read 2, skip 2) at 9 frames/s
Maximum frame rate (full resolution)	5 Hz
Pixel rate	52 MHz (2 x 26 MHz)
Focal plane size	23.3 mm x 15.5 mm
Focal plane multiplier	1.54x compared to 35 mm film
Resolution (including black reference pixels)	3710 x 2434
Resolution (RGB pixels only, final image)	3640 x 2424 (= 8.8 Megapixel)
Dark reference	Optical black pixels Electrical black pixels
Process	0.15 µm single-poly dual-metal with local tungsten interconnect layer
Package	42 pins PGA

The metal stack above the silicon is kept thin by the use of only 2 metal layers and a thin higher-resistive Tungsten local interconnect layer. This results in a distance between color filters and silicon of 4 micron. Because of the large variety of optical conditions in this application, no other measures can be taken to reduce the effects of angular incident light.

Figure 2 shows the architecture of the device. The timing to the pixels is fully open and the chip does not contain hard sequencing logic. This allows fine-tuning the timing for utmost image quality. All extra on-chip features are related to ease of use (like windowing, binning, sub-sampling, standby mode) or improved data processing or image quality. Column amplifiers contain a variable gain stage with settings at 1x, 2x, 3.2x and 4x. This is implemented with an ac-coupled amplifier, which is calibrated on the reset level of the pixel (figure 1). The signal level and the reset level of the column amplifiers is stored on 2 capacitors. These

signals are multiplexed sequentially to the output, at which the difference is calculated [5]. Offsets between the 2 output channels can be adjusted by a programmable fine offset adjustment between the channels. The chip allows (pseudo-)binning by shunting the sample capacitors of neighboring columns.

The chip generates a dark reference voltage either by an optical black pixel or by an "electrical" black pixel. The latter is realized by sampling the pixel's reset level en lieu of the pixel's signal. This is either realized by a timing change (to create a black row) or by a change in the column amplifier configuration (to create a black column).

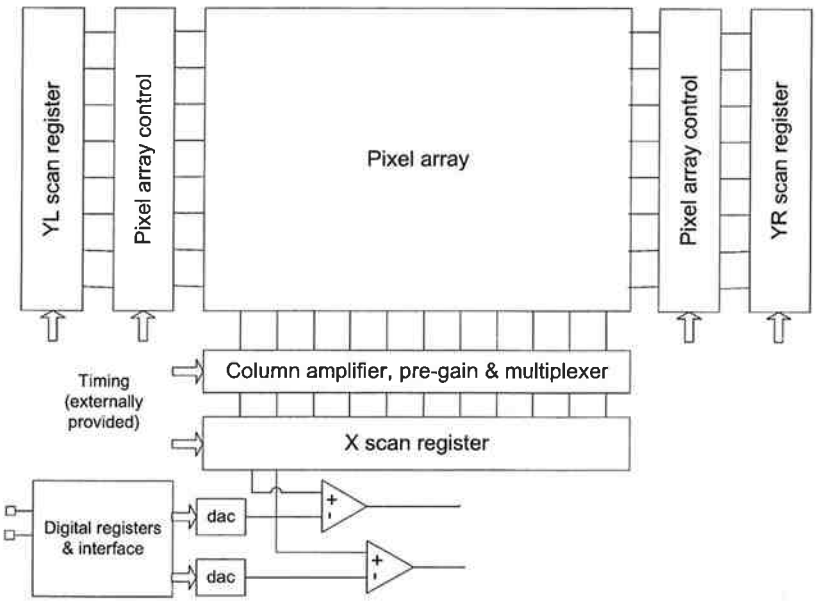

Figure 2: architecture of the 9 Megapixel imager

3. Performance

Table 2 lists the main performance parameters measured on the first generation devices. Figure 3 shows the spectral response curve (including fill factor) measured on a monochrome sample. The dashed lines indicate quantum efficiency. Figure 4 shows an image captured by the chip at 4 seconds exposure time of a 16 lux scene with a F#4 lens.

Table 2: device specifications

Parameter	**Specification**	**Comment**
Quantum efficiency	>40%	400 – 650 nm Including fill factor
Average Spectral response	0.2 A/W	
Temporal noise	25 electrons	
Green noise photons	56	= Noise electrons / QE at 550 nm.
Full well charge	80,000 electrons	
Linear dynamic range	70 dB	
Dark current	3 mV/s @ 30 °C.	Doubling every 10 °C
Conversion gain (unity gain)	8 µV/electron	In unity gain
Fixed pattern noise	1 mV RMS	In unity gain
Photo-response non-uniformity	< 2% RMS of signal	At 50% of amplitude
Power dissipation	150 mW	At max. pixel rate

4. Conclusion

A 9.0 Megapixel APS-size CMOS image sensor for digital still photography is presented. The use of a buried channel photodiode in the 6.4 micron pixel results in excellent low light performance.

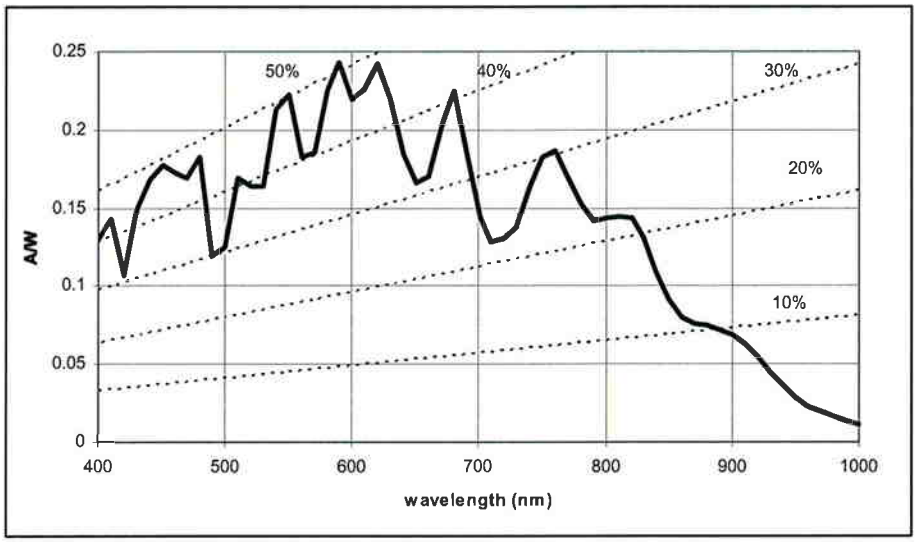

*Figure 3: Spectral response * fill factor. Dashed lines are lines of constant quantum efficiency*

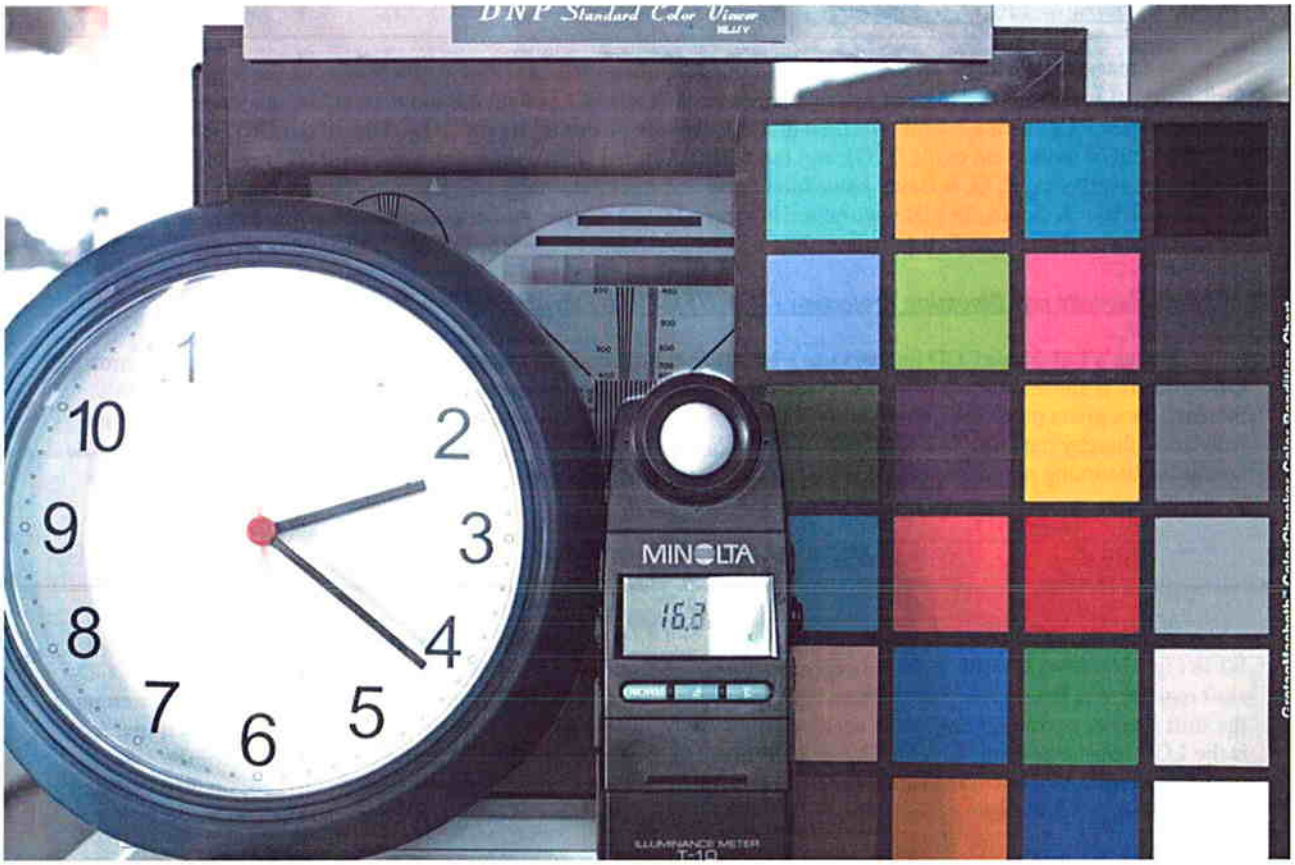

Figure 4: 4 second exposure at 16 lux, lens F#/4, min. gain.

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