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Image compression sensor using inter-frame and intra-frame correlation

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1. Introduction

Integration of image sensing and processing circuits on a LSI chip is novel approach to enhance the performance of image sensor [1]. We have been investigating image compression sensors based on conditional replenishment for high frame rate imaging [2]. In this paper, we propose a new image sensor with image compression and A/D conversion functions. The proposed sensor can significantly reduce the amount of output pixel data by using the spatial and temporal correlation. In this paper, we describe the algorithm of image compression and show design of the image sensor.

2. Proposed image compression method

Fig.1 shows the flow chart of the proposed image compression. In the method, both inter-frame prediction and intra-frame prediction are adopted. Only when the both prediction errors are large, the corresponding pixel data with its address information is output from the sensor.

2.1 Inter-frame prediction

Inter-frame prediction of our sensor is based on a conditional replenishment. First, a present pixel value is compared with the previous output pixel value held in a memory. If the absolute difference is smaller than a threshold (th1), low is assigned for flag1. Then output of the present pixel value is skipped and the memory isn't updated. When the absolute value is larger than the threshold (th1), high is assigned for flag1 and the pixel moves to next step of intra-frame prediction.

2.2 Intra-frame prediction

A pixel value of the individual pixel is predicted by two neighboring pixels (left and up) [3]. In Fig.2, a noticed pixel D is estimated by two neighboring pixels B and C. Supposed P_D is the predicted value of D, M_B is the memory value of B, and M_C is the memory value of C, P_D can be calculated by the following.

$$P_D = \frac{M_B + M_C}{2} \quad \cdots (1)$$

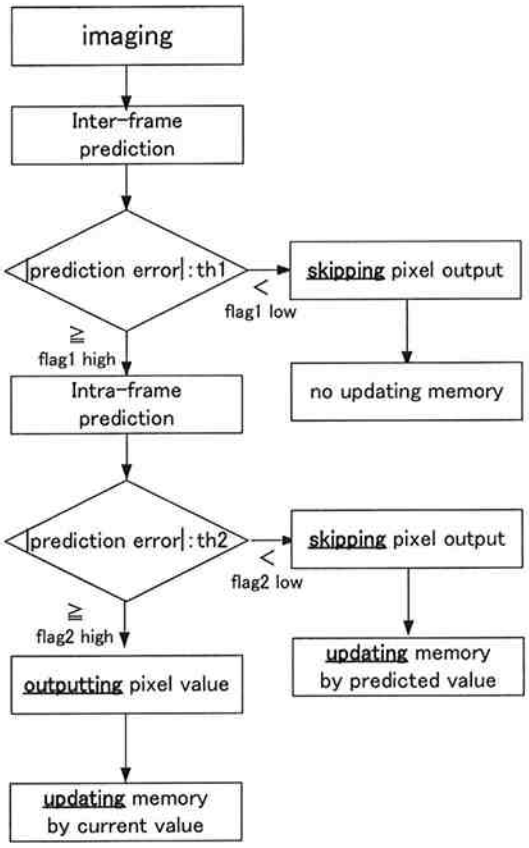


Fig.1 Flow chart of the proposed image compression method

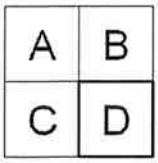
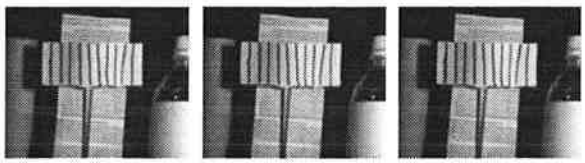


Fig.2 Place of pixels in intra-frame prediction



(a) n+1 frame (b) n+2 frame (c) n+3 frame

Fig.3 Evaluated images

The predicted value is compared with the present pixel value of D. If the absolute difference is smaller than a threshold (th2), low is assigned for flag2. Then output of the present pixel value is skipped and the memory is updated to the predicted value. When the absolute value is above th2, high is assigned for flag2, the present pixel value is output and the memory is updated to the present pixel value.

2.3 Evaluation of the proposed method

We evaluate the proposed method using the images as shown in Fig.3. The images are captured by a high speed CCD camera.

First, Fig.4 shows relation of PSNR to a number of output pixels when th1 is fixed and th2 is adjusted. As a result, by controlling two kinds of thresholds, the number of output pixels can be reduced while keeping high PSNR.

Next, Fig.5 shows PSNR results of different imaging speed when th2 is fixed and th1 is adjusted. As a result, more output pixels can be reduced while becoming higher speed.

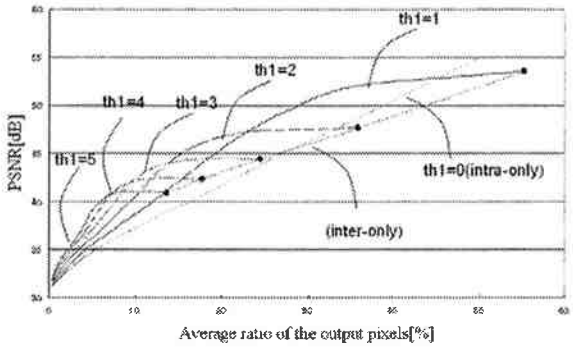


Fig.4 Relation of PSNR to output pixels

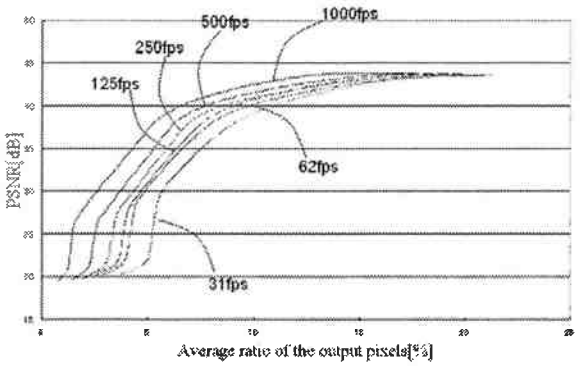


Fig.5 PSNR results of different imaging speed

3. New image compression sensor

Fig.6 shows the block diagram of the image sensor we have designed. There is a Photo Diode (PD) array that consists of 64x64 pixels. Below the PD array, there are Address Encoder, Horizontal Shift Register, Average circuit, Comp circuit and Memory. And at the right of the sensor, 8bits A/D converter is placed. We adopt a column parallel architecture for the new sensor. The pixels of each column share one processing circuit.

Fig.7 shows the processing scheme for one pixel. For inter-frame prediction, the pixel value read out from the PD array is compared with the previous pixel value held in memory C_m by Comp circuit. If the difference is smaller than th1, memory isn't updated and output of the present pixel value is skipped. If the difference is larger than th1, the pixel moves to next step of intra-frame prediction.

Fig.8 shows the circuitry of pixel value prediction. Average circuits are placed on the center of the sensor in column parallel. By the previous row capacitor and the present row capacitor, M_B and M_C of equation (1) are averaged and P_D is obtained. Then P_D is compared

with the present pixel value for intra-frame prediction. If the difference is smaller than th2, memory is updated to the predicted value and output of the present pixel value is skipped. If the difference is above th2, the present pixel value is output and memory is updated to the present pixel value.

It is necessary to output the pixel value only when both flag1 and flag2 become high and skip the output of the pixel value when either flag1 or flag2 becomes low. Then, the selective reading has been achieved with a smart horizontal shift register. Fig.9 shows the horizontal shift register with the skipping function.

We have designed the prototype sensor which consists of 64x64 pixels. Table1 shows the outline of the sensor and Fig.10 shows the prototype chip.

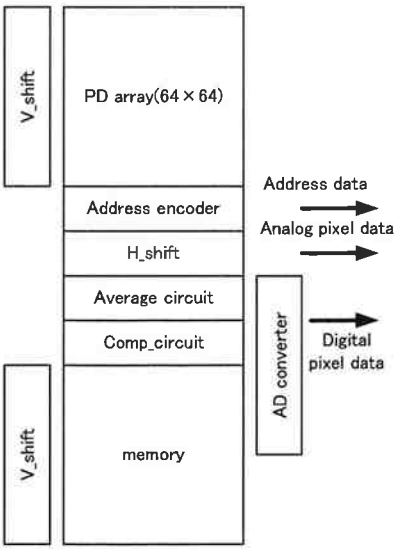


Fig.6 Block diagram of the image sensor

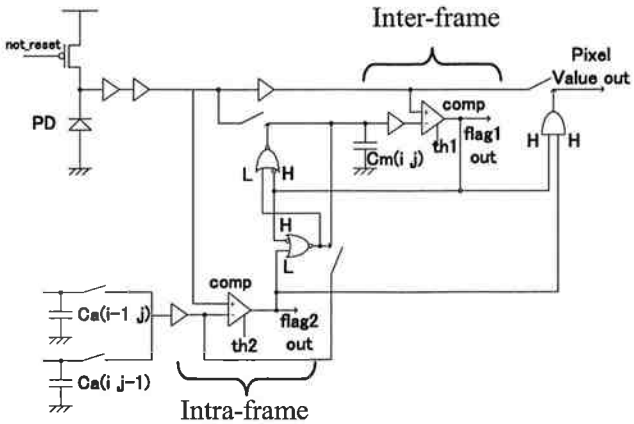


Fig.7 Processing scheme for one pixel

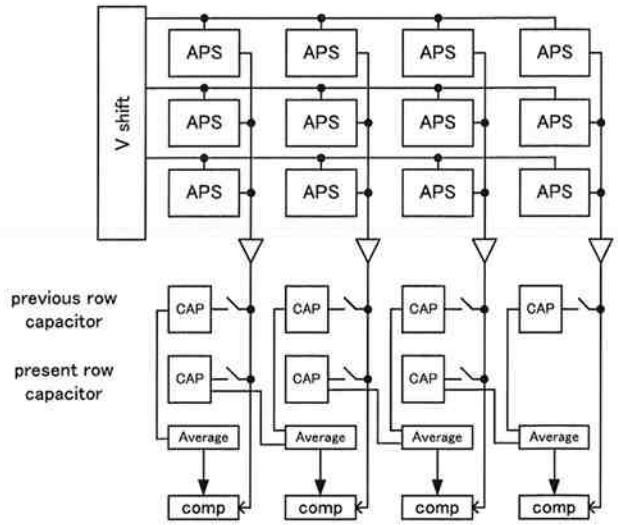


Fig.8 Circuitry of pixel value prediction

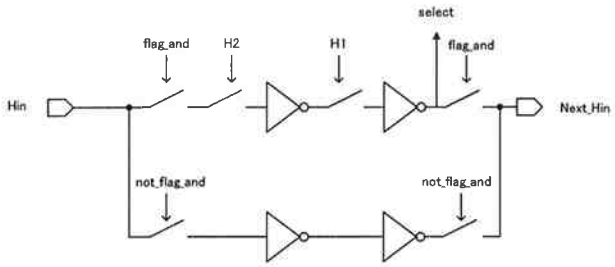


Fig.9 Horizontal shift register with the skipping function

Table 1 Outline of the sensor

Process	2poly, 3metal,CMOS 0.6um
die size[mm²]	3.1×5.4
power supply[V]	5
pixel pitch[um]	25
number of pixels[pixels]	64×64
fill factor[%]	50.5
number of transistors	
transducer[Tr./pixel]	3
memory[Tr./cell]	6

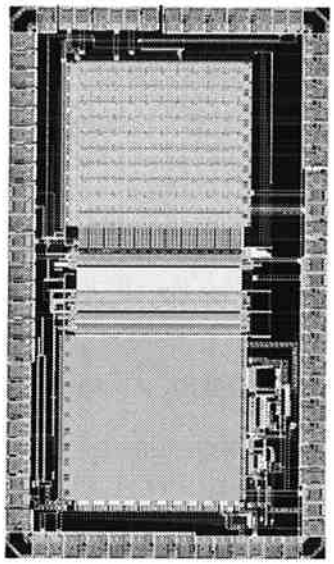


Fig.10 Prototype chip

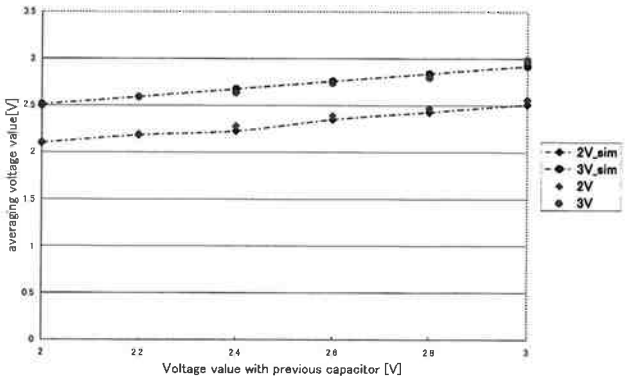


Fig.11 Evaluation result of averaging circuit

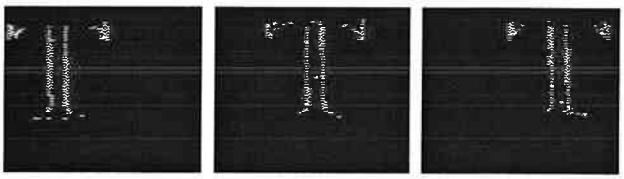


Fig.12 Evaluation result of inter-frame prediction

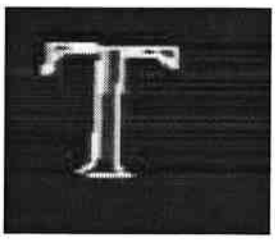


Fig.13 Evaluation result of intra-frame prediction

4. Evaluation of the prototype chip

Fig.11 shows the evaluation result of the averaging circuit implemented on the sensor as a test circuit. At the same time, a result of computer simulation is also shown in the figure. It is verified that the averaging circuit has good accuracy.

Fig.12 shows the flag signals of the inter-frame prediction obtained by the chip. In the experiments, a character "T" was moving horizontally at high speed. The vertical edges of the character activate the flags.

Fig.13 shows the flag signals of the intra-frame prediction without the inter-frame prediction. Both vertical and horizontal edges of the character activate the flags clearly. It is confirmed that both inter and intra prediction functions can be operated correctly.

5. Conclusion

In this paper, we described a new image compression sensor by using the spatial and temporal correlation. And we confirmed correct operation of the inter-frame prediction and intra-frame prediction. The prototype is now under further verification.

References

[1] T. Enomoto, K. Uchiyama, R. Kasai, M. Yoshimoto, T. Ogami, M. Abe, M. Seki and T. Hamamoto, "Video/Image LSI System Design Technology", CORONA PUBLISHING, CO., LTD., Tokyo Japan, pp.279-282, 2003.

[2] T.Hamamoto, Y.Ohtsuka, K.Aizawa, "128x128 pixels image sensor for on-sensor-compression", IEEE Int. conf. on Image Processing (ICIP'98), Vol.1, pp.493-497, 1998.

[3] H.Harashima, et.al., "Image data compression", Ohmsha, 1991.