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A Low-Voltage Pulse-Width-Modulation Image Sensor

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1 Introduction

In this paper, low-voltage operation of a CMOS image sensor using a pulse-width-modulation (PWM) reading method is presented. Mobile and sensory-network applications of image sensors strongly require low power consumption, which is generally achieved by lowering power supply voltages. However, in conventional CMOS image sensors using a source follower to read out the pixel value, in which light intensity is represented by the amplitude of voltage or current signals, the lowered power supply voltage has been achieved at the cost of the dynamic range. As the previous work, applications of pixel-level PWM reading method to on-chip image processing have been explored[1]. In this paper, we propose an application of the PWM method to low voltage driving of a CMOS image sensor and demonstrate that it is achieved with much less degradation of dynamic range than the conventional source-follower-based image sensors.

2 Design and Operation Principle

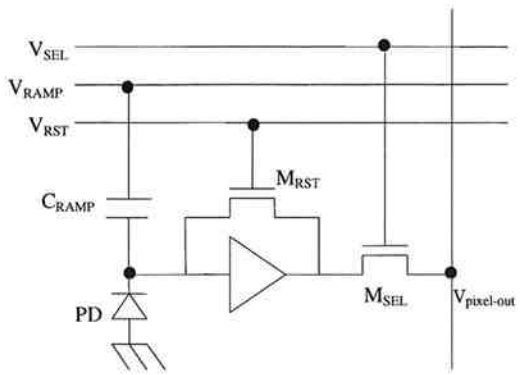

Figure 1: Pixel Structure.

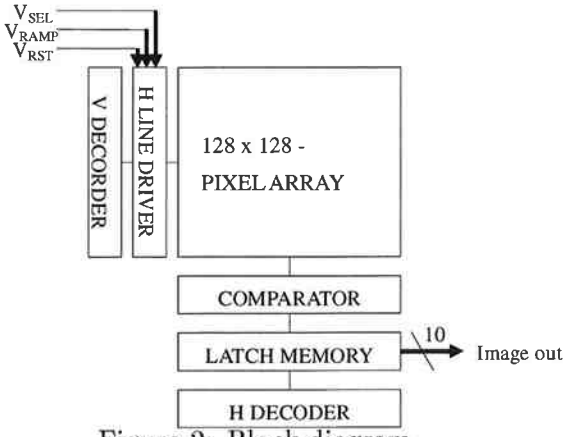

Figure 2: Block diagram.

A pixel structure of the proposed PWM image sensor is shown in Fig. 1. The pixel is composed of an in-pixel amplifier (AMP) working as a comparator, the capacitor (C_{RAMP}), a reset transistor (M_{RST}), and a row select transistor (M_{SEL}). AMP and C_{RAMP} convert the photodiode (PD) voltage to a digital pulse with the corresponding width. A simple source-common amplifier composed of one NMOS and one PMOS transistors is used as an in-pixel amplifier. The advantages are as follows: it operates at a low power-supply voltage around 1.0 V and consumes less area than the other high-gain amplifiers, and the input-referred noise is expected to be smaller than the source-follower-based image sensors because this amplifier has gain of about 10-30.

Figure 2 illustrates a block diagram of a prototype chip of the PWM image sensor. The specifications and characteristics are summarized in Table 1. It consists of a 128x128-pixel array, vertical and horizontal address decoders, horizontal line driver, comparators, and 10-bit digital latch memories. The sensor has been fabricated in a standard 0.35-μm CMOS technology. The comparator is designed to realize a large gain because the gain of the in-pixel amplifier(A_{pix}) is not sufficient for 10-bit analog-to-digital conversion (ADC). Therefore column amplifier whose gain is A_{column} is requred. The transition period(T_{trans}) where the output signal change from LOW to HIGH is described as follows:

$$\Delta T_{trans} = \frac{V_{dd}}{A_{total}\frac{\Delta V}{T_H}}. \tag{1}$$

Where T_H is the period applying a ramp signal and A_{total} is the product of the in-pixel amplifier gain and the column amplifier gain(A_{column}). $\Delta V$is an amplitude of the ramp signal.
T_{1LSB} which represents one LSB period for N-bit analog-to-digital conversion is described as eq. 2.

$$T_{1LSB} = \frac{T_H}{2^N}. \tag{2}$$

Suppose that $\Delta T_{trans} \approx T_{1LSB}$ and $\Delta V \approx \frac{1}{2}V_{dd}$ for simplicity, total gain(A_{total}) should be 2^{N+1}. Column amplifier gain requires at least a few decades for 10-bit digital output.

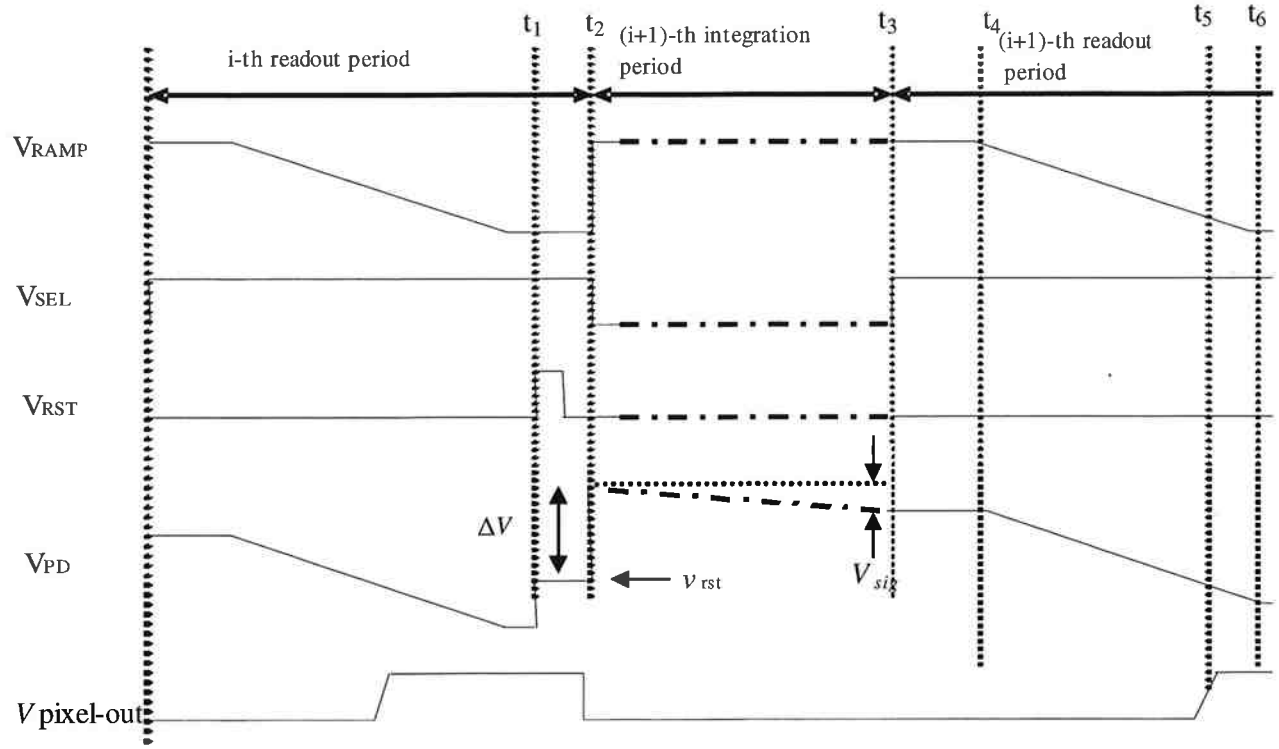

Figure 3: Timing diagram.

The timing diagram of the PWM image sensor is shown in Fig. 3. After the pixel is reset to v_{rst} at t_1, the voltage of PD is promptly pulled up by ΔV introduced by V_{RAMP} through C_{RAMP} at t_2. The period t_2-t_3 is dedicated to integrating the photocurrent at the PD. The PD voltage just after the integration period is described as eq. 3

$$V_{pd}(t_3) = v_{rst} + \Delta V - \Delta V_{sig}. \tag{3}$$

In-pixel ADC starts at t_4. By applying a falling ramp waveform on V_{RAMP} from t_4 to t_6, the PD voltage gradually goes down. At the initial condition (t_4), $V_{pixel-out}$ is LOW. Once the voltage

of PD reaches the reset voltage (v_{rst}), the output signal of the AMP turns to HIGH at t_5.

$$V_{pd}(t_5) = v_{rst} + \Delta V - \Delta Vsig - \frac{\Delta V}{t_6 - t_4} \cdot (t_5 - t_4) = v_{rst}. \tag{4}$$

Considering $t_5 - t_4 = (t_6 - t_4) - (t_6 - t_5)$, ΔV_{sig} can be described as follows.

$$\begin{aligned} \Delta Vsig &= \Delta V \cdot (1 - \frac{t_5 - t_4}{t_6 - t_4}). \\ &= \Delta V(1 - (1 - \frac{t_6 - t_5}{t_6 - t_4})) \\ &= \Delta V \frac{t_6 - t_5}{t_6 - t_4} \\ &= \Delta V \frac{t_6 - t_5}{T_H} \end{aligned} \tag{5}$$

Note that the period t_5-t_6 is proportional to the quantity of the incident light. The digital value of the period is stored by the 10-bit latch memory at the rising edge of the $V_{pixel-out}$. Pixel-to-pixel variations of the reset voltage are cancelled because the rising time of the $V_{pixel-out}$ does not depend on the reset voltage directly but on the voltage swing from the reset voltage.

3 Experimental Results

Figure 4 shows DC responses of 4 pixel-amplifiers. They have variations in offset voltages and gains which can cause fixed pattern noises to degrade image quality. Suppose that the threshold voltage of column amplifier is constant. When root mean square of variations in the reset voltages are denoted by Δv_{rst},

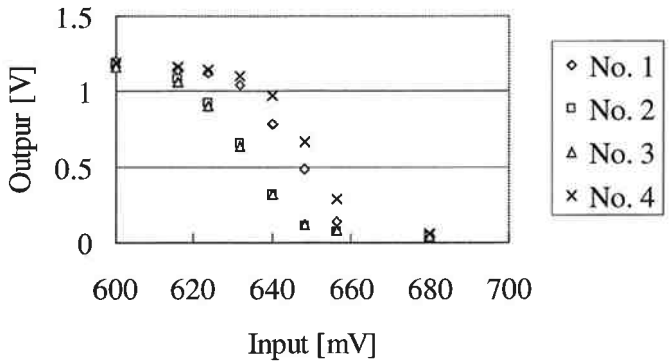

Figure 4: Measured DC responses of 4 pixel-amplifiers. The power supply voltage is 1.5V.

$$t_{variation} = \frac{\Delta vrst}{A_{pix}}. \tag{6}$$

The variations of reset voltage are suppressed by the pixel amplifier gain, so it is not noticeable when A_{pix} is large enough (typically, more than tens).

Figure 5 shows dependencies of the power consumption at the pixel array and the dynamic range on the power supply voltage of the in-pixel amplifier. The dynamic range is defined as eq. 7.

$$DR = 20\log(\frac{T_H}{\delta t_H}). \tag{7}$$

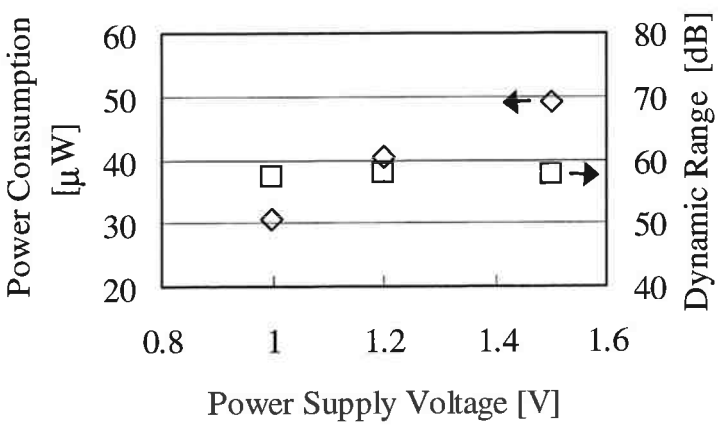

Figure 5: Measured power consumption at pixel array and dynamic range.

Figure 6: A captured image.

where δt_H is a jitter noise of the pixel out.
The jitter noise is measured with an oscilloscope. The results show that the power consumption decreases in proportion to the power supply voltage, while the dynamic range remains almost constant around 57dB. Figure 5 shows a captured image at 1.0-V power-supply voltage. Note that the power supply voltage of the digital circuits such as decoders and latch memories is 2.8 V.

4 Conclusions

We have demonstrated 1.0-V operation of the PWM image sensor fabricated in a standard 0.35-μm CMOS technology without any low-threshold or depletion transistors at the pixel. Even in the low power supply voltage, dynamic range of 57 dB has been achieved.

References

[1] M.Nagata et al., "A Smart CMOS Imager with Pixel Level PWM Signal Processing", Symposium on VLSI CIRCUIT Dig. Tech. Papers, 14-1, pp .141-144, Jun., 1999.

Table 1: Specifications and Characteristics of the PWM Image Sensor.

Technology	0.35 μ CMOS
Pixel Size	15 $\times$15 μm sq.
Fill Factor	15 %
Frame Rate	30 fps
Power Consumption at Pixel Array	31 μW
ADC Resolution	10-bit
RMS Random Noise	0.8 mV
Dynamic Range	57 dB@1.0 V