R33 A Wide Dynamic Range CMOS Image Sensor with Multiple Exposure Time Signals and Column-Parallel Cyclic A/D Converters

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***Abstract*— A wide dynamic range CMOS image sensor with a burst readout multiple exposure method is proposed. In this method, maximally four different exposure-time signals are read out in one frame period. To achieve the high-speed readout, a compact cyclic analog to digital converter(ADC) with noise canceling function is proposed and arrays of the cyclic ADC's are integrated at the column. A prototype wide dynamic range CMOS image sensor has been developed with 0.25μm 1-poly 4-metal CMOS image sensor technology. The dynamic range is expanded maximally by a factor of 1791 compared to the case of single exposure. The dynamic range is measured to be 19.8b or 119dB. The 12b ADC integrated at the column of the CMOS image sensor has the DNL of +0.2/-0.8LSB.**

I. INTRODUCTION

Cameras for automobile, scientific and industrial applications often require very wide linear dynamic range with consistently high SNR in whole illumination range. Numerous methods to expand the dynamic range of the CMOS image sensor have been reported. The methods can be classified into two categories. One uses non-linear response of the pixel devices or circuits. The use of logarithmic response[1], the combination of linear and logarithmic responses [2] and well capacity adjusting [3] are well known. The other group uses two or more exposure time signals to expand the dynamic range. A dual sampling method using the difference of the signal readout timing[4], and a multiple sampling technique using an in-pixel ADC[5] have been reported. Since most of applications require low-noise high-sensitivity characteristics in imaging of dark region as well as the dynamic range expansion to bright region, the availability of a low-noise high-sensitivity pixel device with pinned photo-diode structure[6] is particularly important. The dynamic range expansion methods with non-linear response of the pixel are not compatible with the pinned photo-diode structure. The latter group of the methods using two or more exposure time signals usually allows us to use the pinned photo diode structure in the pixel.

This paper presents a new type of wide dynamic range image sensor with multiple exposure time signals. Our method uses high-speed signal readout mode in CMOS image sensors, and maximally four different exposure time signals are read out within one frame period. The read image signals are synthesized in the external system. This method provides many advantages for high-quality wide dynamic range imaging at the expense of complexity of an external system and frame memories. First, the image capturing conditions such as the number of different exposure times and the choice of each exposure time can be flexibly controlled in real time. Second, the four different exposure times are sufficient for expanding the dynamic range to 120dB while maintaining a sufficient image quality. Any types of pixel devices and circuits can be used, and therefore, a CMOS image sensor with low-noise characteristics as well as wide dynamic range can be realized if the device technology of the pinned photodiode is available. Furthermore, the image can be treated as a very wide linear digital data. This property is particular important if the wide dynamic range image is used for image recognitions in real world applications such as automobile, biometrics, and security systems.

As a key device for reading four different exposure time signals in one frame period with sufficient image quality, this paper introduces a new type of column parallel cyclic ADC with 12b resolution. The proposed cyclic ADC with a built-in pixel noise canceller uses a single operational amplifier per column. This compact configuration allows us to integrate the array of the ADC at the column of the 1/2 inch VGA-size CMOS image sensor.

II. DYNAMIC RANGE EXPANSION METHOD

The proposed burst readout multiple exposure(BROME) method is based on a high-speed signal readout mode in CMOS image sensors. In conventional CMOS image sensors, one frame image signal is read out in whole frame period T_F. In the burst readout method, one frame image signal is read out in time T_R, which is a fraction of the frame period. The ratio T_F/T_R is denoted by M, and M is chosen as a positive integer. The signal accumulation and readout timing of the BROME is shown in Fig. 1 for M=6 and N_A = 4, where N_A is the number of different accumulation-time signals. Fig. 1 is a conceptual diagram and it is assumed that the sensor has 5 vertical pixels. One long and three short accumulation-time signals are read out in a frame period. The long, short, very short and extremely short accumulation are denoted by LA, SA, VSA and ESA, respectively. The LA signals occupy three slots ($3T_R$) for signal accumulation. Using the time slots for reading the LA signals, the SA signals are accumulated.

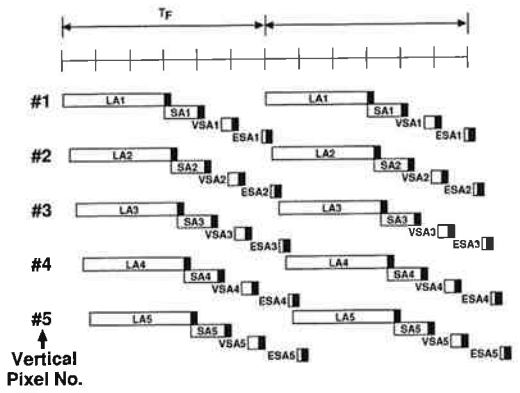

Fig. 1. Accumulation and readout timing of the wide dynamic range CMOS image sensor.

The VSA and ESA signals are accumulated using the time slots for reading the SA and VSA signals, respectively. The accumulation time of the SA, VSA and ESA signals can be controlled to be shorter than T_R by resetting the pixel during accumulation using an additional vertical scanner for resetting. The dynamic range expansion ratio is determined by the ratio of long accumulation time and the shortest accumulation time. The long accumulation time T_{LA} is given by

$$T_{LA} = T_R(M + 1 - N_A) \tag{1}$$

and while the minimum accumulation time $T_{S,min}$ is given by

$$T_{S,min} = \frac{T_R}{N_V} - T_{WR}. \tag{2}$$

where N_V represents the number of vertical pixels, and T_{WR} is the reset pulse width. Therefore, the minimum accumulation-time can be set to a value which is a little shorter than the horizontal readout period. The maximum dynamic range expansion ratio is given by

$$\Delta DR = T_{LA}/T_{S,min} \tag{3}$$

In the design of a VGA-size image sensor with $N_V = 480$, $M = 6$ and $N_A = 4$, and $T_{S,min}$=(1/597)T_R, the dynamic range is expanded by a factor of 1791 or 65.1dB. An advantage of the wide dynamic range CMOS image sensor with the multiple exposure method is that a relatively high SNR is kept in whole illumination range. In the dual sample method which reads one long and one short accumulation-time signals in one frame period, the SNR dip at the boundary of high and low illumination region increases as the time ratio of long to short exposures increases[5]. If the noise level is dominated by photon shot noise, the SNR dip when the accumulation time is switched from T_i to T_j is given by

$$SNR_{dip} = 10\log_{10}(T_i/T_j). \tag{4}$$

In the proposed method, by choosing each accumulation time ratios of LA to SA, SA to VSA and VSA to ESA to be minimum, the SNR dip can be sufficiently reduced at each boundary. For example, assuming that the dynamic range expansion ratio is 1000, M = 6 and N_A = 4, the best choise for each accumulation time ratio is 10, and the ideal SNR dip is 10dB. In the case of the dual sampling, the SNR dip will be 30dB for the dynamic range expansion ratio of 1000.

In the proposed wide dynamic range image sensor, the image capturing conditions of wide dynamic range image can be flexibly and adaptively changed to the scene. The image capturing conditions include the number of different accumulation-time signals(N_A) and each accmulation-time, which can be determined by a histogram of each accumulation-time signal.

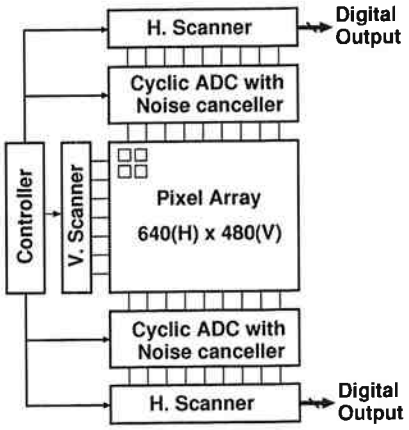

Fig. 2. Block diagram of the proposed wide dynamic range CMOS image sensor.

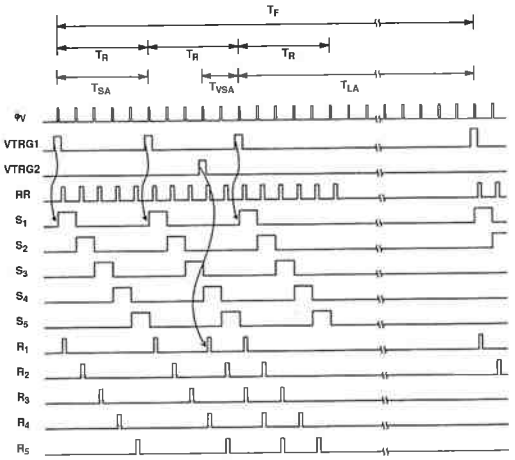

Fig. 3. Reset timing of a pixel.

III. IMAGE SENSOR DESIGN

A. Architecture

Figure 2 shows a block diagram of the wide dynamic range CMOS image sensor. The upper and lower ADC arrays are for odd and even columns, respectively. The implemented wide dynamic range CMOS image sensor has two vertical shift registers for signal readout and resetting. The timing diagrams of the dual vertical shift register is shown in Fig. 3. The timing diagram of Fig. 3 shows the case that the sensor has 5 vertical pixels and 3 accumulation signals are read out. Trigger pulses VTRG1 and VTRG2 are used for the signal readout and resetting, respectively. The both shift registers are operated by a clock pulse ϕ_V. The reset pulse width and the actual timing are determined by a pulse RR. In Fig. 3, T_F is a frame period, T_R is readout time and T_{LA}, T_{SA} and T_{VSA} are the accumulation times for the long, short and very short, respectively. The accumulation time is determined by the internal of the adjacent VTRG1 pulses if the VTRG2 pulse is not given. In Fig. 3, T_{LA} equals to multiple of T_R, T_{SA} is equals to T_R, and T_{VSA} is determined by the interval between the VTRG2 pulse and the next VTRG1 pulse.

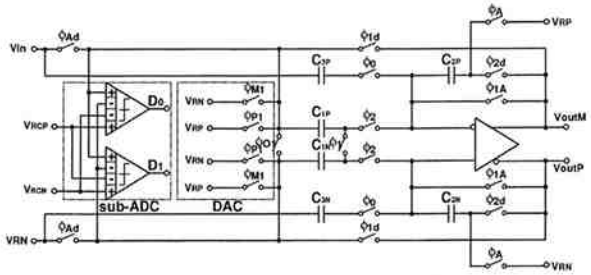

Fig. 4. Shematic of the cyclic ADC.

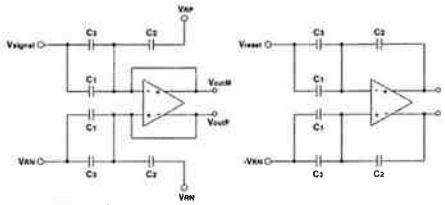

Fig. 5. Equivalent circuits for the noise cancelation mode.

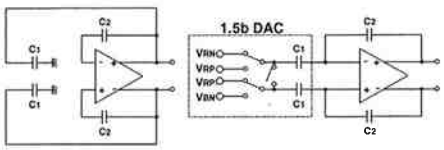

Fig. 6. Equivalent circuits for the cyclic ADC mode.

B. Column-Parallel Cyclic ADC's

A schematic of the cyclic ADC with a built-in noise canceller is shown in Fig 4. It consists of an amplifier, six capacitors, two comparators and switch transistors. This ADC works as an ADC with 1.5b per cycle algorithm[7]. A straight-forward cyclic ADC consists of sample-and-hold and gain stages[8]. A noise canceller is necessary in front of the ADC. In the proposed method, an amplifier and capacitors are shared for the noise canceller, the sample and hold and 1.5b gain stages. The power dissipation and the size can be sufficiently small for the column integration.

Fig. 5 depicts the equivalent circuits for the operation of the pixel noise canceling. In the signal sampling phase of the noise cancellation mode, the signal level of the pixel output V_{signal} is connected to the bottom plates of capacitors C_{1P} and C_{3P}, and a reference singal V_{RN} is connected to the bottom plates of capacitors C_{1N} and C_{3N}. The bottom plates of capacitors C_{2P} and C_{2N} are connected to reference signals V_{RP} and V_{RN}, respectively. The switches controlled by ϕ_0, ϕ_{Ad}, ϕ_A, ϕ_{1A} and ϕ_2 are turned on in the signal sampling phase. The signal level is sampled when the switches controlled by ϕ_A and ϕ_{1A} are turned off. In the reset sampling phase, the reset level of the pixel output V_{reset} is given to C_{1P} and C_{3P}. After that, the switch controlled by ϕ_{2d} is turned on, and the bottom plates of C_{2P} and C_{2N} are connected to the amplifier output. The reset level is sampled when the switches controlled by ϕ_0 and ϕ_{Ad} are turned off. After these operations, the differential output V_{out} is given by

$$V_{out} = \frac{C_{1P} + C_{3P}}{C_{2P}} \Delta V_{sig} - V_R \tag{5}$$

where $V_{out} = V_{outP} - V_{outM}$, $\Delta V_{sig} = V_{reset} - V_{signal}$ and $V_R = V_{RP} - V_{RN}$. By choosing all capacitors are equal, the difference V_{reset} - V_{signal} is amplified by a factor of 2. In order to fit the amplified signal to the full scale, the reference voltage V_R is subtracted from the output.

At the beginning of the cyclic ADC mode, the amplifier output is sampled by the two comparators in a sub-ADC and the capacitors C_{1P} and C_{1N}. To do this, the switches controlled by ϕ_2 is turned off, and the switches controlled by ϕ_1 and ϕ_{1d} are turned on. In the 1.5b/cycle algorithm, a digit set of -1, 0, 1, or a set of digital codes, 00, 01 and 10 excluding 11, is used. An important property of the 1.5b/cycle algorithm is that the comparator offset up to -(1/4) $V_R \leq V_{off} \leq$ (1/4) V_R can be corrected in digital domain[9]. This property of the 1.5b/cycle algorithm greatly relaxes the comparator precision and leads to a great reduction of power dissipation of comparators.

In the amplification phase, as shown in Fig. 6(b), the bottom plates of the capacitors C_{1P} and C_{1N} are connected to a 1.5b DAC using the decision results of the comparators. To do this, the switches controlled by ϕ_2 is turned on, the switches controlled by ϕ_1 and ϕ_{1d} are turned off. Then the relationship between the input and output of the i-th cycle of the ADC is given by

$$\begin{aligned} V_{out}(i) &= \frac{1}{2}\left(2 + \frac{C_{1P}}{C_{2P}} + \frac{C_{1N}}{C_{2N}}\right) V_{out}(i-1) \\ &\quad - D(i)\frac{1}{2}\left(\frac{C_{1P}}{C_{2P}} + \frac{C_{1N}}{C_{2N}}\right) \end{aligned} \tag{6}$$

where $D(i)$ is the sub-ADC output and $V_{out}(i)$ is the output of the i-th cycle. If C_{1P} = C_{2P} and C_{1N} = C_{2N}, Eq.(6) is simplified to

$$V_{out}(i) = 2V_{out}(i-1) - D(i)V_R. \tag{7}$$

The i-th sub-ADC output D(i) is given by

$$D(i) = \begin{cases} 1 & (if \quad V_R/4 < V_{out}(i-1)) \\ 0 & (if \quad -V_R/4 \leq V_{out}(i-1) \leq V_R/4) \\ -1 & (if \quad V_{out}(i-1) < -V_R/4). \end{cases} \tag{8}$$

The comparator reference voltages, V_{RCP} and V_{RCN} are chosen such that V_{RCP} - V_{RCN} = (1/4)V_R. For 12b resolution, the above operation is repeated for 11 times. The designed cyclic ADC dissipates 149μW at supply voltage of 3.3V and clock frequency of 3.75MHz. For 12b resolution, the conversion time is 2.9μs.

IV. EXPERIMENTAL RESULTS

A prototype wide dynamic range CMOS image sensor which has outputs of maximally 4 different exposure-time signals in one frame is designed and implemented. A chip microphotograph of the developed wide dynamic range image sensor with 0.25μm 1P 4M CMOS image sensor technology is shown in Fig. 7. The image array has 664 $\times$ 448 pixels with the pixel size of 10μm $\times$ 10μm. The chip size is 8.34mm $\times$ 9.84mm. Two sets of a 332 cyclic ADC array are integrated at the upper and lower sides of the image array.

Fig. 8 shows an image taken by the developed wide dynamic range image sensor. Three different exposure time signals of $2T_R$, (1/16)T_R and (1/256)T_R are synthesized. The both regions of inside and outside of the tunnel is captured clearly with good contrast.

The SNR characteristic of the developed wide dynamic range CMOS image sensor is measured as shown in Fig. 9. In this case, The accumulation-time ratios of long (LA) to short

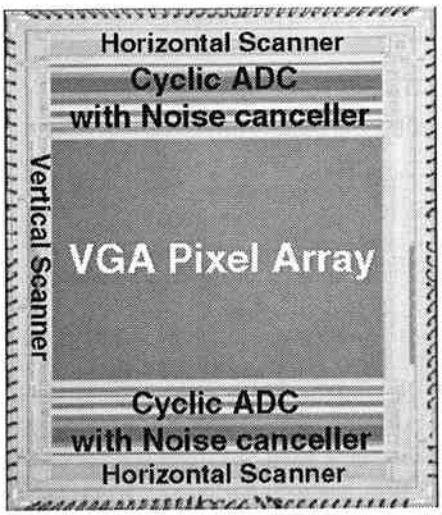

Fig. 7. Chip Microphotograph.

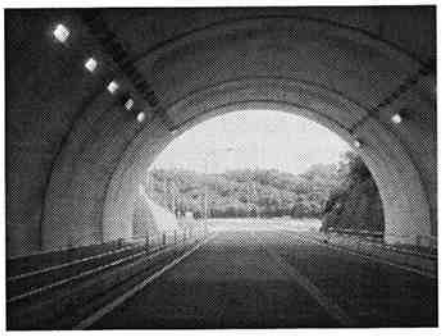

Fig. 8. Sample image taken by the developed wide dynamic range image sensor.

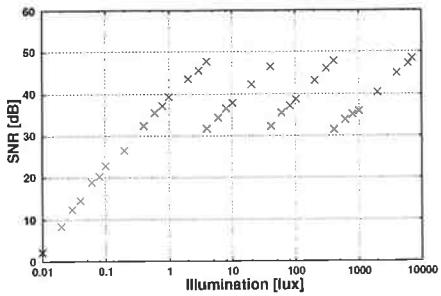

Fig. 9. SNR of the prototype wide dynanic range image sensor.

(SA), very short (VSA) and extremely short (ESA) are set to 1/12, 1/96, and 1/1791, respectively. In other words, the ratios of LA to SA, SA to VSA and VSA to ESA are 1/12, 1/8 and 1/18.7, respectively. The measured SNR dip at the boundaries of LA to SA, SA to VSA and VSA to ESA is 16dB, 14dB and 16dB, respectively. These are larger than the theoretical SNR dip if the noise is limited by photon shot noise. This is because of the relatively large readout noise, and the small conversion gain in this experimental chip.

The measured 12b differential nonlinearity (DNL) and integral nonlinearity(INL) are within -0.8/+0.2 LSB, and -8.0/+1.0 LSB, respectively. The input referred random noise is 6.2LSBrms. A single-channel cyclic ADC with the same design as that integrated at the column of the image sensor is also implemented in a test chip. The maximum DNL and INL in 12b resolution are within -0.8/+0.6 LSB, and -4.0/+3.9 LSB, respectively. The input referred random noise is 2.7LSB($667\mu V$) in 12b.

The performance of the developed CMOS image sensor is summarized in Tabel I. The maximum accumulation time ratio is 1791 to 1, or 10.9bits. From the noise measurement results, the dynamic range is measured to be 19.8bits or 119dB.

TABLE I

PERFORMANCE OF THE DEVELOPED CMOS IMAGE SENSOR.

Technology	0.25 μm CMOS 1P4M
Chip size	8.34mm(H) × 9.84mm(V)
Array size	664(H) × 488(V)
Pixel size	10 μm × μm
Fill factor	54.5%
Sensitivity	5.92V/lx-sec
Fixed pattern noise	< 0.1% (p-p)
Dark current	16mV/s(@27°C)
ADC resolution	12b
ADC DNL/INL	(+0.2, -0.8) / (+1.0, -8.0)
Saturation signal	1000mV
Maximum exposure time ratio	× 1791 (10.9b)
Digital dynamic range	19.8b(916992:1 mesured)
	or 119dB
Power supply	2.5(Digital) / 3.3(Analog)
Power consumption	130mW(@30fps)

V. CONCLUSION

In this paper, a wide dynamic range CMOS image sensor with 12b column-parallel high-speed cyclic ADC's has been described. The developed image sensor can capture maximally four different accumulation-time signals in one frame. The dynamic range is expanded by 65.1dB. The 12b cyclic ADC with the noise canceling function integrated at the column has a sufficient linearity. The resulting dynamic range is 119dB. A clear wide dynamic range image keeping relatively high SNR in all the illumination range can be synthesized using the image signals captured by the developed CMOS image sensor.

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