

## The design and characterization of CMOS image sensor with active pixel array of $2.0\mu\text{m}$ pitch and beyond

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### I. Introduction

As the application of CIS is being focused on mobile solution and demand for better imaging quality is increased, the high pixel density up to several millions is required in consumer imaging devices and it makes device maker shrink down the pixel size further down to  $2.0 \times 2.0 \mu\text{m}^2$  and beyond in a few years as shown in Fig.1. Since the dynamic range and S/N should be maintained even though the pixel size becomes smaller, it is required that the aperture area ratio should be increased by decreasing the area of the rest parts consisting of transistors. Both sharing transistors with adjacent pixels or applying tighter design rules are the most effective approaches for the reduction of that area[1][2]. And more, the aperture width for the small pixel pitch becomes narrow and to be comparable to the wavelength of light. It makes another problems including sensitivity falling down and cross-talking[3].

In this work, a new pixel design concept to implement a smaller pixel size and the measured results will be shown. CMOS image sensor as a logic compatible product is expected to follow logic DR. However, introduction of specific DR for APS array could give a room to transistor layout or enhancing PD area. as this work. Comparable pixel characteristics could be obtained.

### II. Design Rule and Process integration

Typically, the area of a logic chip becomes about half as the technology node changes by one generation. However, the shrinking rate of the circuit part area in CIS pixel is lower than that of typical logic chip area as shown in Fig.1. It is mainly because the pixel driving voltage is almost fixed to about 2.8V for getting proper dynamic range and the in-pixel-transistors should have enough large length and width to reduce the random noise largely due to  $1/f$  noise of SF transistor and cut-off leakage current of transfer gate.

Until now, the pixel design rules have been based on those of the standard logic process for the fabrication of highly integrated logic circuits, which are focused on random pattern and high performance with small size and low voltage driving. APS pixel based on 130nm design rule was already developed and the mega pixel image sensors with  $2.8\mu\text{m}$  pitch pixels are under mass production. Full 90nm logic DR could be introduced but APS pixel optimization based on full 90nm logic DR is believed to have burden due to limited thermal budget.

As mentioned above, the operation voltage should be optimized by concerning the transistor size and aperture ratio and a simple modeling about operation voltage and aperture ratio is performed. In the

calculation, the photodiode area is increased as the pixel circuit area decreased by smaller design rule and the photodiode charge handling capability calculated as the product of photodiode area and operation voltage which is also scaled by design rule. Fig.3 shows the result and it can be known that the capability becomes maximum value with 0.25  $\mu\text{m}$  design rule for photodiode area of 1~2  $\mu\text{m}^2$ . The selected operation voltage is 2.5V. For the pixel shrinkage, the critical and non-critical design rules are investigated. The final pixel design rules mixed from 90nm and 130nm technology. Though some design rules are tighter than 90nm standard logic design rule, the final layout patterns are trimmed and confirmed by photo lithography simulation. Fig.4 shows the typical optical proximity correction results.

The shallow trench isolation(STI) process is applied for isolation while introducing field implantation under STI to suppress dark current from STI oxide interface state. Basic scheme adopted 1P4M processes with MIM capacitors. In the pixel region, S/D and Poly was not silicided, whereas logic SD region and gate was silicided with masking layer. Silicide blocking layer which was the SiN and SiO<sub>2</sub> double layer, and metal contact stopper material was optimized as anti-reflecting layer to maximize the incident light into Si by mitigating the large refractive index difference between ILD/IMD SiO<sub>2</sub> and Si. By Proper application of manual OPC and ArF patterning to metal layer, random 0.12 $\mu\text{m}$  Al metal patterning was delineated on the pixel region, as mentioned above. As for ILD & IMD, HT-USG and HDP material was used. Because M4 layout could be used in the logic region, pixel height to the lens bottom could be larger than 5 $\mu\text{m}$ . With varying top lens height or refractive index, they could optimize the focal point on photodiode. Or, they could reduce the height itself to the lens bottom by oxide removal on the pixel region only, which had the nominal focal length. In order to reduce optical cross-talk, they might use light-guiding structure in addition to proper layer shift including u-lens, Color-filter and metals on the photo-diode.

### III. Pixel Characteristics

To measure various pixel characteristics, the test patterns with 80 $\times$ 80 pixel array including 8 lines of optical black pixels for each sides. Saturation and dark level should be controlled with lag-free condition. As known, PD capacity, in other words, saturation is determined by the PD capacitance and PD max. potential. PD capacitance is inversely proportional to PD max. Potential position and proportional to PD area, which drive them to maximize PD fill factor. Also, floating diffusion conversion efficiency could be increased to satisfy the larger saturation level. As for getting lag-free condition, they could adopt TG boosting concept to transfer charge to Floating diffusion thoroughly, in addition to tuning NPD implantation and channel implantation under transfer gate. To suppress the dark level, oxide interface state just below transfer gate and STI boundary needs to be reduced with care. The final pixel structures for each pixel sizes are optimized by utilizing full 3-D process and device simulation tools[4].

By this way, we could increase the ratios of photo-diode area and the optical aperture up to about 50%, and obtain proper characteristics in 2.0 $\times$ 2.0 $\mu\text{m}^2$  pixel array with conventional 4 Tr. structures. The key characteristics for 2.2 $\mu\text{m}$  and 2.0 $\mu\text{m}$  pixels are listed in the table 1. To minimize dark level, proper passivation of Si-SiO<sub>2</sub> interface is necessary and further area of Si-SiO<sub>2</sub> interface resulting in dark current increase should be minimized. In this work, we could reduce dark level below 20mV/sec, in other

words,  $< 220e/sec$  at 60 Degree Celsius, which was partly ascribed to optimizing profile of potential barrier toward floating diffusion [Fig. 5] and passivation methodology. Random noise which is spatial standard deviation of dark noise is mainly due to SF transistor flicker noise and PD dark level. By optimizing oxide quality and anneal condition including alloy anneal [Fig. 6], random noise could be reduced less than 10LSB.

#### IV. Conclusion

There is the trend of Pixel size shrinkage while pixel voltage and oxide thickness are hardly scalable. It could be compromised by introducing special pixel DR different from peri/logic DR. Under that concept, 80x80 pixel array with varying pixel size was designed and fabricated, while a full CIS chip in which 2.2 $\mu m$ -pitch 1.3M pixel array and peripheral circuits including column ADC and timing generator with 130nm design rule was fabricated. Fully working die in which all pixels have uniformly equivalent sensitivity and saturation level could be obtained. And comparable characteristics were obtained for 2.0 $\mu m$ -sized 4-Tr. Type pixel. Further study is necessary to clarify the scalability of CIS to sub 2.0 $\mu m$  in terms of lens optics including module integration.[5]

#### References

- [1] H. Takahashi et al., ISSCC, pp.108-109, 2004.
- [2] M. Kasano et al., ISSCC, pp.348-349, 2005.
- [3] H. Rhodes et al., IEEE Workshop on Microelectronics and Electron Devices, pp.7-18, 2004.
- [4] ISE TCAD Release 9.0 Manual, Integrated Systems Engineering, 2003
- [5] To be published.

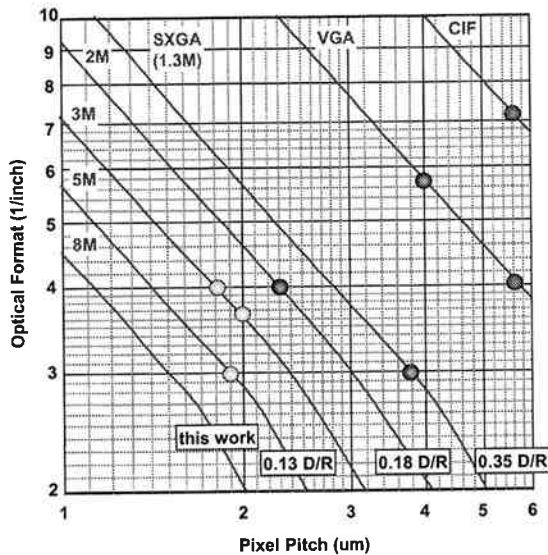


Fig.1. Sensor resolution and unit pixel pitch.

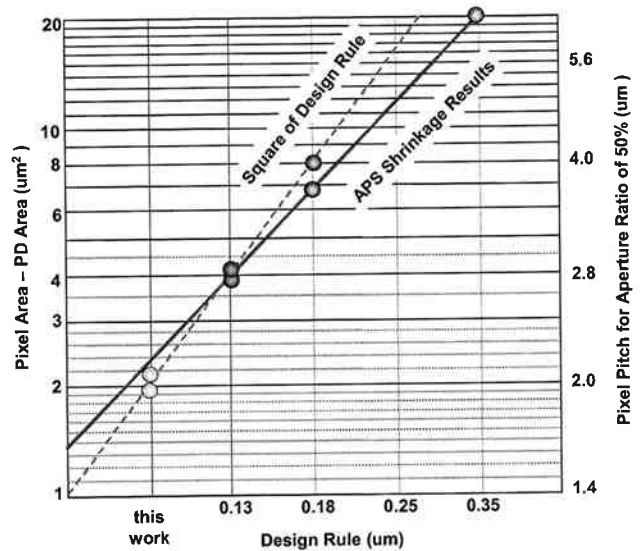


Fig.2. Shrinkage trend of the circuit area for an active pixel

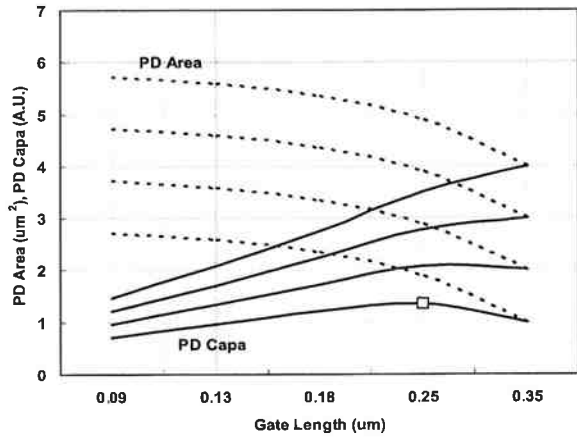


Fig. 3 Photodiode capability calculation results.

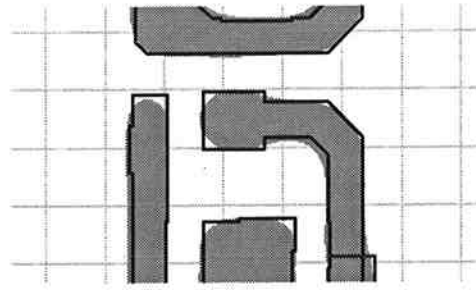


Fig.4. M1 OPC Example ( 2.0um Pixel )

Table 1. The measured pixel characteristics of APS test pattern without color filter and micro-lens.

Pixel pitch	2.2 $\mu\text{m}$	2.0 $\mu\text{m}$
Sensitivity	1500 mV/lux sec @BW	1100 mV/lux sec @BW
Saturation Level	700 mV	450 mV
Dark Level	< 20 mV/sec @60°C	< 20 mV/sec @60°C
Image Lag	None	None

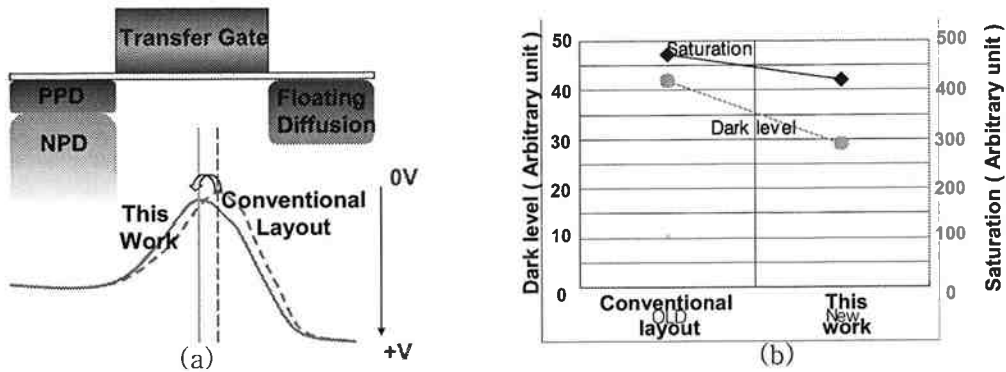


Fig. 5 Dark level reduction by potential profile optimization under transfer gate, (a) potential profile optimization, (b) dark level dependence on potential profile

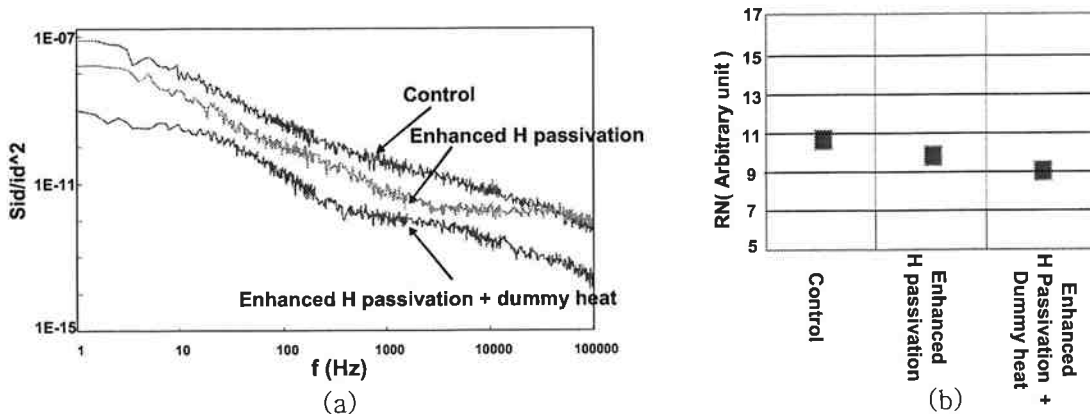


Fig. 6 Random noise depending on Anneal condition (a) Flicker noise of Source Follower Transistor (b) Random noise