A 4M Pixel CMOS Image Sensor for High Speed Image Capture

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Abstract

This article describes a 4M pixel, 60 frame per second CMOS image sensor designed for high speed machine vision applications. The sensor employs a 5-transistor pixel and features snapshot image capture, electronic exposure control, and simultaneous integration and readout. The analog data is processed and digitized by two column-parallel signal chains, and the digitized data is routed through dual high speed column multiplexers to two differential output taps each ten bits wide and operating at a data rate of 160MHz.

I. Introduction

There has been much development of CMOS image sensors for digital still photography, mobile applications, and other applications where the final image will be viewed by a human[1-3]. However, there has been comparatively little development of image sensors that are optimized for machine vision applications[4,5]. As a result, interline transfer (ILT) CCD technology has remained the image sensor technology of choice for cameras targeted to industrial applications such as electronics inspection, traffic inspection, and industrial metrology.

In this paper, we describe a 4 MPixel CMOS image sensor that has been developed specifically for machine vision applications and exceeds the performance achieved with comparable ILT CCD technology. The pixel architecture allows for global shuttering with electronic exposure control, and the signal chain is capable of reading the array at up to 60 frames per second.

II. Pixel Architecture

The pixel is based on a 5-transistor architecture as illustrated in Figure 1. Signal charge is collected on the photo site during the integration phase. Prior to integration PR is held high and photo charge is drained to VPR. Integration begins when PR is clocked to low and continues until the TCK gate is clocked high. Then, signal charge is spilled into the storage node. The TCK and PR gates are addressed globally. Charge in the sense node is converted to a voltage which is buffered onto the column signal bus on a row-wise basis and is sampled at the base of the column. Following each row read the storage nodes for the row are reset through the RST gates. The reset storage node levels are sampled. The two sampled levels are differenced in column-wise switched capacitor amplifiers in order to correct for offset differences in the pixel buffers and resistive voltage drops in the column buses.

This circuit topology allows for synchronous charge integration (no rolling shutter artifact) in conjunction with electronic exposure control (signal integration during a portion of the frame read out time) and with simultaneous image capture and frame readout (100% temporal coverage and maximum use of the available optical signal). There are other circuit topologies and clocking schemes that can be used to achieve the same combination of functionalities. For example, if a sixth transistor is added to the pixel then the photo charge can be sensed directly on the photo site as a voltage and buffered to an in-pixel sample-and-hold capacitor. This can be advantageous in terms of minimizing the contamination of the signal stored on the in-pixel memory elements, however other considerations make this solution less favourable: fixed pattern noise (FPN) that cannot be easily differenced on-chip; reduced voltage swing in the pixel; higher temporal noise; and reduced fill factor. An alternative clocking of the 5T pixel eliminates the spill of signal charge from the photo site to the sense node but has higher reset noise. Similarly, a 4T pixel can be configured to operate with a synchronous shutter, however one needs to sacrifice either electronic

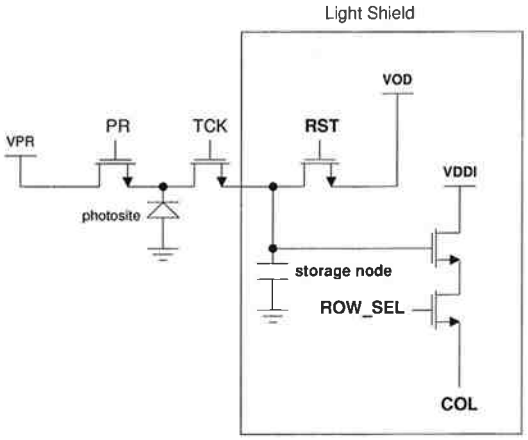

Figure 1: Schematic of 5-transistor pixel.

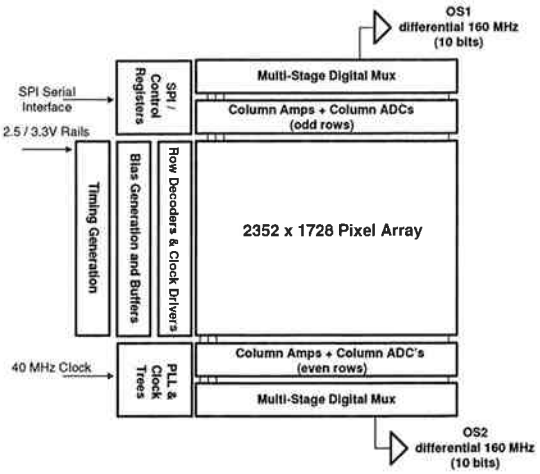

Figure 2: Block diagram of image sensor

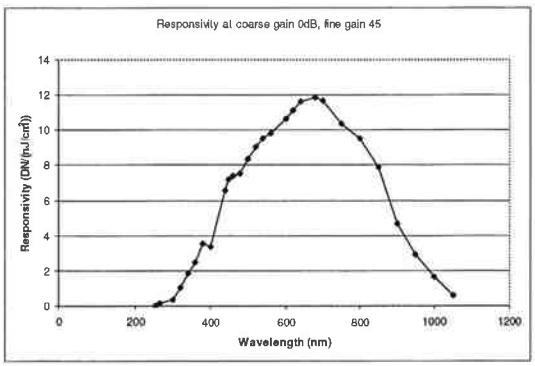

Figure 3: Spectral response curve

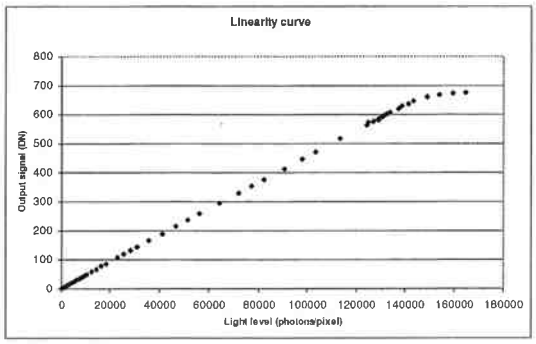

Figure 4: Output Linearity at minimum sensor gain, showing the pixel saturation level. The nominal gain setting is defined such that the analog chain and output saturate with the pixel.

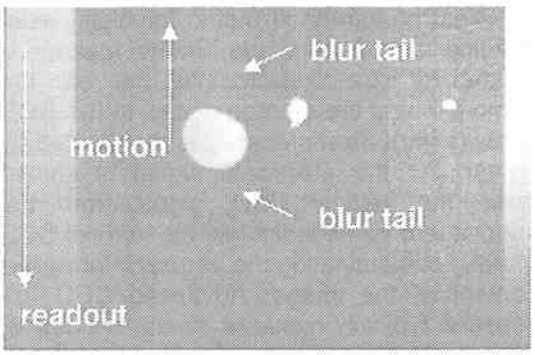

Figure 5: Example of high speed image capture. The exposure time is 20 µs and the frame time is 33 ms. The scene moves 0.4 frames between exposures. The signal magnitude in the blur tail is approximately 10% of the signal level in the dot.

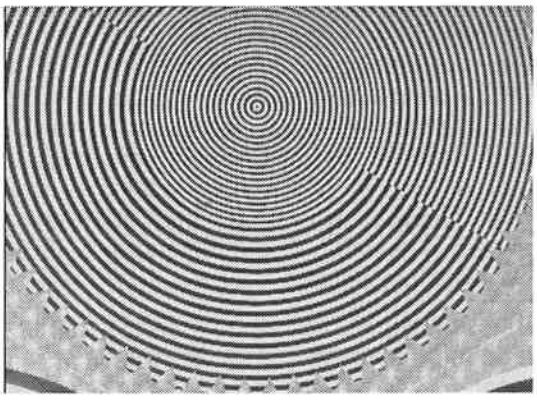

Figure 6: Sample Still Image

exposure control or the ability to simultaneously integrate and readout.

Machine vision applications typically offer high illumination levels. The well capacity and photosensitive area per pixel therefore need to be larger than in most consumer image sensors. For a 4M pixel array, 7.4 µm is close to the maximum pixel pitch that can be accommodated in a single reticle field. The device described in this paper was targeted to a 0.25 µm dual-oxide triple-metal fabrication process. The dual-oxide process allows for a higher voltage rail in the pixel array and in turn a larger well capacity. By optimizing both the absolute capacitances in the pixel as well as the capacitance ratio of the photo site to the sense node a full well capacity of the order of 70,000 electrons has been achieved. The use of 3 metals in conjunction with a microlens process allows for a reasonable compromise between high effective fill factor (~75%) and a low optical stack. The use of a deep pixel implant in conjunction with a shallow storage node implant has allowed us to achieve crosstalk levels between the photo site and the storage node that rival what is achieved in machine vision ILT devices.

III. Signal Chain Architecture

In order to achieve the target 60 Hz frame rate the data path needs to support an average throughput of 240 Mpixels/s and a burst rate of 320 Mpixels/s. A block diagram of the signal chain is illustrated in Figure 2. For each column in the pixel array there are two parallel analog chains. The chain at the bottom of each column processes even rows and the chain at the top of each column processes odd rows. This interleaved configuration is used to achieve maximum throughput independent of the vertical region of interest.

Each chain consists of a switched capacitor difference-and-hold preamplifier circuit followed by a 10 bit analog-to-digital converter (ADC). The ADCs are implemented in a single slope architecture which is driven by an 80 MHz on-chip ramp generator. The digital data is stored in a double buffered latch – while the data from one row is being processed by the ADC, the data from the previous row is being simultaneously read out through a high speed column multiplexer.

The column multiplexers are configured as pipelined analog switch networks and are clocked at 160 MHz. The digital data from each chain (even rows and odd rows) is driven off-chip by differential drivers at 160 MHz per channel.

There are two programmable gain stages in the analog chain to provide a gain range from -3.0dB to 8.0dB. The first gain stage is in the preamplifier circuit, where one of four coarse gain settings is selected by switching in different feedback capacitors. The second gain stage provides fine resolution by adjusting the swing of the ramp signal used in the single slope ADC.

IV. Support Circuitry

All clocks and biases are generated on-chip. A phase locked loop (PLL) is configured as a clock multiplier to allow high speed internal timing with a low frequency input clock. Region of Interest (ROI) control and digital timing are programmable to allow for higher frame readout speeds at lower resolution and for optimization of sensor performance. A serial-parallel interface provides access to the on-chip configuration registers.

The clock and bias networks were carefully designed to minimize image artifacts associated with high frame rate, large array size and snapshot imaging.

V. Sensor Characterization

A preliminary characterization of the sensor has been performed. The results are shown in Table 1 for the nominal 0dB gain setting. Figure 6 shows a sample still image

Table 1: Sensor Performance Test Results

Specification	Value	Unit
Saturation Level	1023	DN
Saturation Level	~ 70	ke^-
Responsivity	11.8 (1)	$DN/(nJ/cm^2)$
Random noise	1.2	rms DN
Random noise	82	rms e^-
Dark Offset (2)	100	DN
Dynamic range	58.6	dB
FPN (2)	20.0	DN rms
FPN (3)	2.2	DN rms
PRNU	1-2	% rms
Linearity	1 (4)	%

CCD WS R26

Specification	Value	Unit
Power	1.5	W
Antiblooming	> 200x	sat light level
Lag	< 1	%
Shutter Leakage	0.03 [5]	%
MTF [6]	> 60	%

[1] Peak, see Figure 3
[2] Electronic exposure control enabled
[3] Electronic exposure control disabled
[4] see graph in Figure 4
[5] white light source
[6] At 1.0 Nyquist and 550nm

VI. High Speed Image Capture Performance

A critical performance metric for high speed imaging is shutter leakage. Shutter leakage is caused by intra-pixel crosstalk between the photo site and the storage node. In ILT CCD sensors intra-pixel crosstalk is manifested by smear. As the electronic signal is shifted down the vertical CCD, signal from the subsequent frame leaks into the vertical CCD thereby contaminating the vertical information content of the image. Advanced CCD ILT sensors typically achieve smear values in excess of 90 dB[6] which corresponds to crosstalk of less than 1 part in 3000. In CMOS sensors intra-pixel crosstalk also leads to image contamination, however the characteristics are different. For example, images from static scenes display no artifacts – crosstalk only influences images from dynamic scenes. And the crosstalk in dynamic scenes only affects the pixels along the trajectory of the object. In general far fewer pixels in an image captured by a CMOS stop-action sensor will be affected compared to the image captured by an ILT CCD. This can be a significant advantage in applications like electronics inspection and traffic inspection where the information content is generally in the regions away from the scene highlights.

An example of high speed image capture performed with the sensor described in this paper is illustrated in Fig. 5. The test conditions were designed to exaggerate the effects of intra-pixel crosstalk. The exposure time is 20 μs and the frame time is 33 ms. The scene moves 0.4 frames between exposures. The large white spot in the lower left quadrant has a blur tail that extends up by approximately 2 spot diameters and down by approximately 1 spot diameter. The signal level in the blur region is approximately 10% of the level in the dot. The corresponding crosstalk ratio is better than 1 part in 3,000.

Conclusions:

Design details and performance results have been presented for a CMOS image sensor designed for high speed machine vision applications. The sensor captures images with 4 Mpixel resolution at 60 fps.

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