R24: Development of 2/3-type 1-mega pixel Progressive Scan CCD for HDTV capable of high frame rate of 96fps

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Abstract

We have developed a high speed 720p HDTV 2/3-type 1-mega pixel progressive scan CCD featured by a variable frame rate ranging from 1 to 96 frames per second (fps). By reducing the horizontal CCD (HCCD) gate electrodes width, by making their electrodes pitch nearly equal and by optimizing the last stage of HCCD, we have driven at HCCD frequency of 118MHz with drive voltage of 3V at 96fps. The last stage of Floating Diffusion Amplifier (FDA) is designed to switch its bias current, which results in an appropriate FDA's output impedances and bandwidth according to their frame rates. From experimental result, we have estimated FDA bandwidth of 270MHz. We will be able to achieve 300MHz bandwidth, by reducing 10% of load capacitance from the present condition.

1. Introduction

In the professional broadcasting camera market, there is a great demand for high speed High Definition CCD (HDCCD) [1], because HDTV broadcast has been increasing and a wide variety of programs are needed. In the cinema camera market, HDCCD is going to take places of film. And also there is a great demand for high speed HDCCD because movie camera which can take a wide variety images of slow motion scenes are required [2].

From these points of view, we have developed a high speed 720p HDTV 2/3-type 1-mega pixel progressive scan CCD featured by high frame rate of 96fps. We must drive at HCCD frequency of 118MHz with drive voltage of 3V at 96fps. To realize it, there are two requirements of sufficient horizontal transfer efficiency even at HCCD 118MHz and wide FDA bandwidth of 300MHz. The details to solve them are as following.

2. Technologies for high speed HCCD of 118MHz

Figure 1 shows a structure of a connecting section from VCCD to HCCD. In conventional structure, we design HCCD storage electrode length Y longer than length X to suppress fixed pattern noises caused by transfer inefficiency in this section, resulting in narrower barrier electrode length Z than storage electrode length Y. In conventional structure, electrons can't be transferred completely at HCCD frequency of 118MHz with drive voltage of 3V because longer storage electrode causes poor transfer efficiency due to low fringing fields.

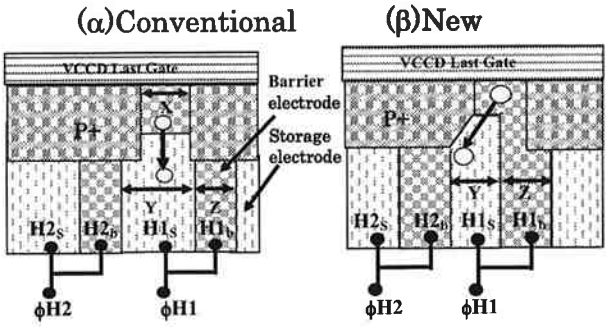
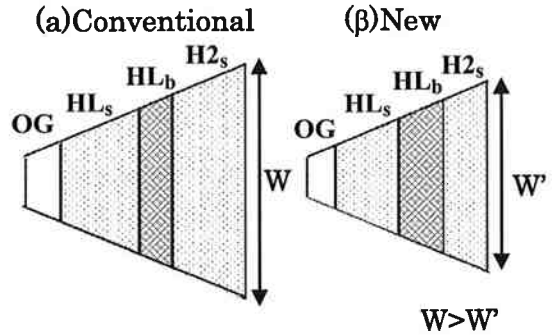
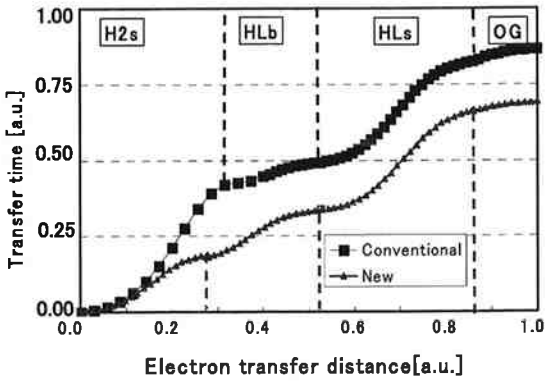


Figure 1: A structure of a connecting section from VCCD to HCCD.



(a)



(b)

Figure 2(a). A structure of the last stage of HCCD, Figure 2(b). Simulation result of electron transfer time.

In new structure, we design the channel stop layout with beveled edge at the connecting section from VCCD to HCCD. As a result, it is easy to make the storage electrode length Y nearly equal to the barrier electrode length Z without suffering from poor transfer efficiency at the connecting section from VCCD to HCCD. This geometry of storage and barrier electrodes enables sufficient fringing field for high speed HCCD transfer at HCCD drive frequency of 118MHz with drive voltage of 3V.

Figure 2(a) shows a structure of the last stage of HCCD. In new structure, we improve HCCD overflow drain performance to absorb the excessive charges over charge handling capability of HCCD, and than HCCD gate width W is able to be narrowed in order to decrease electrode capacitance. As a result, driving pulse waveforms and transfer time are improved.

By removing the excessive charges in HCCD, we design that $H2_s$ width is narrower than conventional structure as shown in figure 2(a). Figure 2(b) shows simulation result of electron transfer time at the last stage of HCCD consisting of gates; $H2_s$, HL_b, HL_s and OG. Because transfer time between $H2_s$ and HL_b is much improved and fringing fields are well balanced, total transfer time at the last stage of HCCD becomes shorter than conventional one.

As a result, sufficient transfer efficiency is obtained even at HCCD drive frequency of 118MHz with drive voltage of 3V.

3. Wide bandwidth of FDA of 300MHz

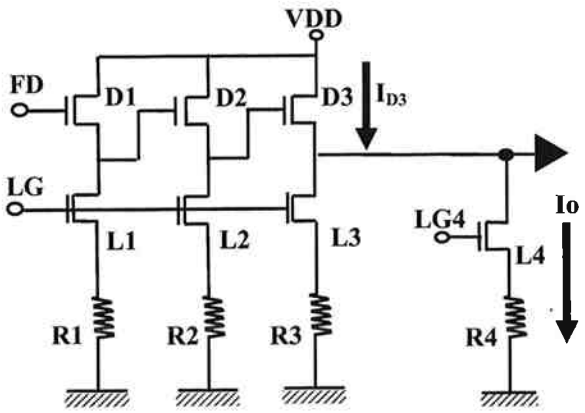


Figure 3. New source follower circuit.

Figure 3 shows newly developed source follower circuit. This circuit consists of three stages of source follower circuits, and the third stage source follower circuit has load elements of L3 and L4 in parallel.

Targets of bandwidth for 1-60fps and 96fps are 200MHz and 300MHz, respectively.

Two important points of new source follower circuit are discussed as following.

1. By improving transistor size of this circuit, the second and the third source follower circuit input capacitances are reduced, and

bandwidth of the first and the second source follower circuits become wider. In addition, by increasing the transconductance gm3 of D3, wider total bandwidth is obtained.

2. By switching the bias current Io of L4, frame rate is changed from 1-60fps to 96fps. L4 is cut off and drive current I_{D3} of D3 decreases at 1-60fps. L4 is switched on and I_{D3} increases to obtain lower output impedance at 96fps.

Figure 4(a) shows simulation result of bandwidth and gain versus LG voltage in conventional circuit. Gain G_3 of the third stage source follower is described as following;

$$G_3 = \frac{gm3}{gm3 + gmb3 + gds\_D3 + gds\_L3 + gds\_L4} \quad (1)$$

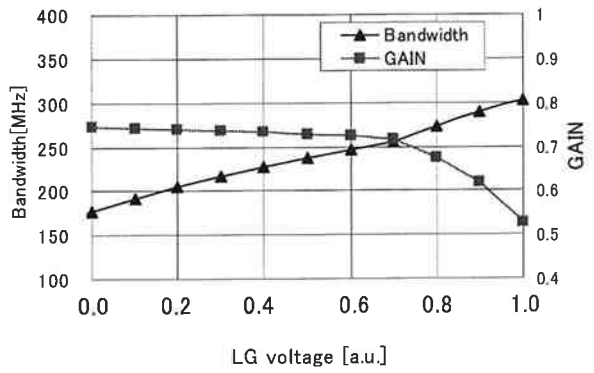
where gmb3 is back gate conductance of D3, gds_D3 is drain source conductance of D3, gds_L3 and gds_L4 are drain source conductance of L3 and L4, respectively. The parameters of gmb3, gds_D3, gds_L3 and gds_L4 need to reduce to increase the gain G_3. Bandwidth (BW) of the third source follower is described as following;

$$BW \cong \frac{gm3}{2\pi \cdot Co}, \quad (2)$$

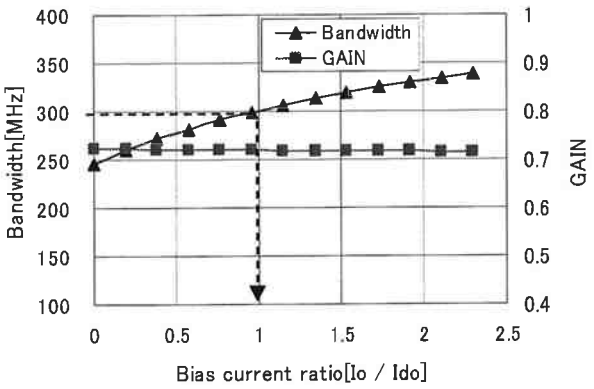
where Co is output load capacitance.

In conventional circuit, while the bandwidth is improved by increased LG voltage, the gain degradation is occurred because gds_L3 goes up and operating point of L3 moves from saturation region to linear region. From this point of view, it is impossible to obtain wider bandwidth without gain degradation by increasing LG voltage in conventional circuit. Right side of the turning point of gain curve in figure 4(a) shows that operating point of L3 moves from saturation region to linier region.

Figure 4(b) shows simulation result of



(a)



(b)

Figure 4(a). Simulation result of bandwidth and gain versus LG voltage. Figure 4(b). Simulation result of bandwidth and gain versus bias ratio of Io / Ido.

bandwidth and gain versus bias ratio of Io / Ido in new circuit, where Ido is bias current of D3 at Io=0mA. When L4 is cut off, R1, R2, R3, R4 and LG are designed to achieve the bandwidth 250MHz. When L4 is switched on, wide bandwidth is obtained by increasing Io. Furthermore, Gain is maintained because LG voltage doesn't increase and operating point of L3 doesn't move and gds_L4 is very small. For both bandwidth 200MHz and 300MHz, operating points of this circuit can be always kept suitable by setting R3 and R4 to be optimum value. On the other hand, experimental results of bandwidth show 200MHz and 270MHz for 1 – 60fps and 96fps in figure 5, respectively. Bandwidth for 96fps is little bit lower than an

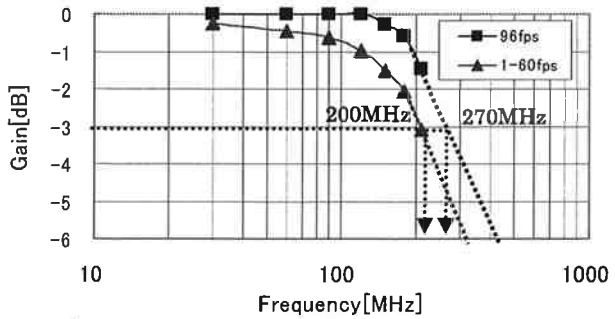


Figure 5. Experimental result of bandwidth.

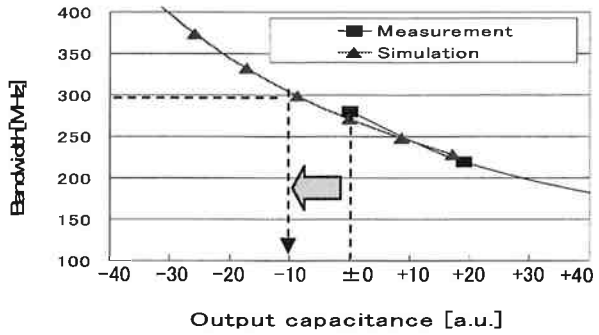


Figure 6. Measured and simulated bandwidth as function of load capacitance.

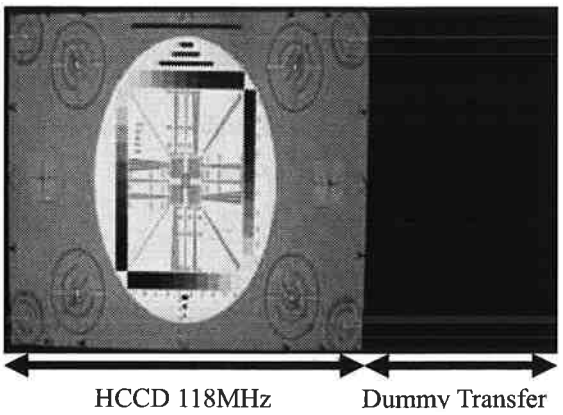


Figure 7. A reproduced image of a resolution chart at HCCD drive frequency of 118MHz.

expectation by a circuit simulation shown in figure 4(b). We estimate that load capacitance in an evaluation circuit is lager than that of simulation condition. Figure 6 shows measured and simulated bandwidth as a function of load capacitance. By reducing 10% of load capacitance from the present condition, we can achieve 300MHz bandwidth. Figure 7 shows a reproduced image of a resolution chart at HCCD drive frequency of 118MHz. The device has excellent characteristics such as high sensitivity, low smear and large saturation signal as shown in table 1.

4. Conclusion

In this paper, we described key technologies in order to realize high speed HCCD drive frequency of 118MHz and wide bandwidth of 300MHz. These technologies enable a 720p HDTV 2/3-type 1-mega pixel progressive scan CCD featured by a variable frame rate ranging from 1 to 96fps. The device shows high performance suited for broadcasting and cinema use.

5. Acknowledgement

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6. References

[1]S.Suzuki et al, "A 2/3-in. 2200k-pixel FIT-CCD for DTV 1080i", IEEE Workshop on CCDs and Advanced Image Sensors, Nagano, Japan (1999)

[2] R.Asada et al, "Development of Variable Frame Rate Camera recorder "Varicam" for Digital Cinema.," ITE Technical Report, vol.26, No.78, IPU2002-108

Table 1 . Specifications and characteristics.

Pixel	1-mega pixel (1280H×720V)
Cell size	7.5μm×7.5μm
Frame rate	1-96fps
Horizontal drive frequency	74.25MHz @ 1-60fps 118MHz @ 96fps
Horizontal CCD drive voltage	3V
Sensitivity (96fps, face plate illumination : 3lx)	185(mV)
Saturation signal	1160(mV)
Smear	-120(dB)