

## 12-Bit Column-Parallel ADC with Accelerated Ramp

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**Abstract:** Ramp analog-to-digital converters (ADC) have been widely used for column-parallel ADCs in imagers for several reasons: simple implementation, low power consumption, and guarantee of high linearity and monotonicity [1,2,3,4]. One drawback to using a ramp ADC is its slow operation speed when bit resolution is increased. In this paper we propose an accelerated ramp scheme based on photon shot noise limited characteristics of an image signal. Influence of the accelerated ramp-to-image quality was investigated by simulation, which confirmed its effectiveness. The scheme was successfully demonstrated by fabricating a prototype imager with 12-bit column-parallel ADCs.

### I. Introduction

In principle, a ramp ADC needs a conversion time of  $N_{RAMP} = 2^N - 1$  clock cycles, where  $N$  is the bit resolution of the ADC. To complete a 12-bit data conversion, 4,095 steps are necessary. In column-parallel ADC architecture, shown in Figure 1, an AD conversion sequence is completed during row operation time. Thus, the row operation time must be longer than 4,095 clock cycles if a comparator operation is synchronized with the clock. For an imager with 1,080 rows and a ramp clock of 25 MHz, for example, the frame rate is limited to 5.6 frames per second (fps) and is not sufficient for video applications. In order to support 1,080 rows and 30 fps, ADC conversion speed must be less than  $30\mu\text{s}$  and the number of ramp cycles must be less than 750 (with a ramp clock frequency of 25 MHz).

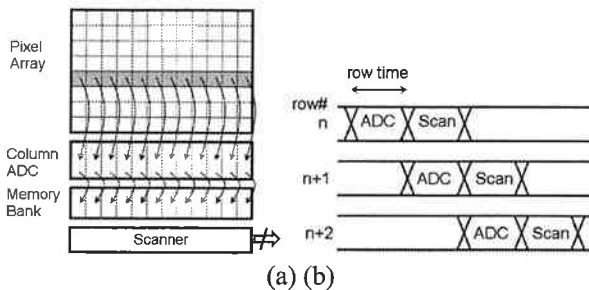


Figure 1 Architecture of a column ADC imager; (a) block diagram, (b) operation sequence

Recent trends in consumer imagers require smaller pixel sizes. This reduces the maximum output signal in terms of electrons. Reduction in pixel size affects the signal-to-noise ratio due to quantum fluctuation of signal electrons. The quantum fluctuation follows Poisson statistics, and this noise is termed shot noise. Figure 2 shows the relationship between pixel size and signal electrons in a typical condition. With a pixel pitch of  $3.0\mu\text{m}$  and camera sensitivity set at 500 lux with an F2.8 lens, the saturation signal is approximately 10,000 electrons ( $e^-$ ) at  $1/30$  sec exposure time.

When an averaged number of signal electrons is  $\overline{N_{sig}}$ , the temporal signal is affected by the shot noise fluctuation with a deviation of  $\sqrt{\overline{N_{sig}}}$ , and the S/N ratio becomes  $\overline{N_{sig}} / \sqrt{\overline{N_{sig}}} = \sqrt{\overline{N_{sig}}}$ . In the case of  $N_{sig} = 10ke^-$ , the maximum S/N ratio is limited at  $100 = 40\text{dB}$ . The contribution from shot noise increases with decreasing pixel size.

Given this background, we investigated a way to reduce the number of ramp steps based on the nature of photon shot noise limitation.

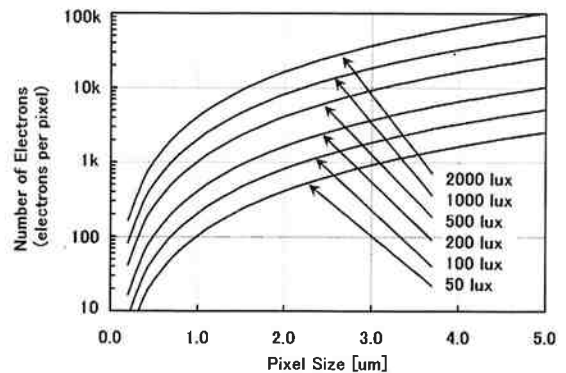


Figure 2 Signal electrons versus camera sensitivity, F=2.8, 5000k light + IR-cut,  $1/30$  sec, effective pixel QE=0.25.

### II. Accelerated Ramp Modulation

The shot noise fluctuation is converted into a digital value of least significant bits (LSB) using the following relation:

$$D_{shot}(N_{sig}) = \text{int}[2^N \times \sqrt{\overline{N_{sig}}} / N_{sat} + 0.5] \text{ LSB}, \quad (1)$$

where  $N_{sat}$  is the number of saturation electrons and corresponds to an ADC input window.  $D_{shot}$  values are plotted in Figure 3(a) versus signal electrons  $N_{sig}$ , assuming  $N = 12$  bits, and  $N_{sat} = 20ke^-$ . The  $D_{shot}$  value near the saturation is 14 LSB.

Since digital data resolution below  $D_{shot}$  is covered by the shot noise, we considered that the ramp step width could be increased in the large signal regions, where there is increased  $D_{shot}$ . However, if the ramp step width is close to or larger than  $D_{shot}$ , the quantization noise and/or contour-wise artifacts affect image quality. Therefore, we introduced a parameter called shot noise margin:  $M_{shot} = W_{shot}(N_{sig})/D_{shot}(N_{sig})$ . This constraint is followed such that the increased ramp step width  $W_{ramp}(N_{sig})$  should not exceed  $M_{shot} \times D_{shot}(N_{sig})$ , as shown in Figure 3(b). Where  $M_{shot} = -6\text{dB}$  ( $= 1/2$ ), the ramp step width is less than half of the shot noise deviation at all signal levels. In other words, the shot noise spreads at least twice the ramp step width, which effectively reduces the possible appearance of contours.

Actual ramp patterns with 12 bits,  $N_{sat} = 20\text{ke}^-$  and  $M_{shot}$  values of 0dB, -6dB and -12dB, are shown in Figure 4, and required ramp steps are summarized in Table I. The ramp pattern shows a square-like curve. When  $M_{shot} = -6\text{dB}$ , the number of ramp steps for the 12-bit AD conversion is 607. Compared to the linear ramp, the step number is reduced to  $606/4,095$  or  $\sim 1/6.7$ . Even with  $M_{shot} = -12\text{dB}$ , i.e., a step width smaller than one quarter of the shot noise, the step number can still be saved to 1,240, which is close to the 10-bit linear ramp of 1,023.

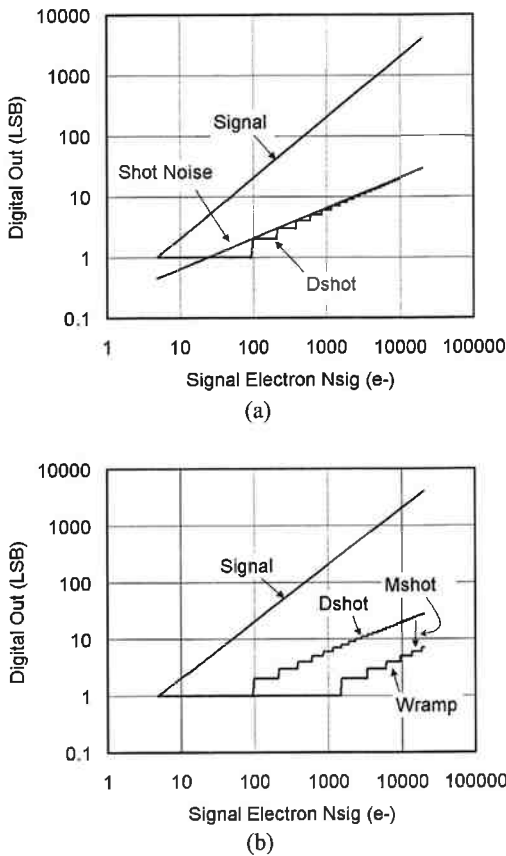


Figure 3 Saturation electrons of  $20\text{ke}^-$  and 12-bit AD conversion; (a) Signal, shot noise and  $D_{shot}$ , (b) Ramp step width  $W_{ramp}$  with a margin  $M_{shot} = -12\text{dB}$

Mode	Linear	0dB	-6dB	-12dB
Ramp Steps	4095	298	607	1240

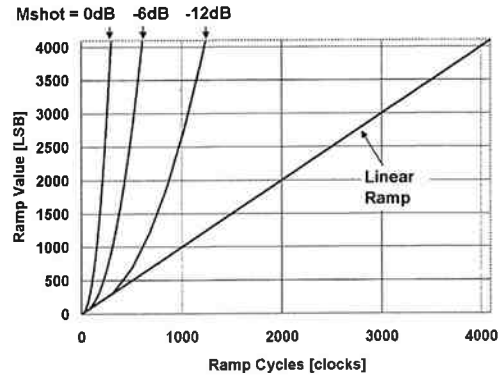


Figure 4 Ramp pattern in accelerated ramp at  $20\text{ke}^-$  saturation and 12-bit AD conversion

### III. Image Simulation on Noise Margin, $M_{shot}$

The visual simulation was performed to investigate image quality versus the noise margin,  $M_{shot}$ . A reference image was obtained in the following manner: first a raw image was captured by a high-end camera, then image size reduction to VGA size was performed with pixel binning, which reduces shot noise in the sample image. The original sample image is shown in Figure 5(a). Next, artificial shot noise was added assuming saturation electrons of  $5\text{ke}^-$ . The image was then equivalent to one captured by an imager that has  $5\text{ke}^-$  full-well capacity or by a camera with adjusted sensitivity to  $5\text{ke}^-$  saturation per pixel. The image was used as an initial image in the following simulations. Twelve-bit digital-to-digital conversion was applied to the initial image, each corresponding to the ramp pattern with a noise margin of -12dB, -6dB, 0dB, +6dB, +12dB, and +18dB. White balance was performed before the conversion.

A possible problem caused by the accelerated ramp scheme is noise increase at portions that have middle/high signal levels, because the ramp compression is only applied for the levels as illustrated in Figure 4. In order to compare the noise between images, a  $70 \times 50$  pixel region of an image (a picture of part of a human face) is magnified and arranged in Figure 5 (a)–(h): (a) sample image, (b) simulation initial image with  $5\text{ke}^-$  saturation, (c)  $M_{shot} = -12\text{dB}$ , (d)  $M_{shot} = -6\text{dB}$ , (e)  $M_{shot} = 0\text{dB}$ , (f)  $M_{shot} = 6\text{dB}$ , (g)  $M_{shot} = 12\text{dB}$  and (h)  $M_{shot} = 18\text{dB}$ . All images are reproduced without gamma compression.

In comparison between Figures 5(a) and 5(b), image degradation by the shot noise can be seen. However, the shot noise is inherent in small pixel imagers and/or high sensitivity imaging as described in the Introduction. Therefore, actual influence from the accelerated ramp modulation in Figure 5(c)–5(h) is evaluated by comparison with the simulation initial image in Figure 5(b).

Comparison between the images shows that no image degradation is visible when  $M_{shot}$  is equal to or below 0dB. Increasing  $M_{shot}$  to 6dB or greater yields extra random-wise noise. Contour-wise artifacts become visible when ramp step width becomes extremely large, such as the case of  $M_{shot} = 12\text{dB}$  or  $18\text{dB}$ .

$M_{shot}$  dependence of image degradation compared to the original image is summarized in Figure 6. The results show that the image is not affected by the accelerated ramp modulation when  $M_{shot}$  is equal to or less than 0dB.

From these results, we can conclude that the accelerated ramp modulation will not degrade image quality when the ramp step width is smaller than the shot noise. However, from an image sensor production point of view, introducing the noise margin  $M_{shot}$  is preferred in terms of immunity to variations.

#### IV. Prototype Imager

We fabricated a prototype imager that employs 12-bit column-parallel ADCs with an on-chip functional ramp generator to demonstrate the accelerated ramp scheme. A simplified architectural view of the prototype imager is shown in Figure 7. The pixel array consists of an active area of  $2352\text{H} \times 1728\text{V}$  pixels with the addition of peripheral rows/columns used for optical black pixels. The pixel size is  $2.9\mu\text{m}$ . A column cell comprises sample and hold memory, a variable gain column amplifier, 12-bit ramp ADC, and DRAM memory for a readout buffer. One amplifier and ADC is shared by two columns, thus two AD conversion operations are performed for one row cycle.

While an ADC code is applied from a digital timing controller to the ramp ADCs, a ramp generator provides an analog ramp voltage corresponding to the temporal digital ADC code. Several variations of ramp modes, 12-bit linear mode, 10-bit linear mode, 12-bit  $M_{shot} = -6\text{dB}$  mode, and  $M_{shot} = 0\text{dB}$  mode, are programmed in the timing controller and the ramp generator. The accelerated ramp pattern is designed to fit a maximum full-well capacity of  $20\text{ke}^-$ .

Imager performance was measured with a 24 MHz ramp clock. Photoconversion characteristics of the imager operated in a 12-bit linear ramp mode and a 12-bit accelerated ramp mode with  $M_{shot} = 0\text{dB}$  are plotted in Figure 8 with temporal noise and column FPN values. Temporal noise includes both electrical noise and shot noise. Except for a small non-linearity around 2,048 LSB, seen in the Figure 8(b), along with the accelerated ramp, this doesn't affect photo response and noise performance. The kink near the 1/2 MSB is due to ramp generator non-linearity and not an inherent issue in terms of the accelerated ramp scheme.

#### V. Conclusion

We have proposed an accelerated ramp scheme for column-parallel ramp ADCs. The compressed ramp pattern for acceleration is determined based on signal-to-noise limitations from shot noise, and was shown to allow large reduction for the number of ramp cycles without degradation of image quality. These results show that the use of column-parallel ramp ADCs for high-resolution video imaging is an attractive solution.

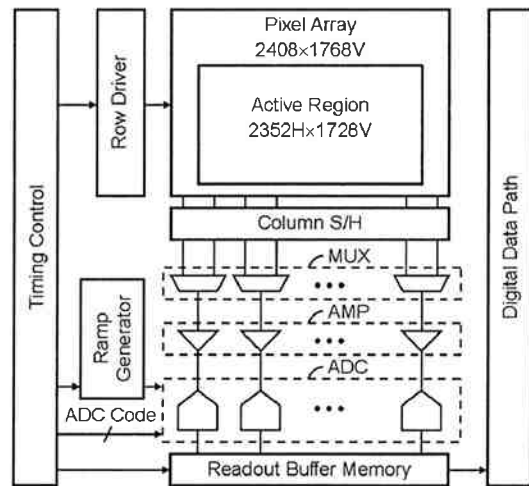


Figure 7 Block diagram of a prototype imager

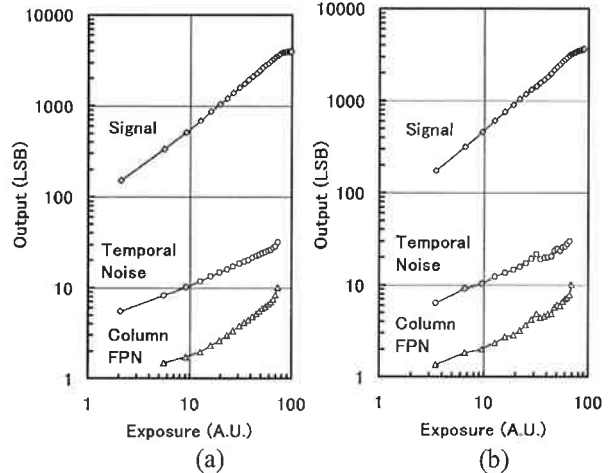


Figure 8 Photoconversion characteristics; (a) 12-bit linear ramp mode, (b) 12-bit accelerated ramp mode with  $M_{shot} = 0\text{dB}$

#### References

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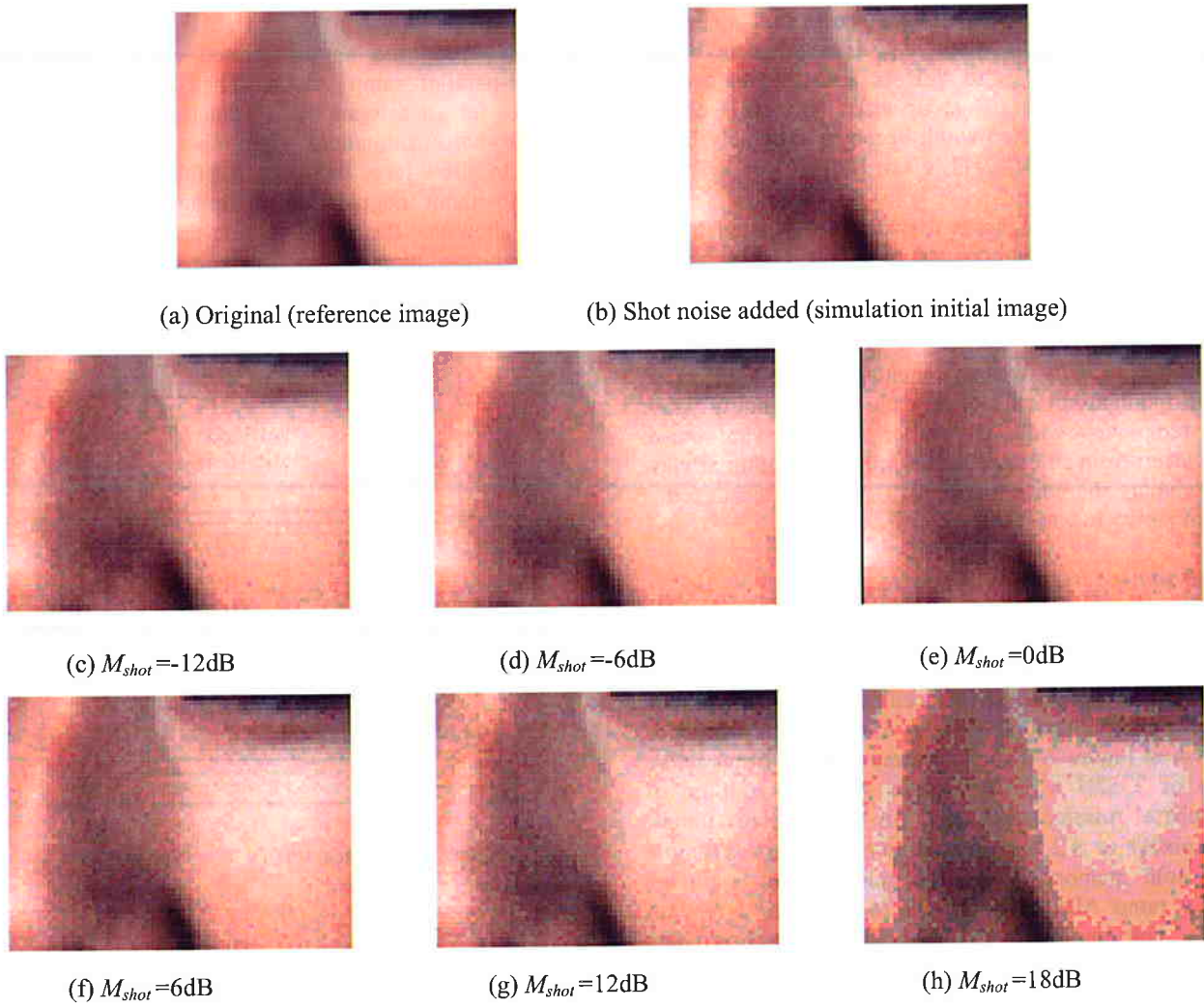


Fig.5 Magnified view of a 70 pixel (H) x 50 pixel (V) region of image simulation result varying shot noise margin (FullWell=5ke- fixed)

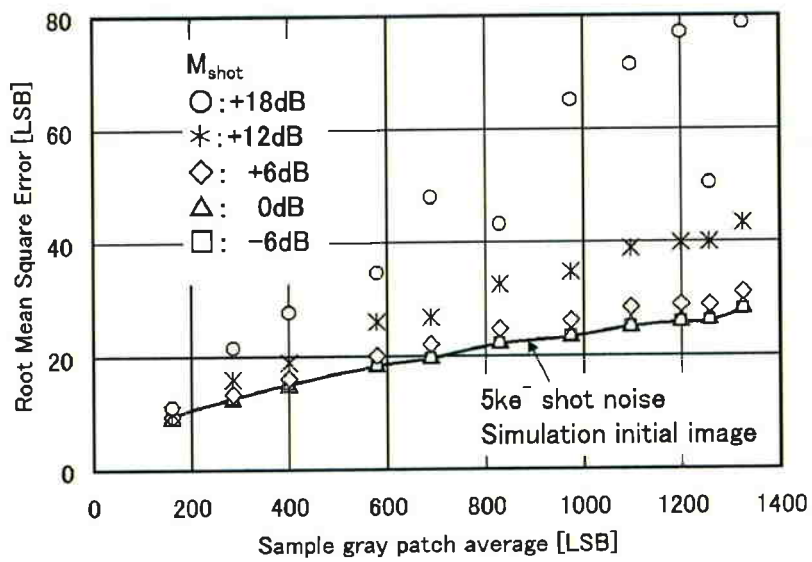


Figure 6 Originality degradation dependency with signal levels