A CMOS image sensor for ID detection with high-speed readout of multiple region-of-interests

Koji Yamamoto[a], Yuki Maeda[b], Yasuo Masaki[c], Keiichiro Kagawa[a], Masahiro Nunoshita[a] and Jun Ohta[a]

Affiliations: [a]Graduate School of Materials Science, Nara Institute of Science and Technology (NAIST), 8916-5 Takayama, Ikoma, Nara 630-0101 JAPAN

Tel: +81-743-72-6054, Fax: +81-743-72-6052, E-mail: ya-kouzi@ms.naist.jp

[b]Innovation Plaza Osaka, Japan Science and Technology Agency (JST); [c]FUNAI ELECTRIC CO., LTD.

Abstract

We propose a CMOS image sensor that can capture both normal images and multiple region-of-interests (ROIs) images at a high-speed frame rate for our newly developed man-machine interface system called "Opto-Navi". In this system, optical beacons equipped with network appliances inform their positions at slow frequency around 10 Hz, which define ROIs, and send their ID at several 100 bps to the sensor. The sensor can recognize the position of ID with frame differences of normal images and simultaneously obtain the ID by readout only ROIs at a high-speed frame rate. A QVGA image sensor is fabricated in 0.35-μm CMOS process. This sensor can capture ROIs images @ 1.1 kfps/ID for ID detection with capturing normal images @ 30 fps.

1. Introduction

Recently, home-network for electronic appliances is growing interest; many network appliances will be connected each other over home-network. We have proposed the "Opto-Navi" system for a man-machine interface to control network appliances visually [1]. In this system, a mobile phone with the custom image sensor is used as an interface; many of mobile phones are equipped a large display, a digital camera, IrDA, Bluetooth, etc. In the "Opto-Navi" system, home network appliances such as DVD recorder, TV, PC, etc., are attached with LEDs that transmit ID signals at ~500 Hz. The image sensor can receive IDs with high-speed readout of multiple region-of-interests (ROIs). The received IDs are displayed with a superimposed background image captured by the sensor as shown in Fig.1. With the "Opto-Navi" system, we can control such appliances with visually confirming them on a mobile phone display.

2. Image Sensor for the "Opto-Navi" system

The image sensor for ID detection has already proposed [2] [3]. However, they have issues of large power consumption or large pixel size in the cause of high-speed readout of all pixels or ID receiver circuits in each pixel for receiving ID. Here we have proposed an image sensor dedicated for the "Opto-Navi" system to realize high-speed readout at low power consumption with a simple pixel circuit. In our readout scheme, the sensor is operated for capturing normal images at a conventional video frame rate with simultaneously capturing multiple ROIs which receiving ID signals at a high-speed frame rate. To find out ROIs with the sensor, we introduce a pilot signal which blinks at a slow rate of ~10 Hz so that the sensor can easily recognize it with a fame difference method.

The proposed readout scheme is shown in Fig.2. The feature is based on a multiple interleaved readout of ROIs; each ROI is readout in multiple times during one frame of normal images so that ROIs can be readout much faster than the frame rate of normal images. To explain the readout scheme simply, only 6×6 pixels are depicted in the Fig.2, where two IDs exist and thus two ROIs are shown. In Fig.2, the number in each pixel indicates the readout order and the number in parentheses means that the pixel involves with ID signals. In this case, 3 ROIs images/ROI are read during one frame rate of whole images. Actually, frame rate of ROIs images is 1.1 kfps in our sensors case; number of pixels: 320×240 [pixel], ROIs size; 5×5 [pixel], number of IDs: 7, frame rate of whole images: 30 [fps]. This readout scheme has a feature that a system clock speed is same as one for a conventional image sensor operating at 60 fps, and thus it essentially consumes very little power even reading ROIs with a high-speed frame rate. The power consumption can be further suppressed without supplying power to the column involving ROIs.

Fig.3 shows a block diagram of the sensor. The sensor is operated with ID Map Table, which is a 1-bit memory array memorized IDs position for reading out only ROIs at high-speed and cutting off power supply to pixels outside ROIs. The pixel circuit is simple; it has only one additional transistor for column reset compared with a conventional 3-Tr APS. This transistor is used for XY-address reset to read out pixels only in ROIs. Timing chart for the sensor is shown in Fig.4. In this timing chart, fragmented normal images and ROIs images are interleaved readout.

3. Experiments

We fabricated a QVGA image sensor with 0.35-μm CMOS process. Fig.5 shows a microphotograph of the sensor. Specifications are summarized in Table1. Fig.6 shows a captured normal image at 30 fps and Fig.7 (a) and (b) show experimental results for ID detection. ID signals are transmitted differential 8-bit code modulated at 500 Hz from 3 LED modules. 36-frame ROIs images per ID, which consists of 5×5 pixels, are captured for detecting ID signals while one frame of a whole image is captured as shown in Fig.6 (b). The patterns of ROIs images successfully demonstrate the detection of each ID. These results demonstrate the image sensor can capture QVGA images @ 30 fps with capturing images of 3 IDs @ 1.1 kfps/ID. The power consumption of the sensor is 3.6 mW @ 3.3 V.

4. Conclusions

The "Opto-Navi" system is proposed as a new man-machine interface. In this system, network appliances are controlled by a mobile phone equipped the custom image sensor for ID detection. Architecture of the image sensor with high-speed readout of multiple ROIs to simplify the pixel circuit and suppress power consumption of the sensor is proposed for the "Opto-Navi" system. We have fabricated the image sensor with 0.35-μm CMOS process and have demonstrated ID detection @ 1.1 kfps/ID with capturing scene @ 30 fps. The power consumption of the sensor is 3.6 mW @ 3.3 V.

Acknowledgement

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References

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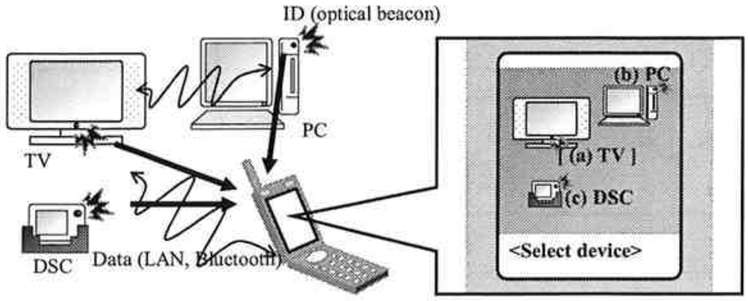


Fig.1 "Opto-Navi" System

1	2	3	6	7	8
11	12 ROI#1	13	16	17	18
21	(4),(24) 22, (44)	(5),(25) 23, (45)	26	27 ROI#2	28
31	(9),(29) 32,(49)	(10),(30) 33, (50)	36	(14),(34) 37, (54)	(15),(35) 38, (55)
41	42	43	46	(19),(39) 47, (59)	(20),(40) 48, (60)
51	52	53	56	57	58

Fig.2 Timing for high-speed readout of multiple region-of-interests

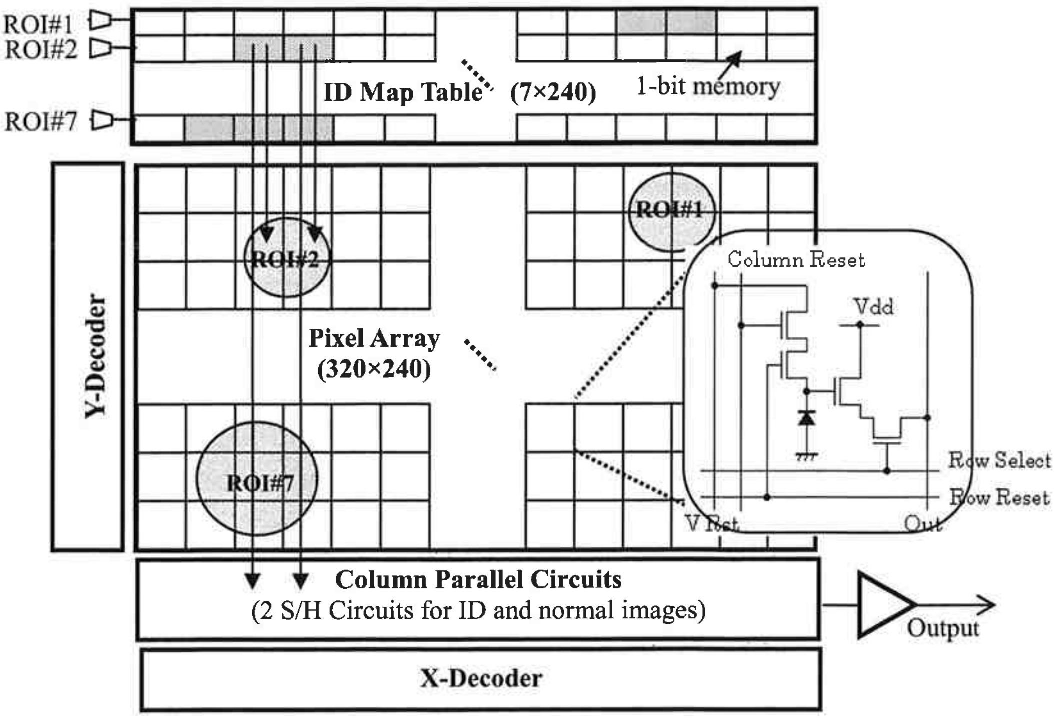


Fig.3 Block diagram of the image sensor

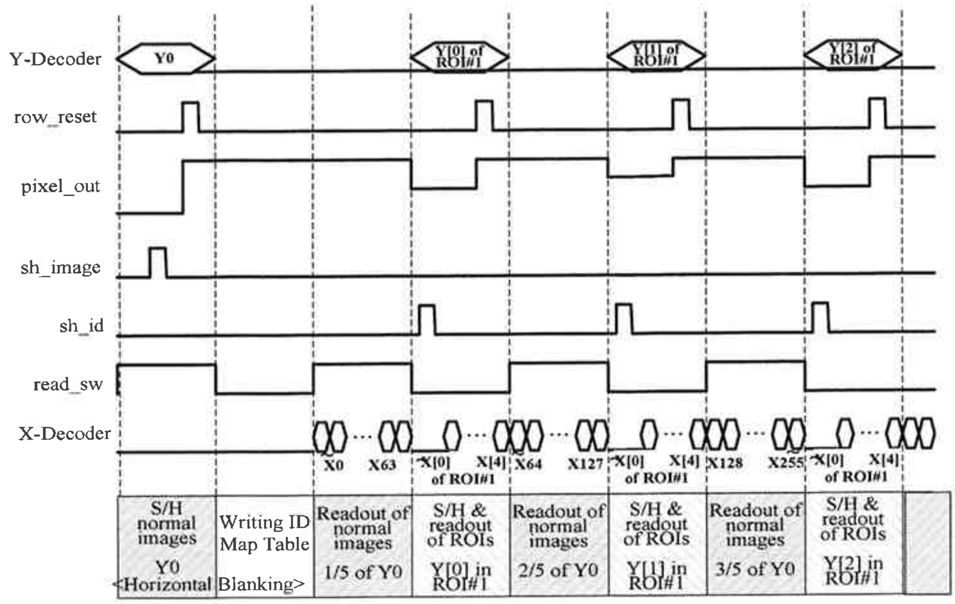


Fig.4 Timing chart of the image sensor

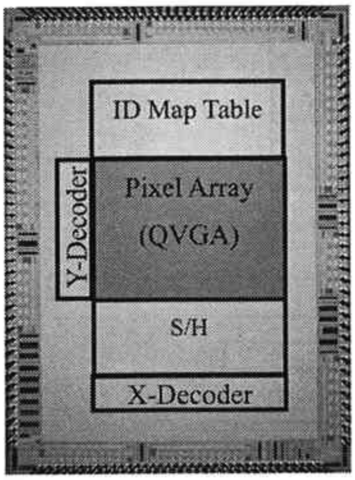
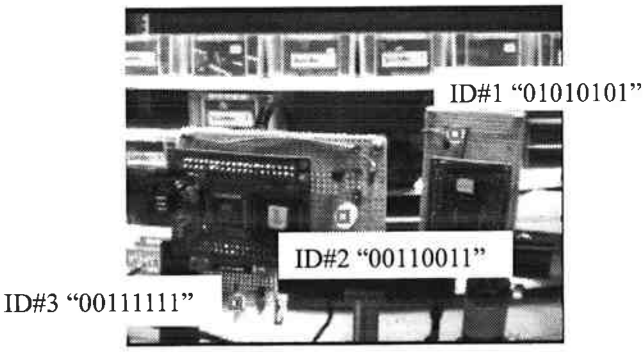


Fig.5 Microphotograph of the sensor

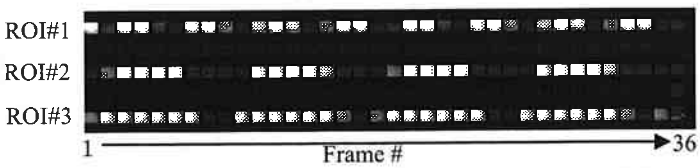
Table1 Specifications of the image sensor

Technology	0.35-μm CMOS (2Poly 3Metal)
Number of pixels	QVGA (320×240)
Chip size	4.2×5.9 mm^2
Pixel size	7.5×7.5 μm^2
Dynamic range	54 dB
Frame rate of normal images	30 fps
Number of IDs (max)	7
Frame rate of ID images	1.1 kfps/ ID
Power Consumption	3.6 mW @ 3.3 V

Fig.6 Captured image



(a) Normal image



(b) 36-frame ROIs images / ID (in 1 frame for normal image)

Fig.7 ID detection