Ultra High Light Shutter Rejection Ratio Snapshot Pixel Image Sensor ASIC for Pattern Recognition

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I. Introduction

The ultra high light shutter rejection ratio snapshot pixel image sensor ASIC is designed for detecting moving objects without motion artifacts. This chip can be integrated into the fast moving pattern recognition system, such as machine vision and robot control system. One of main challenges for snapshot CMOS sensor is the light leakage to the storage node [1], [2]. This paper presents a solution on minimizing the light leakage that provides snapshot images without motion artifacts.

II. Image Sensor and System Overview

The pattern recognition system includes the CMOS image sensor ASIC, Control host, Illumination System, and Event Detection Unit. Figure 1 shows the block diagram of the pattern recognition system.

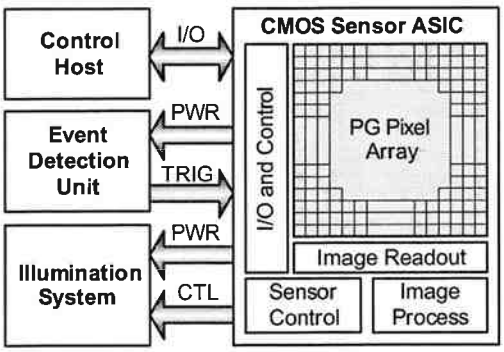


Figure 1 *Block diagram of the pattern recognition system.*

The CMOS image ASIC with single power supply contains a low resolution snapshot pixel image sensor array and on-chip image processing. The CMOS ASIC also contains I/O control (interfacing with Control Host), sensor control, illumination control (high voltage power supply to the light source from charge pump and switching control for turn ON/OFF the illumination), phase lock loop (PLL), power management (provides analog and digital power), power on reset (POR), band-gap reference, and event triggering analog input. The block diagram of the CMOS ASIC chip is shown in figure 2.

III. Image Sensor Design

The CMOS ASIC has image sensor pixel array with 100×100 active pixels for pattern recognition, and few rows of dark pixels for auto offset correction. The illumination source of the system is controlled by the ASIC with on chip charge pump as power supply. To suppress motion artifact and minimize the system power consumption, the illumination turned ON during the very short integration time. However, in the particular application for which this ASIC is intended, the background illumination is expected to vary several orders of magnitude. Thus, snapshot operation of image sensor with minimum light and substrate charge leakage is required.

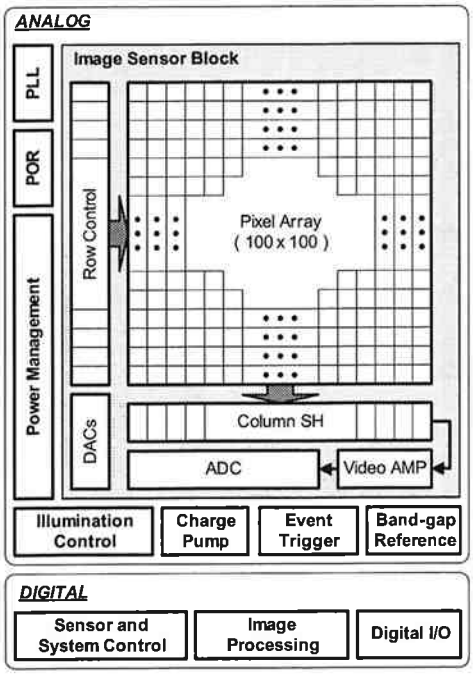


Figure 2 *Block diagram of the CMOS ASIC chip.*

Imager pixel array utilizes 5T photogate pixel architecture with 20-μm×20-μm pitch for adequate MTF and QE in near IR illumination. In addition to near IR image quality requirement, the most critical performance parameter was the shutter rejection ratio (SRR). The ratio of readout time compared to the shortest integration time requirement of 20 μsec presented a challenge to achieve 50,000× (94 dB) SRR under bright ambient illumination during readout. A typical 5T photogate pixel CMOS sensor with snapshot operation can not achieve such a high SRR due to light leakage and substrate charge leakage to the pixel charge storage node during the readout time. Light leakage is due to the stray light finding its way to the storage node if the storage node is not fully covered by metal shield. The light leakage can be minimized by careful metal shield design to cover the silicided storage node. Substrate charge leakage is caused by the photoelectrons generated in the substrate beneath

the photon sensing area drifting to the storage node. A deep n-well charge isolation layer connected to the guard ring is placed under the storage node to prevent the charge leaking to the storage node. Figure 3 gives the schematic cross section of the ultra high light shutter rejection ratio snapshot photogate pixel.

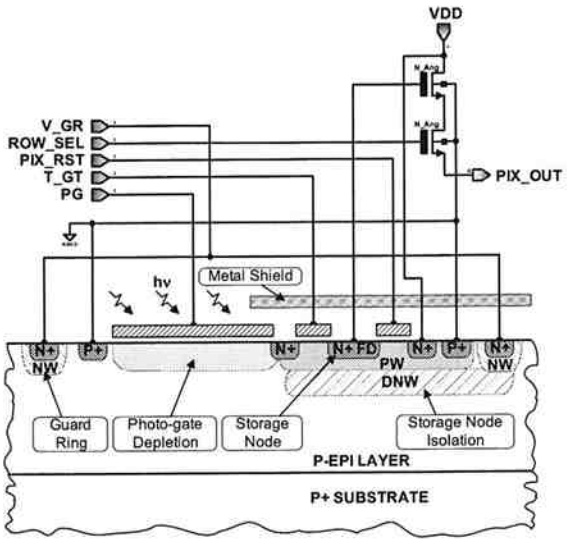


Figure 3 *Schematic cross section of pixel.*

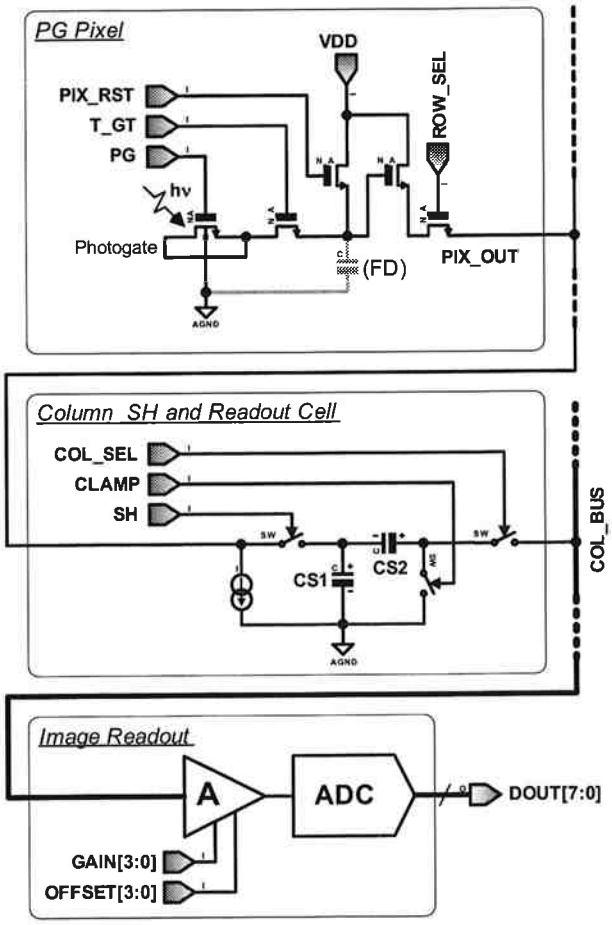


Figure 4 *schematic block diagram of the image sensor signal chain.*

The imager runs up to 100 frames/sec with pixel output rate of 1.5 MPixels/sec. The pixel output is sampled differentially to the passive column sample/hold and readout block with very low column fixed pattern noise. Image readout block contains the output amplifier (video AMP) with CTIA (capacitive transimpedance amplifier) configuration and analog-to-digital converter (ADC). Video AMP applies gain (getting code from auto-exposure control) and offset correction (getting code from auto dark offset correction) to the signal. Low power 8-bit ADC (nominal 0.9 mA current consumption) converts the signal to digital data.

Figure 4 shows the schematic block diagram of the image sensor signal chain. Table 1 gives the key design specifications of the image sensor ASIC.

Table 1 *Key design specifications of the image sensor ASIC.*

Parameters	Value	Remark
Pixel Size	20-μm×20-μm	
Pixel Array	100×100	
Pixel Type	Photogate	Snapshot with ultra high SRR
Pixel Out Rate	1.5 MPixels/sec	
Frame Rate	100 Frames/sec	Max. frame rate
Image Output	8-bit	
Integration Time	20 μsec 200 μsec	Minimum Typical
Power Supply	3.3 V ± 10%	
Gain Settings	0.5× to 8×	16 linearity steps
QE×FF	15 %	@ 850 nm
Image Lag	< 1.0 %	
SRR	> 94 dB	
MTF	80 % @ 10 lpmm 60 % @ 20 lpmm	
Current Consumption	< 10 mA @ active mode < 40 μA @ sleep mode	Does not include the IR Charge Pump current

IV. Experimental Results

The image sensor ASIC has been fabricated in standard 4-metal 1-poly MIM cap 0.25-μm CMOS process. Figure 5 shows the photograph of the packaged chip.

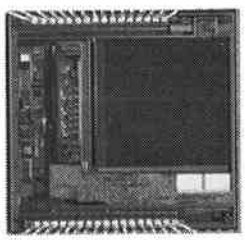


Figure 5 *Picture of the image sensor ASIC.*

Lab evaluations of the chip, including linearity, signal-to-noise ratio, dark current, full well capacity, and power consumption, have been completed. Extensively pixel characterizations have also been performed. They are quantum efficiency (QE), modulation transfer function (MTF), Image lag, and shutter rejection ratio (SRR).

- *Quantum Efficiency*

The measured quantum efficiency without the fill factor adjustment is given in Figure 6, below. Note that, QE at the near IR illumination of interest is defined by the epi thickness available in standard 0.25 μm process. The pixel size is chosen to provide adequate signal as required for this particular application. Since photo-gate type pixel design is utilized, peak QE is about 37% around 650 nm. In this application, it was also desirable to reduce the visible light sensitivity of the pixel which was partially achieved by photo-gate.

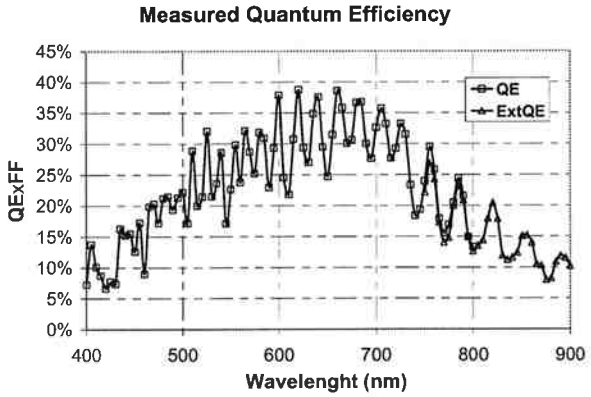


Figure 6 *Measured chip QE×FF.*

- *Modulation Transfer Function*

MTF is a very important parameter for pattern recognition. To enhance the MTF of the chip, n-well guard-ring is implemented in the pixel. The guard ring is reducing the cross-talk between adjacent pixels. Figure 7 shows the measured MTF of the chip at 850 nm illumination.

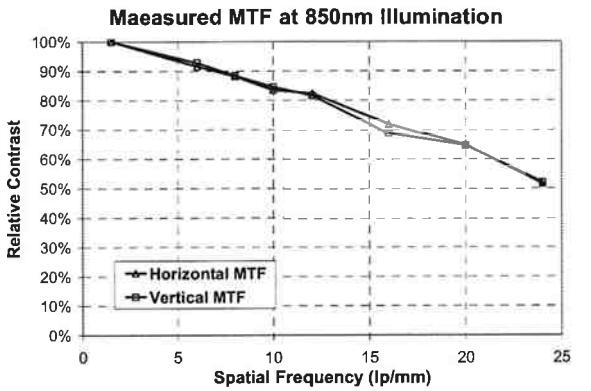


Figure 7 *Measured MTF of the chip.*

- *Image Lag*

For photogate type pixels, image lag is caused by incomplete charge transfer from photogate to sense node. When a pixel is exposed to a transition between high to low light levels, the residual charge under photogate gives the *ghost* imaging for the consecutive frames. Thus, low image lag is desired. Measurement of the image lag is described below:

(a) Five consecutive image frames were acquired with first frame illuminated by LED and four consecutive frames in the dark, as shown in figure 8. Illumination level of the first frame is about 220 DN (for 8-bit ADC output) at low gain setting which is close to saturation.

Figure 8 *Images taken for image lag measurement.*

(b) Assume the fifth frame of image has no residual charge left under photogate, the mean of the fifth frame only represent the dark current and image offset. The image lag can be calculated by:

$$IMG\_LAG = \frac{Mean_{SECOND\_FRAME} - Mean_{FIFTH\_FRAME}}{Mean_{FIRST\_FRAME} - Mean_{FIFTH\_FRAME}}$$

The measured image lag is about 0.18%.

- *Shutter Rejection Ratio*

In the image operation, integration time is much shorter than the readout. High shutter rejection ration (SRR) is required for getting pictures without motion artifacts. SRR definition and measurement are given below:

(a) Set illumination level near saturation close to full ADC output range at minimum integration time (i.e., T_{INT} = 20 μsec). Illuminate the image during the integration time only, calculate the image output mean $Mean_{ILLUM}$.

(b) Keep the same illumination level. Illuminate the image during readout operation (i.e., readout time of each row T_{ROW_READ} = 80 μsec). Calculate the slope of image output as function of row number. The slope ($Leak_{ROW}$) represents the leakage to the sense node during one row readout time.

(c) Sutter rejection ratio is given by:

$$SRR = 20 \cdot \log_{10}\left[\frac{(Mean_{ILLUM} / Leak_{ROW})}{(T_{INT} / T_{ROW\_READ})}\right] \quad (dB)$$

Table 2 gives the measured image SRR at different illumination level. We should emphasize the difficulty in measuring the SRR when the light leakage has been successfully eliminated, as has been the case in this

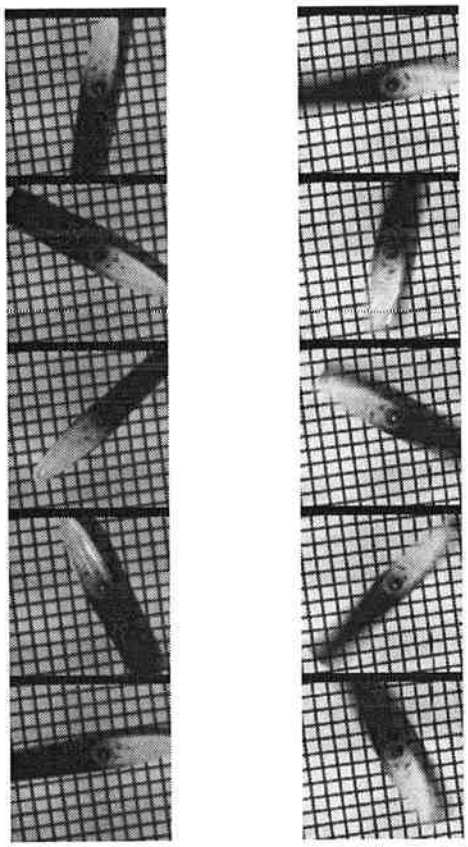
imager. The low illumination level corresponds to 100× the saturation signal at 20 μsec integration time. Even at this level of illumination during readout, the slope for the entire frame is less than 0.3 LSB; which is at the limit of theoretical ADC digitization noise. The other two numbers correspond to 200× and 400× saturation level at 20 μsec integration time.

Table 2 *SRR at different illumination level.*

Illumination Level (Image Output)	Measured SRR
236 (DN)	96.8 dB
114 (DN)	97.0 dB
52 (DN)	96.5 dB

- ***Snap Shot Images***

Figure 9(a) and 9(b) show the five consecutive images of rotating fan taken by the sensor at 200 μsec and 2.0 msec, respectively. The fan is running at approximately 22.5 r.p.s. The image is operating at 75 frames/sec. At 200 μsec integration time, the clear image of the rotating fan as well as the background grid pattern demonstrates the low image lag with the snap-shot operation. In comparison the image sequence taken with 2.0 msec integration shows a blurry picture of the fan.



(a) (b)

Figure 9 *Images of rotating fan taken by the sensor with 200 μsec (a) and 2.0 msec (b) integration time.*

- ***Image Sensor Performance***

Measured performance of the ultra high light shutter rejection ratio snapshot pixel image sensor is given by table 3.

Table 3 *Measured image sensor performance.*

Parameters	Value	Remark
Max. SNR	49.1 dB	
Full Well	26.8 ke^-	
Dynamic Range	47.6 dB	
Dark Current	1.05 mA/cm^2	
Response none uniformity	< ± 2DN	At Gain = 1×
QE×FF	37 % 15 %	@ 650 nm @ 850 nm
Image Lag	< 0.2 %	
MTF	85 % 65 %	@ 10 lpmm @ 20 lpmm
SRR	> 96 dB	
Chip Size	3.65×3.55 (mm^2)	

V. Conclusions

An ultra high light shutter rejection ratio snapshot pixel image sensor is designed with novel storage node structure in order to reduce the charge leakage to the sense node. Experimental results show that > 96 dB SRR and very low image lag has been achieved. The image sensor meets the requirements for pattern recognition on fast moving objects.

VI. Acknowledgement

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References

[1] G. Yang, O. Yadid-Pecht, C. Wrigley and B. Pain, *Snap-Shot CMOS Active Pixel Imager for Low Noise, High Speed Imaging*, pp. 2.7.1-2.7.4, IEDM Digest, Dec 1998.

[2] S. Seshadri, G. Yang, M. Ortiz, C. Wrigley, and B. Pain, *CMOS Difference Imagers with Charge-Leakage Compensation and Sum Output*, pp. 125 128, 2001 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Lake Tahoe, Nevada, USA, June 7-9, 2001.