# Characterization and improvement of random noise in 1/3.2" UXGA CMOS image sensor with 2.8um pixel using 0.13um-technology

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**Abstract**

**The noise sources of CMOS image sensor have been characterized through overall signal path from the photodiode to analog circuit with 1/3.2" UXGA, 2.8um pixel using 0.13um-process. As a result, it is found that the dominant source of dark random noise in CMOS image sensor is the flicker noise of source follower transistor. We have achieved the improvement of total random noise by reducing the flicker noise of the source follower transistor as a proof of this analysis.**

## I. Introduction

Recently, CMOS image sensors (CIS) have gained much more interests in digital camera application than charge coupled device (CCDs) for its low power consumption, low cost, and the level of integration with image signal processor on a single chip. However, CIS still suffer from higher noise than CCD due to the temporal noise and fixed pattern noise (FPN) from pixel as well as additional analog circuits. Fortunately, the FPN has been reduced to an acceptable range with the assist of the correlated double sampling (CDS) technology. However temporal noise, which sets limits on dynamic range and SNR in low illumination, have still deteriorated image quality compared to that of CCDs.

In this work, for the first time, we have characterized the dark random noise (DRN) of CIS and resolved out the amount of noise contribution of each source using specific test patterns. It is pointed out that the dominant source of random noise in CIS and the physical model is developed to explain two paths of flicker noise affecting the pixel output noise. Finally the improvement of dark random noise is shown by reducing the dominant noise source.

## II. Characterization of dark random noise

The standard 4-Tr active pixel sensor analyzed in this paper is described in Fig. 1. Each pixel is comprised of photodiode (PD), reset gate transistor (RG), transfer gate transistor (TG), source follower (SF), row selection transistor (SEL), and floating diffusion (FD). The pixel output node (Vout) is connected to the bias transistor and the analog circuits including CDS block, which is not shown in this figure.

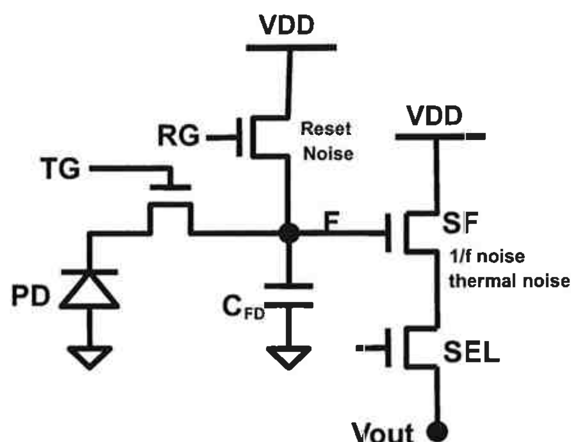


Fig. 1. 4-Tr active pixel sensor. Each pixel is comprised of a photodiode (PD), reset gate transistor (RG), transfer gate (TG), source follower (SF), row selection transistor (SEL), and floating diffusion capacitance ($C_{FD}$).

To characterize the feature of DRN of the total array, the standard deviations of the consecutive 20-frame outputs of each pixel is defined as DRN. The measured DRN histogram in Fig. 2 shows the asymmetric distribution around the peak value, having a long tail toward high value of random noise ($\sigma_{left}$ = 0.34, $\sigma_{right}$ = 2.51). The root-mean of the total array's DRN square is about 8.9, but the peak value of total array's DRN is about 7. The presence of this abnormally high DRN value degrades the overall noise characteristics of CIS.

To further investigate the characteristics of pixels with high random noise, the temporal behavior of random noise of each pixel is monitored from the captured three consecutive 20-frames (totally 60 frames).

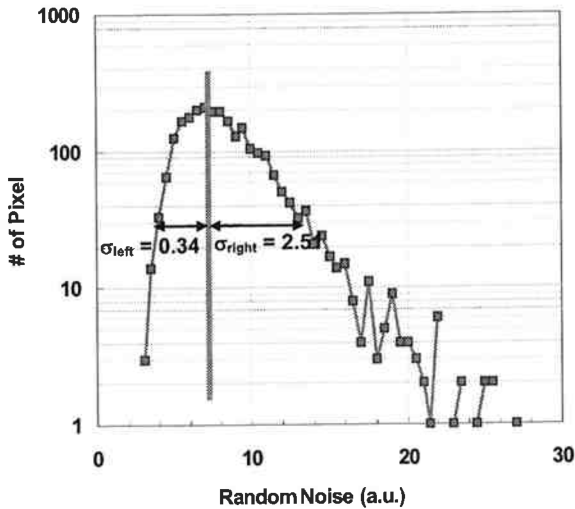


Fig. 2. Dark random noise histogram, where random noise of each pixel is obtained by calculating the standard deviation of 20-frame outputs of each pixel. It has been measured under dark condition. The abnormal, asymmetric distribution around peak value is observed.

The 1st, 2nd and 3rd 20 frames' DRN of the same pixel is calculated, as shown in Fig. 3 [1]. It is observed that each pixel has always the same value of random noise instead of arbitrary value, which means that there exist particular pixels having the high value of random noise at each measurement, corresponding to the long tail in DRN histogram (Fig. 2). It also indicates that the random noise is caused in the pixel, rather than in the analog circuit.

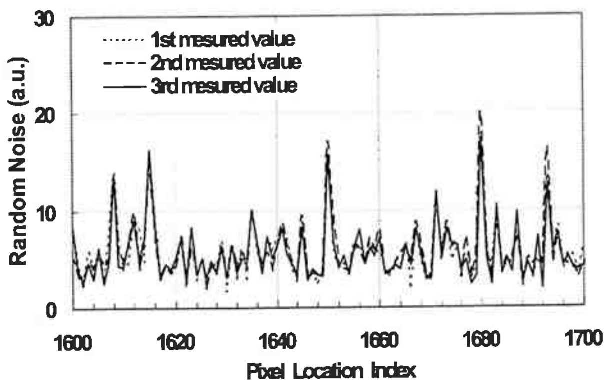


Fig. 3. Three consecutive captures of dark random noise with respect to each pixel location. Each pixel has always the same value of random noise instead of arbitrary value at each measurement, showing the random noise is due inherently to the individual pixel itself.

### III. Dominant source of the random noise.

In analyzing the noise source in the overall signal path from photodiode to analog domain, there might be a variety of noise sources, including dark current shot noise in photodiode, the reset noise of reset transistor, thermal and flicker noise of SF transistors, and analog circuit noise.

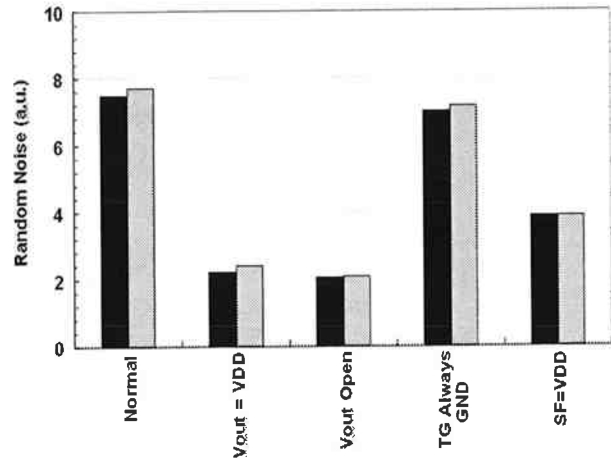


Fig. 4. Dark random noise measured from the various test patterns. It is found that the dominant source of the random noise is SF transistor.

The four specific test patterns have been used to clarify the amount of source of random noise. Two of them, where one is the case of the output node being connected to the analog power ('Vout=VDD') and the other being floated ('Vout=Open'), have negligible random noise compared with the normal pixel, which correspond to the amount of noise contribution of analog circuit. It also shows that the dominant source of random noise is in the APS block rather than in the analog block, which is the same result as that of the consecutive DRN capture analysis in Fig. 3. Another test pattern of the transfer gate always grounded ('TG always GND') has almost the same noise level as that of the normal pixel, resulting that the shot noise due to the dark level of photodiode contributes little to total random noise in the CIS. This is also confirmed from the results that there is little change of random noise in even varying the integration time of photodiode from 1-horizonatal time to 1-frame time. Moreover the reset noise can be neglected in the CIS with the help of CDS architecture.

The last test pattern of FD being tied to VDD has much larger DRN value than that of analog circuit but smaller than that of normal pixel, so that the most part of the noise is considered to come from FD and SF.

Although the junction leakage of FD can be a noise source, it has little effect on DRN, confirmed by additional tests of both varying FD integration and temperature. Increase of FD integration up to eight times makes little change in DRN. In addition, the increase of temperature from 20°C to 80°C makes no change in DRN, excluding the noise component of PD dark level by shortening the PD integration to 1-horizontal time, in spite of the increase of total DRN due to PD dark level. Therefore it is concluded that the SF noise is dominant in overall signal path in CIS. It is also notable that the increase of DRN from the case of 'SF = VDD' to the normal pixel case seems to be caused by the presence of FD capacitance at the input of SF transistor, which will be modeled in next section.

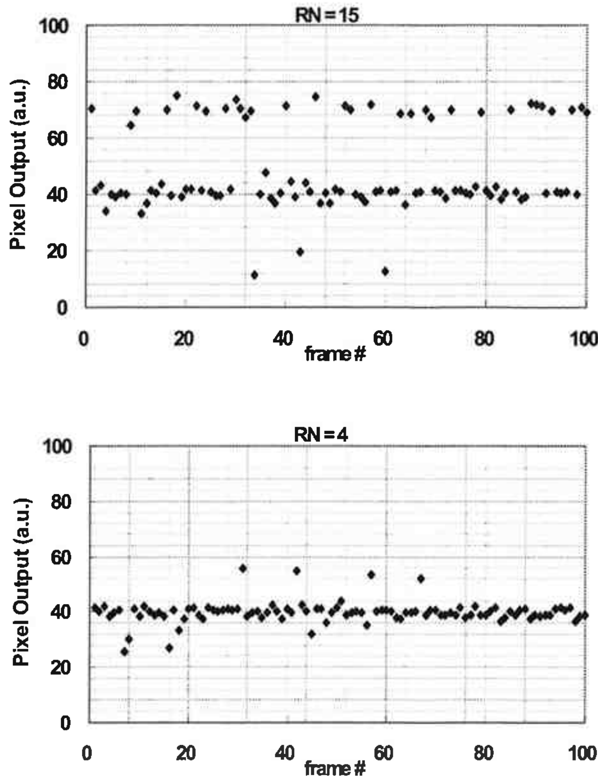


Fig. 5. Temporal output behavior of one pixel. The upper pixel has high random noise and the lower pixel has low random noise, respectively. It is shown that the output of pixel is switching between just two discrete levels.

There might be two noise sources in SF, one is flicker noise and the other is thermal noise [2,3]. In order to determine which of the two is dominant, the temporal output behavior of pixels with low and high random noise is measured, as shown in Fig. 5. It is notable that the pixel output levels with high random noise are quantized to just two discrete levels rather than arbitrary levels. This quantized temporal behavior is known as a typical feature of flicker noise [2], originating from the trapping and de-trapping process of charge at the interface between the gate oxide and the silicon channel of MOS transistor. The independency of DRN upon temperature as well as the above finding indicates that 1/f noise contributes dominantly to SF noise rather than thermal noise. At last it can be concluded that the dominant noise source of CIS is due to the flicker noise of SF in pixel.

## IV. Flicker noise model for pixel source follower

In the above analysis, it is revealed that the most part of the DRN comes from the source follower flicker noise. In addition, it should be noted that DRN is affected and seems to be amplified by FD capacitance. These results can be made apparent by considering the following simplified, physical model for the pixel SF with the gate being connected to FD capacitance, as shown in Fig. 6.

In the presence of the trapped charges ($\Delta Q_{trap}$) at the interface between the silicon channel and the gate oxide, the variation of trapped charges induces the corresponding fluctuation of channel potential ($\Delta V_{trap}$),

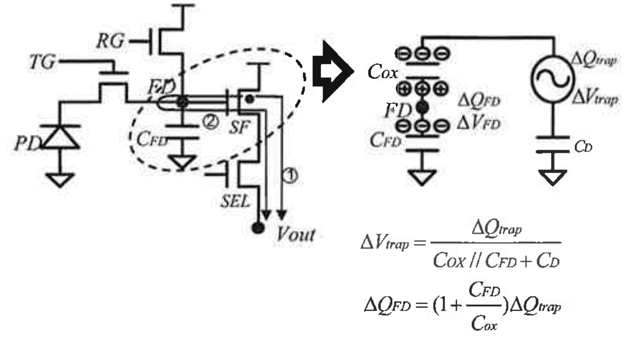


Fig. 6. SF trapping model with floating diffusion node, which explains the dependency of the SF flicker noise on conversion gain of FD.

which is the total output noise of pixel due to the flicker noise. This fluctuation of the output of SF, $\Delta V_{trap}$ is related to the trap charges $\Delta Q_{trap}$, as below.

$$\Delta V_{trap} = \frac{\Delta Q_{trap}}{C_D + C_{ox}C_{FD}/(C_{ox} + C_{FD})} \quad (1)$$

$$\cong (1 + \frac{C_{ox}}{C_{FD}})\frac{\Delta Q_{trap}}{C_{ox}}, \quad (C_D \cong 0) \quad (2)$$

As $C_{FD}$ becomes infinite, $\Delta V_{trap}$ converges to the constant value of $\Delta Q_{trap}/(C_{ox}+C_D)$ and thus becomes independent of $C_{FD}$, which is the case that the gate of SF is ac-grounded just as for 'SF=VDD' test pattern in Fig. 4. Such is not the case, however, when the gate of SF is connected to the finite capacitance of $C_{FD}$. As long as the finite $C_{FD}$ exists at the gate of SF, the output fluctuation $\Delta V_{trap}$ has the strong relation to $C_{FD}$. As $C_{FD}$ becomes even smaller than $C_{ox}$, $\Delta V_{trap}$ increases linearly with respect to $1/C_{FD}$.

To get a more physical perspective of the effect of the trap charges in gate oxide as well as FD capacitance on the noise performance, the input-referred noise charge $\Delta Q_{FD}$ can be calculated by normalizing $\Delta V_{trap}$ with $A_v \cdot G_{conv}$, where the SF gain and the conversion gain of FD node are denoted by $A_v = C_{ox}/(C_D + C_{ox})$ and $G_{conv} = q/\{C_{FD} + (1 - A_v)C_{ox}\}$, respectively.

$$\Delta Q_{FD} = \Delta V_{trap}/(A_v \cdot G_{conv}) = (C_{FD}/C_{ox} + 1)\Delta Q_{trap}, \quad (3)$$

There are two terms affected by the trap charge $\Delta Q_{trap}$. One component of the input-referred noise charges is $(C_{FD}/C_{ox})\Delta Q_{trap}$, which is equivalent to $\Delta Q_{trap}/(C_{ox}+C_D)$ at the pixel output, corresponding to the case of the input of SF being ac-grounded. Hence this component is what is seen to output through the direct path from SF channel variance due to trap to pixel output variance (path ① in Fig. 6). The other component $\Delta Q_{trap}$ in the input-referred noise charges corresponds equivalently to $A_v \times G_{conv} \times \Delta Q_{trap}$ at pixel output. It is interpreted by this 2nd component that $\Delta Q_{trap}$ induces the corresponding change of the number of the charge in FD ($\Delta Q_{FD}$) through the gate oxide capacitor and then be amplified by the amount of the total gain of $G_{conv} \times A_v$ (path ② in Fig. 6). Hence it is concluded that the total output noise due to the flicker noise of gate oxide trap is the

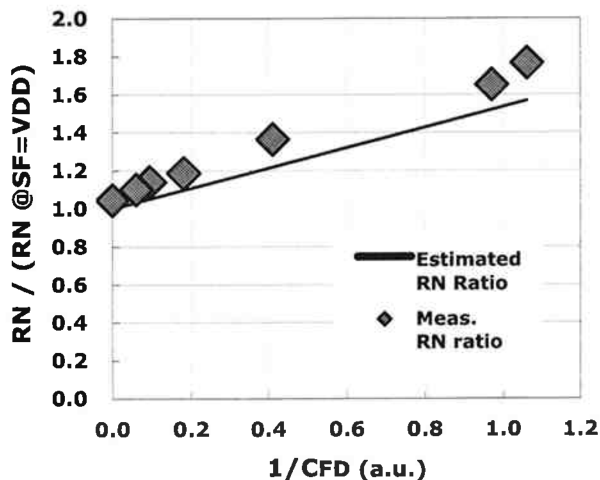


Fig. 7. The dependency of dark random noise upon the floating diffusion capacitance.

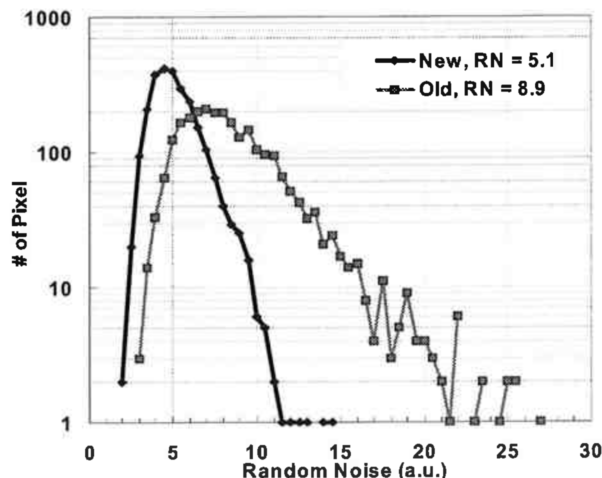


Fig. 9. Improvement of random noise by reducing the trap effect on SF transistor. The abnormal asymmetric behavior has been greatly disappeared.

superposition of the direct effect as well as the gain effect by conversion gain.

To confirm the flicker noise model of pixel source follower, DRN is measured from the test patterns with various FD capacitances. By normalizing the output noise with regard to the infinite FD capacitance (the ac-grounded input of SF), the experimental results in Fig. 7 show that the output noise increases linearly according to $1/C_{FD}$ with an offset of $\Delta Q_{trap}/(C_{ox}+C_D)$, in a good agreement with the flicker noise model of pixel SF described previously in Fig. 6.

For the analysis of the signal to noise ratio, with all the noise sources put into FD node, it would be favorable to increase the conversion gain as large as possible if direct path noise were dominant. However, as the conversion gain becomes large enough, the gain effect of flicker noise by conversion gain is more dominant than that of direct path. Hence it is more efficient to reduce noise source itself, $\Delta Q_{trap}$ rather than to increase conversion gain. Fig. 9 shows the improved DRN histogram of 1/3.2" UXGA CIS with 2.8um pixel by 0.13um-technology, by reducing gate oxide trap effect itself, proving the validity of the above analysis associated with noise sources in CIS.

### V. Conclusion

The dark random noise of CMOS image sensor has been characterized so that the flicker noise due to gate oxide trap of source follower transistor causes the abnormal, asymmetrical histogram and two discrete, quantized output behaviors in time domain, as the main source of dark random noise in the overall signal path from pixel to analog circuit. In addition, it is physically modeled and verified that dark random noise due to the gate oxide trap is the superposition of two output noises by not only the direct effect from source follower channel to output but also the amplification effect by conversion gain of floating diffusion. Finally the improvement of dark random noise by more than 40% is achieved by the reduction of the gate oxide trap effects, verifying the above analysis.

*[References]*

[1] J.R. Janesick et. al., "Charge coupled device charge collection efficiency and the photon transfer technique", Optical Engineering, vol. 26, no. 10, pp. 972-980, Oct. 1987.

[2] K.K. Hung et. al., "Random Telegraph Noise of Deep-Submicrometer MOSFET's", IEEE Electron Device Letters, v. 11, no. 2, pp. 90-92, Feb. 1990.

[3] Willy M.C. Sansen and Zhong Yuan Chang, "Limits of Low noise performance of Detector Readout Front Ends in CMOS Technology", IEEE trans. on Circuit and Systems, vol. 37, no. 11, pp. 1375-1382, Nov. 1990.

[4] K.K. Hung et. al., "A unified model for the flicker noise in MOS semiconductor field effect transistors", IEEE trans. on Electron Devices, vol. 37, no. 3, pp. 654-665, Mar. 1990.