Excess Noise and Dark Current Mechanisms in CMOS Imagers

Bedabrata Pain, Thomas Cunningham, Bruce Hancock, Chris Wrigley, and Chao Sun
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
Phone: 818-354-8765; Fax: 818-393-0045; Email: bpain@jpl.nasa.gov

The average noise and dark current of CMOS imaging technology has vastly improved within the last decade [1,2]. However, the presence of "hot" pixels continues to be a source of major annoyance. "Hot" pixel refers to those imager pixels that have dark current or noise much above the mean value. The continuing trend of using newer (and more scaled) technology nodes for implementation of CMOS imagers is presenting fresh challenges to the dark current and noise reduction. In this paper, we present some results of our investigation to identify the behavior and sources of the "hot" pixels.

Figure 1 shows the schematic cross-section of two photodiode-type pixels. On the top is the n-well pixel consisting of a diode formed between n-well and p-epitaxial silicon, with the n-well connected to the source of the reset FET by a n^+ source-drain (S/D) implant. At the bottom, an additional p^+ implant added to the surface to form a buried diode (p-cover pixel).

Maximum dark current is generated when a depletion region encounters either a large number of traps (usually interface traps or metallic impurities near the surface) or a large electric field or both. The leakage-prone regions within the pixel are identified by oval-shaped markers in figure 1 [3]. For the n-well pixel (top), the most vulnerable regions are located at the n-well to p-well junction under the STI oxide, n^+ implant to p-well junction along the STI edge, and the edge between the source and gate of the reset FET. For the buried diode pixel, an additional region of vulnerability is the surface-p^+ to n-well junction along the STI edge.

Figure 2 shows the spatial distribution of dark current for two imagers of 512^2 and 256^2 format, implemented in a 0.25 μm CMOS technology. The schematic cross-sections of the imager pixels are shown in figure 1. It can be seen that at 300K, the modal dark current of p-cover pixel (109 pA/cm^2) is ~ 3 times less than that of the n-well pixel (293 pA/cm^2). Although the junction area is nearly the same for both pixel types, a large part of the junction periphery does not terminate at the STI for the p-cover pixel, resulting in a reduction of the modal dark current. However, the shape of the spatial distribution is nearly the same for both types of pixels – both exhibit distinct exponential tails that continue till ~1.5 nA/cm^2.

In order to determine the dark current generation mechanisms for the "hot" pixels, we extracted their dark I-V characteristics as follows. First, an accurate conversion gain ($c_g(V)$), including its voltage dependence, was carried out on a pixel-by-pixel basis [4], and then the slope of dark current (dV/dt) was measured as a function of the output video level (V). From these, the dark current was calculated as:

$$I_d(V) = \frac{1}{c_g(V)} \cdot \frac{dV}{dt}.$$

It was found that most of the hot pixels shows a marked voltage (and hence electric field) dependence. The electric field at the diode area is controlled both by the diode reverse-bias voltage and the gate voltage. Figure 3 (left) shows the circuit schematic of the pixel, showing the diode connected to the reset FET and the source follower FET. The reset FET is selected by a horizontal bus that swings between V_H and V_L – the reset ON and reset OFF levels respectively.

When the reset FET is turned off, the reverse electric field between its source (connected to the photodiode) and gate is very high, causing significant field-assisted leakage in the diode [5]. This can be clearly seen from figure 3 (right) where the accumulated dark signal is plotted against the integration time for different values of V_L. At low V_L (large back-bias), the dark signal is high and extremely non-linear, becoming lower and more linear as V_L is increased. The gate-induced-leakage (GIL) is clearly discernible from the resultant I-V curve, as shown in figure 4. Since the output (V) is measured differentially, a zero voltage corresponds to a reset level (which was set to 2.3V). Figure 4 shows that the dark current was extremely high a low voltages (corresponding to high reverse field), and become lower at higher voltages where the electric field is greatly reduced. The measured dark current data was modeled as follows [6]:

$$I_d = I_{fixed} + \alpha \cdot \exp\left[\frac{V_{rst} - V - V_G}{V_x}\right]^2$$

where I_{fixed} is the fixed current, α is the proportionality constant, V_{rst} is the reset voltage on the diode, V_G is

the reset gate voltage, and V_x is the field-threshold voltage. Figure 4 (right) shows that the model matches the family of curves quite well, indicating that the dark current mechanism is the trap-assisted-tunneling [7] that is dependent on the gate-to-source electric field, rather than the band-to-band tunneling that is often considered to be the main mechanisms behind GIDL [8].

Not all "hot" pixels, however, showed the same voltage dependence. For instance, some of the pixels showed an exponential voltage dependence (trap-assisted-tunneling), but were practically independent of the reset FET gate bias, as shown in figure 5 (left). Others "hot" pixels behaved in a more normal fashion (SRH generation), exhibiting lesser voltage dependence. The fact that the "hot" pixels behave differently from the normal pixels is further ascertained from the Arrhenius plot shown in figure 6. It shows that dark current for both a normal and a "hot" pixel follow the Arrhenius relation, but with different activation energies. While the activation energy for normal pixels is ~ 0.6 eV, that of the "hot" pixels is only ~ 0.35 eV, further pointing to an increased electric field dependence. It can be concluded that most of the "hot" pixels exhibit some form of increased voltage dependence, pointing to the need for reducing internal electric fields.

Figure 7 shows the measured spatial distribution of read noise as a function of temperature. Noise was measured using an off-chip 4-point correlated double sampling (CDS) method with the minimum integration time. It can be seen that at all temperatures, the spatial distribution consists of a gaussian distribution followed by an exponential tail. The modal dark current reduces slightly with temperature, going from ~ 8 e^- at 300K to ~ 6 e^- at 140K. However, the noise tail shows no discernible change, although the dark current was negligible at low temperatures, indicating that the noise in the "hot" pixels is non-thermal in nature.

Figure 8 shows the measured noise at 220K as a function of integration time for two different imagers implemented in 0.25 μm technology. Measurements were carried out at 220K to eliminate dark current shot noise contribution. For the first imager, a pixel belonging to the gaussian part of the distribution exhibited no 1/f noise as shown in figure 8A, while one taken from the exponential tail did exhibit a large amount of 1/f noise. The imager was then operated in the flushed reset mode [9], that allows cycling of the source-follower FET into accumulation prior to readout and reset - a technique that has been reported to reduce flicker noise [10]. However, as shown in figure 8A (data points marked by *flicker_mod*), no significant flicker noise reduction was achieved for this imager. In contrast, significant 1/f noise reduction was achieved in another imager with the flushed reset, as shown in figure 8B.

Figure 8C shows the read noise measurement for two different values of pixel source-follower current but a fixed pixel sampling time. It can be seen that as the source-follower bias current is reduced, the read noise reduces by more than a factor of 2. Furthermore, there is no dependence of the noise on the exposure time. Since the source-follower voltage and current bias strongly influences hot electron generation [11,12], the data in figure 8C is strongly indicative of hot-electrons being responsible for generating read noise in these pixels. Since a pixel is selected (causing the source-follower to draw current) only for a tiny fraction of the integration time, hot-electrons are not significant dark current contributors. Nevertheless, they play a major role in generating the pixel excess noise.

While more work is needed to better quantify the relative contributions of each effect, it is clear that a reduction in the pixel electric field can play a big role in reducing the noise and dark current spread.

Acknowledgments:

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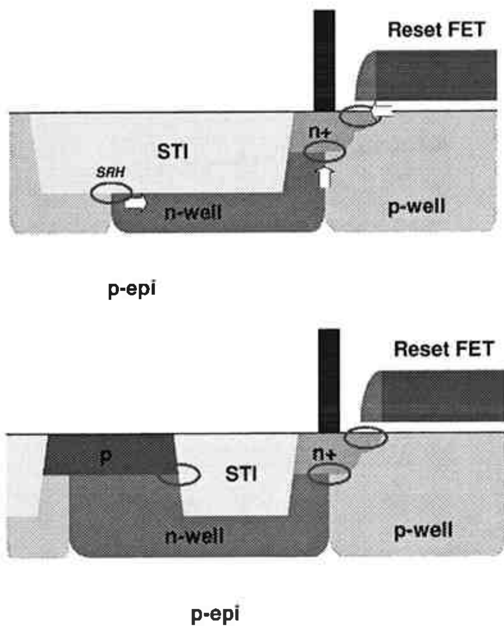


Figure 1: Schematic cross-section of the pixel diode and reset FET: n-well pixel (top) and p-cover pixel (bottom)

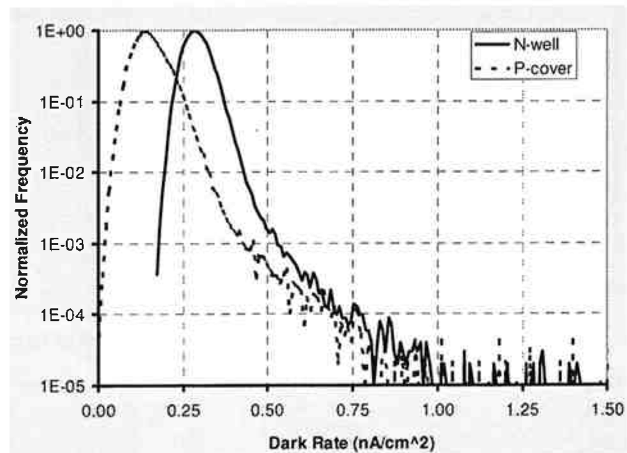
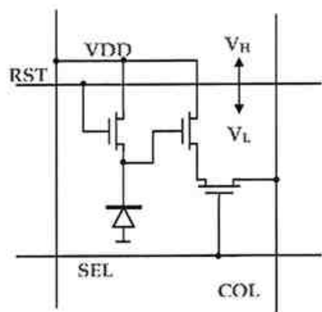


Figure 2: Histogram of spatial distribution dark current for two types of pixels



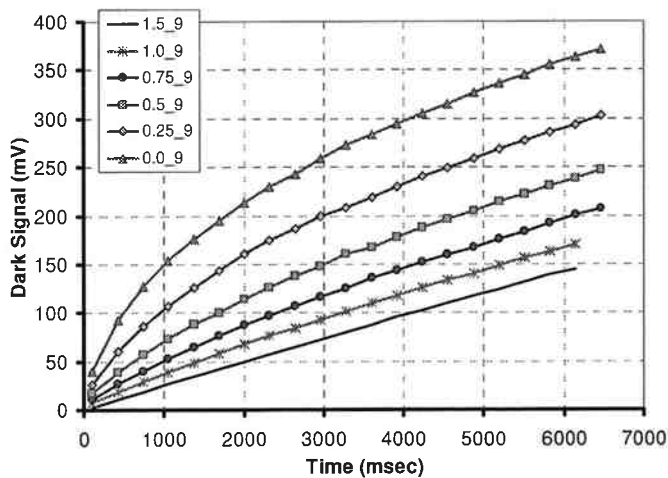
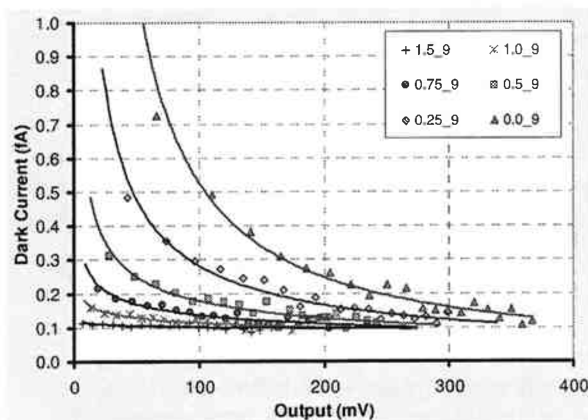


Figure 3: Pixel schematic (left) and the evidence of Gate induced source leakage (right)



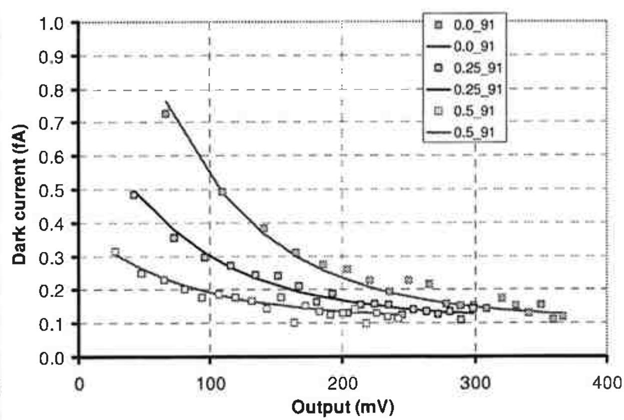
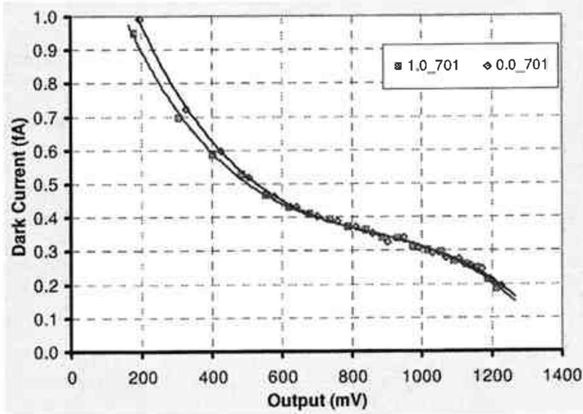


Figure 4: Gate-induced-Source-Leakage (GISL) – leakage current as a function of accumulated voltage (measured data on the left, and modeled on the right)



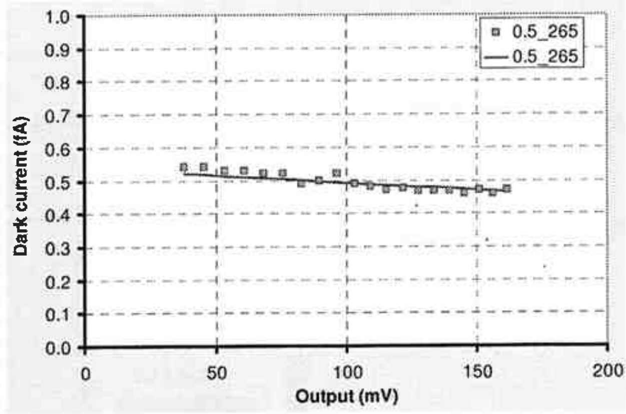


Figure 5: Trap-assisted tunneling (TAT) and SRH dark current behavior of the "hot" pixels

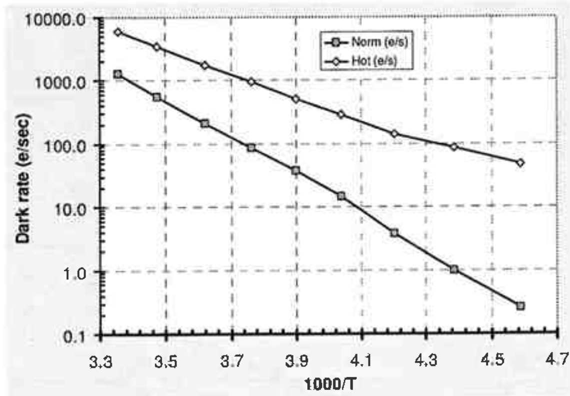


Figure 6: Measured dark current change with temperature (for a normal and a hot pixel)

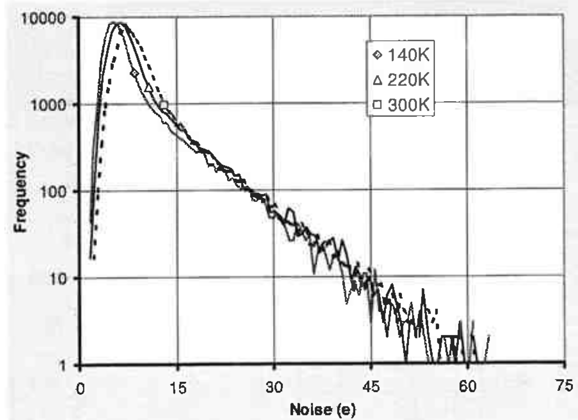
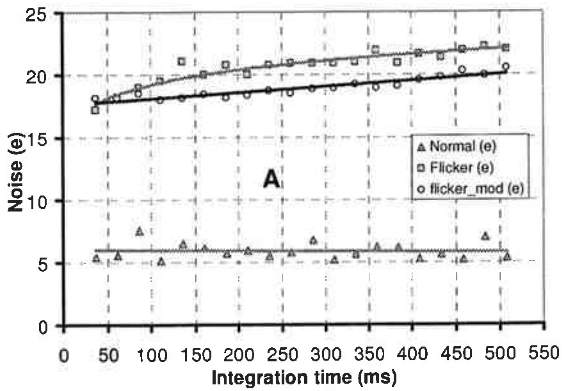
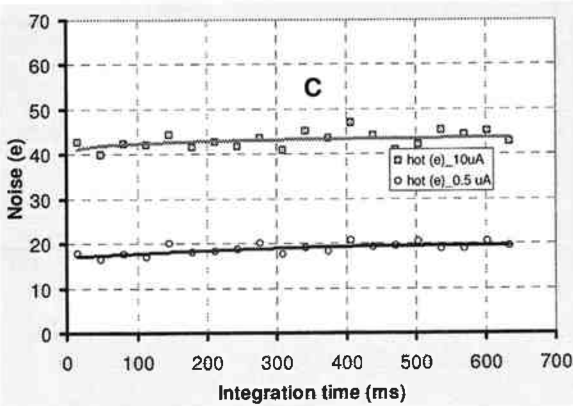


Figure 7: Read noise histogram at different temperatures





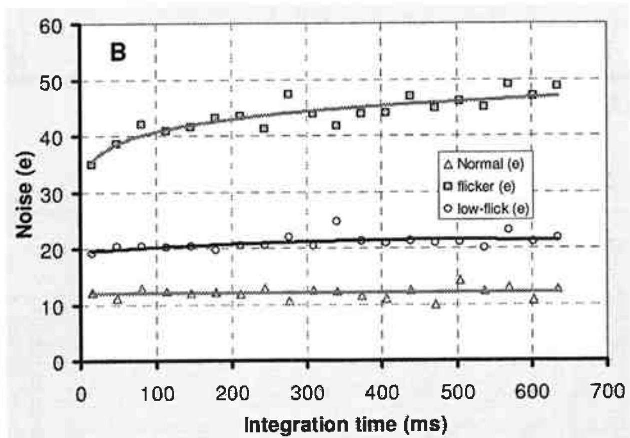


Figure 8: Read noise as a function of integration time: A and C are from one imager, and B is from a different imager, all implemented in 0.25 μm CMOS technology