P-18 Design of the PC-ISIS: Photon-Counting In-situ Storage Image Sensor

T. Goji ETOH[1*], Nao OHTSUKA[1], Toshiki ARAI[2], Hideki MUTOH[3], Dirk POGGEMANN[4], and Arno Ruckelshausen[4]

[1] Graduate School of Science and Engineering, Kinki University, JAPAN
[2] NHK Science and Technical Research Laboratories, JAPAN
[3] Link Research Corporation, JAPAN
[4] Fachhochschule Osnaburueck, GERMANY

Higashi-Osaka, 577-8502 JAPAN
TEL: +81-729-28-3130 FAX: +81-729-95-5192 e-mail: best2010@civileng.kindai.ac.jp

ABSTRACT

This paper presents a design of an image sensor of 10 Mega frames per second with photon-counting sensitivity.

In 2001, the authors developed an image sensor for an ultra-high-speed video camera of 1 Mfps for continuous image capturing of 103 frames[1]. The image sensor was an In-situ Storage Image Sensor (ISIS), which operates at a very high frame rate with high sensitivity and low noise. Much higher sensitivity is, however, necessary, when it is applied to a transmission electron microscope for researches on nano-technology, a fluorescence microscope for biological science, etc, especially when it is operated at more than 1,000 fps. An image sensor was proposed for the applications, which is a CCD image sensor with combination of innovative technologies: "ISIS" invented by the authors, "CCM", Charge Carrier Multiplication, invented by Hynecek, and a conventional backside-illumination. It provides photon-counting sensitivity with the theoretical maximum frame rate up to 100,000,000 fps. This sensor was named the PC-ISIS, the photon-counting ISIS. The basic structure was proposed and the performance was examined by means of simulations. Based on the results, the PC-ISIS was designed.

1. INTRODUCTION

In 1991, the authors developed a video camera of 4,500 fps with the pixel count of 256 x 256. The frame rate could be increased up to 40,500 fps by decreasing the pixel count. The sensor was a parallel readout sensor with sixteen readout taps. In 2001, they developed an image sensor and a video camera of which frame rate is 1,000,000 fps with the pixel count of about 80,000 pixels (312 x 260), as explained later in the section 2.

The high-speed video cameras have been applied to various scientific and engineering fields. Currently, nano- and bio-science and technology are the most attractive R and D topics. For applications of high-speed video cameras to these fields, the most serious problem is the lack of light. For example, strong illumination to a microscope immediately kills biological specimens. Therefore, sensitivity of the image sensor is the most important factor for designing the image sensor for the next-generation ultra-high speed video camera.

An image sensor was designed to achieve both photon-counting sensitivity and ultra-high frame rate, which was named the PC-ISIS, the Photon-Counting In-situ Storage Image Sensor. The PC-ISIS will be 250-time more sensitive than the previously-developed ISIS-V2, as explained below:

(1) The fill factors of the ISIS-V2 is 13.5%; that of the PC-ISIS is 100%, thanks to the backside illumination.
(2) Their average quantum efficiencies for visible light are about 20% and 60%, respectively.
(3) Noise floor of the readout amplifier of the ISIS-V2 is about 12 e-. If a charge packet are amplified by 12 times by CCM before readout, a signal of one electron can be detected from readout noise.

Therefore, the sensitivity of the proposed sensor is expected to be 266 (=100/13.5x60/20x12)-time higher.

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1) T. G. Etoh et. al., "A CCD Image Sensor of 1 Mframes/s for Continuous Image Capturing of 103 Frames", Proc. 2002 IEEE ISSCC, pp. 46-47, 2002.

The concept is illustrated in Fig.1. to Fig, 3. Major problems in the design are as follows:
(1) Prevention of migration of photoelectrons from the collection layer to the memory CCD channels through barrier of the p-well
(2) Prevention of direct intrusion of light to CCD channels, which are used for memory elements, fabricated in the front surface area
(3) Efficient transfer of photoelectrons from the collection layer to the memory CCD channels

This paper mainly describes the simulation results relating to the third topic, i.e., the transfer efficiency of generated photoelectrons from the collection layer to the memory CCD channels. The structure to solve the problem was sought by extensive simulation study. Based on the results, the practical PC-ISIS was designed.

2. The basic structure of PC-ISIS

2.1 Surface structure

The basic structure of the PC-ISIS is explained in Fig.1 to Fig.3. One pixel element is composed of a collection gate, an in-situ CCD storage channel stretching downward from the gate, and a drain attached at the end of each CCD storage channel. The center of a pixel is at the center of each collection gate, consisting of a pixel grid, which is slightly slanted to the CCD grid. The storage area is composed of the pixel array and vertical readout CCD channels with short bends stretching beside each column of the collection gates. A vertical readout CCD consists of a string of the last segments of in-situ CCD storage elements connected with CCD switches. The sensor consists of the photoreceptive area, four horizontal readout CCD channels, four diffusion amplifiers and four readout taps which are not shown in the figure.

2.2 Operation

2.2.1 Image capturing operation

The image capturing operation is shown in Fig. 2. Fig. 2 (a) and Fig.2 (b) show the states in which the image signals of the first two frames are recorded, and the image signals for the second to the sixteenth frames are recorded, respectively. In the latter case, the image signals for the first frame have already been

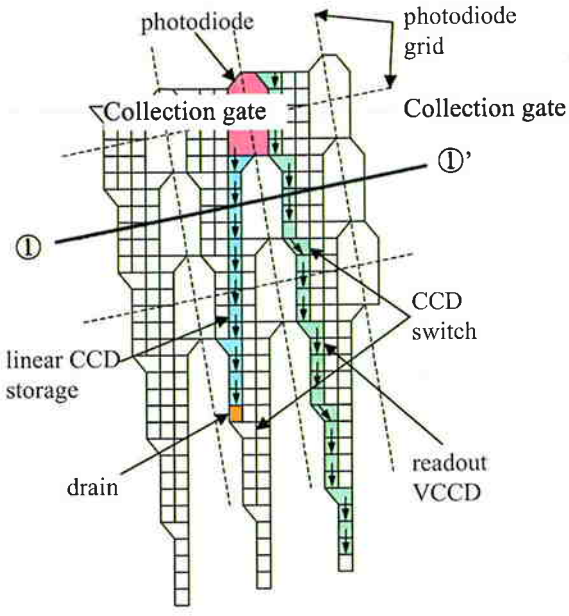

Fig. 1 The basic structure of an ISIS

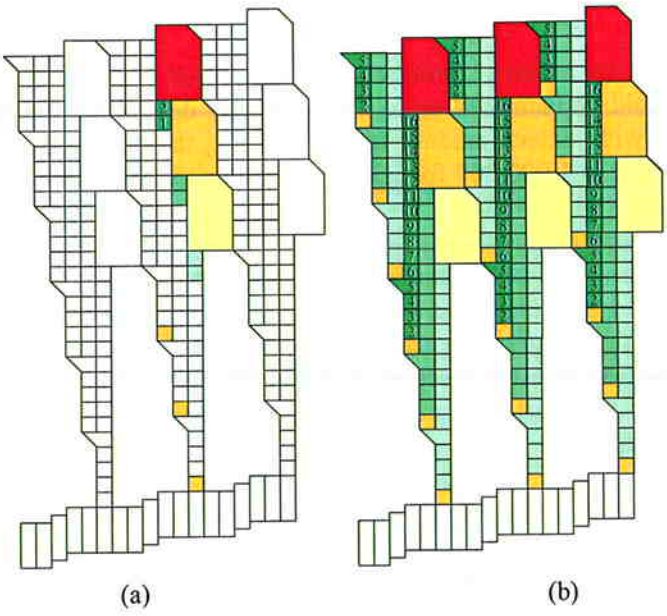

Fig. 2 Image capturing operation of the ISIS

(a) Image signals of the first and the second frames are stored in the CCD storage channels.

(b) Image signals of the second to the sixteenth frames are stored in the CCD storage channels. The storage area is full of image signals. The image signals of the first frame have been drained. By the continuous overwriting operation, the latest image signals are always kept within the image sensor until a target event occurs and the trigger signal to cease the continuous recording operation is released to the sensor.

drained to the outside of the sensor through the drain. The image capturing operation with the overwriting continues until the target event occurs and a trigger signal to stop the image capturing operation is released to the sensor.

2.2.2 Readout operation

After the image capturing operation ceased, the image signals stored in the in-situ storage are readout to a buffer memory outside the sensor and, finally, reconstructed as consecutive image frames. At first, the image signals stored in the vertical readout CCDs, i.e., the last segments of the storage CCD elements, are readout through the horizontal readout CCDs. When the vertical readout CCDs become empty, the image signals stored in the storage CCD elements are transferred to the vertical readout CCDs until the vertical readout CCDs are filled with the image signals. The operation is repeated until all the image signals are read out of the sensor and the in-situ storage CCDs become empty.

2.3 Cross-section structure

The cross section at ①-①' section in Fig.1 is explained in Fig. 3. The ISIS structure is installed on the surface of PC-ISIS. Therefore, the structure is more complex than that of the standard backside illuminated CCD. In this figure, arrows express flow of electrons.

The section flow is summarized as follows:
(1) Electron-hole pairs are generated by the incident light was the backside of the sensor.
(2) The holes are drained from the sensor. The electrons are transfered to collection gate through the collection layer, and to the CCD memory.

2.4 Performance of PC-ISIS

The specification and the performance of the designed PC-ISIS are summarized in Table 1.
(1) Pixel Size
Electrode pitch is 0.9 micron. Since we apply the standard 4-phase transfer scheme to the photo-receptive area, the length of a CCD cell is 3.6 microns. Each pixel consists of ten CCD channels, the collection gate and drains for holes and electrons. Each CCD channel has twelve CCD cells. The size of a pixel is the product of the size and the number of CCD cells in it, i.e., 3.6 microns x 12 elements = 43.2 microns.
(2) Thickness of the chip
To achieve fast electron transfer, the sensor should be completely depleted. Therefore, thinning process is applied to the chip to 20-30 micron-thick.

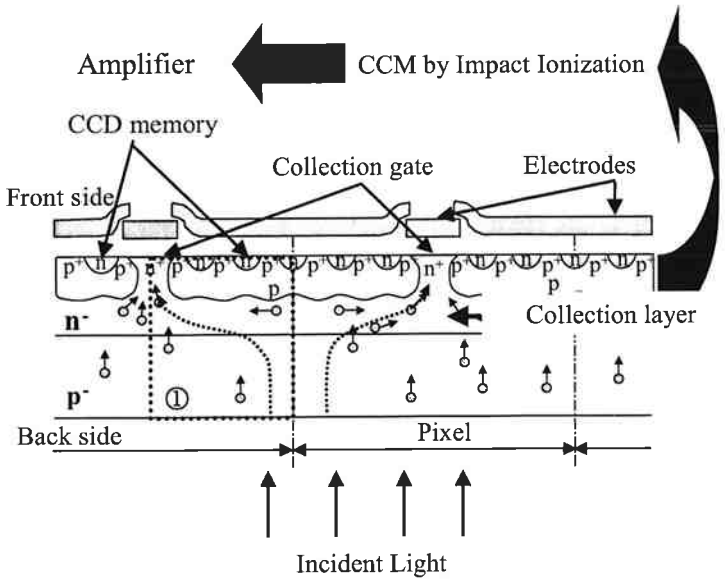

Fig. 3 Cross sectional explanation of the PC-ISIS
(Conceptual model)

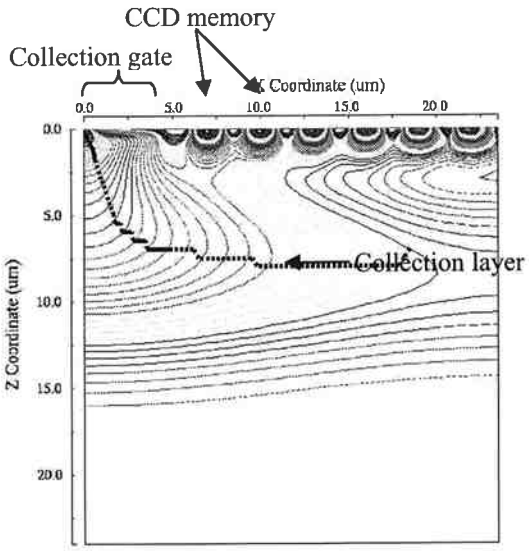

Fig. 4. A result of simulation
An electron path in the collection layer

(3) Pixel count and the size of the chip
The pixel count is more than 200 kpixel (480x420). The size of the photo-receptive area is 20.73x18.14 mm^2, calculated by multiplying the pixel size to the pixel count.
(4) Maximum frame rate
The frame rate is the inverse of the time for an electron to travel from the edge of a pixel to the collection gate through the collection layer, and finally to the input gate, i.e., the first element of the CCD storage. Along the electron path, sufficiently smooth electric field must be realized. Even if there is a slight up-and-down or a long flat root in the path, electrons are trapped or detained, which causes serious decrease of the traveling time. To achieve the maximum frame rate, the minimum electric potential gradient (electric field) in the path should be minimized. Extensive simulation study for the pixel of 43.2 x 43.2 $microns^2$ and the thickness of 21 microns has finally realized that the traveling time through the collection layer is 0.9 ns and that in the collection gate is 2.0 ns; the total is less than 3.0 ns. Therefore, the theoretical maximum frame rate of this sensor is expected to be less than 100,000,000 fps.
(5) Sensitivity
Since the PC-ISIS is a backside-illuminated image sensor, it is sensitive to ultraviolet rays and visible light. Infrared ray penetrates through the 21-micron-thick chip and reaches to the CCD storage channel made in the surface area. With combination of the fill factor of 100% by backside illumination and the amplification by impact ionization (CCM), the sensitivity is expected to be less than 10 photons for standard readout rate.
(6) Number of frames
The number of frames of continuously captured image is 117, which is the same number as the number of the CCD storage elements in a pixel.
(7) Other specification and functions
Overwriting mechanism is installed. Continuous parallel readout is also possible up to 500 fps for the full frame by installation of four parallel readout taps.

3. An Example of Simulation Results

3.1 Transfer in the collection layer

Fig. 4 shows a result of the simulation on electron traveling path in the collection layer, which was conceptually explained in Fig. 3. The electric potential is simulated for the cross-sectional area of a half of a pixel, i.e., the area between the centers of a collection layer and a collection gate.

Before simulation study, some conditions for electrons to travel smoothly in the layer are listed up and realized, which produces a very smooth and nearly constant potential gradient in the figure. The potential barrier from the collection layer to the CCD storage channel is sufficient.

A dotted line in Fig. 4 expresses the path of an electron that is put on an arbitrary place in the collection layer and travels to the collection gate. The traveling time of the electron is less than 1.0 ns.

Table 1. Specification of the PC-ISIS

	PC-ISIS
Frame Rate (Theoretical Maximum)	100,000,000 fps
Pixel Count	480 x 420 (=201,600) pixels
Pixel Size	43.2 x 43.2 microns2
Size of CCD Element	3.0 x 3.6 microns2
Fill Factor	100%
Number of Frames	117 frames
Transfer Scheme	4-phase transfer (Quasi 2-phase transfer for HCCD)
Temperature of the Sensor	(-20 ~ -40 degree)
CCM	installed
Sensitivity	10 Photons
Sensitive Wavelength	250 nm ~ 600 nm
Overwriting Operation	installed