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SOI CMOS Image Sensor with Pinned Photodiode on Handle Wafer

Yong Soo Cho, H. Takao*, K. Sawada*, M. Ishida*, and Sie Young Choi

School of Electronic and Electrical engineering, Kyungpook National University, 1370 Sankyuk-dong, Buk-gu, Daegu, 702-701, Korea; Email : ysensor@hotmail.com

*Department of Electrical and Electronic engineering, Toyohashi University of Technology, Toyohashi, 441-8580, Japan

Abstract

We fabricated 32 × 32 hybrid bulk/FDSOI CMOS active pixel image sensor with the p+/n-well/p-sub of photodiode structure to reduce dark current, improve quantum efficiency, and transfer photocarriers completely. The active pixel comprised of reset and source follower transistor on the SOI seed wafer, while the pinned photodiode, readout gate, and floating diffusion were fabricated on the SOI handle wafer. The pinned photodiode could be optimized because the process of a photodiode on the SOI handle wafer was independent of a transistor process on the SOI seed wafer. The source of dark current could be also eliminated by the planner process of hybrid bulk/FDSOI structure between localized oxidation of silicon and pinned photodiode. The most wavelength is absorbed in visible range, as a optimized pinned photodiode is located in handle wafer.

INTRODUCTION

Charge-coupled devices (CCD's) are currently the dominant technology for image sensors. CCD arrays with high fill-factor, small pixel sizes, and large formats have been achieved and some signal processing operations have been demonstrated with charge-domain circuits. However CCD's cannot be easily integrated with CMOS circuits due to additional fabrication complexity and increased cost. Also, CCD's are high capacitance devices so that on-chip CMOS drive electronics would dissipate prohibitively high power levels for large area arrays. Furthermore, CCD's need many different voltage levels to ensure high charge transfer efficiency. CMOS active pixel sensor (APS) has been a growing interest. The major reason for this interest is customer demand for miniaturized, low-power, and cost-effective imaging systems. CMOS-based image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics on-chip and reduce component and packing costs. It is now straight forward to envision a single-chip camera that has integrated timing and control electronics, sensor array, signal processing electronics, analog-to-digital converter (ADC) and full digital interface [1-2]. In order to extensively apply CMOS image sensors to mobile equipment which relies on the features of CMOS image sensors, such as low power supply voltage and low power consumption, it is necessary to establish simple and precise methods of suppressing fixed-pattern noise (FPN) inside the image sensors without depending on signal processing circuits. However, the dark current levels reported for CMOS APS imagers in current technologies are still more than an order of magnitude larger than those of the CCD sensors with the optical fabrication process [3-5].

SOI technology has been proven to be advantageous compared with the conventional bulk technology. Devices on FD-SOI display a steep sub-threshold slope, with low parasitic capacitances, making them appropriate for low-voltage, low-power application. By adopting fully depleted type SOI device structure, the many advantages of SOI which include low leakage current and low voltage high performance when used for digital circuits, improved high frequency characteristics for CMOS analog circuits, and good isolation between circuits in mixed signal applications. As a result, image sensors built on SOI will find many useful applications. However, to integrate image sensors on SOI substrate suffers from low quantum efficiency. Due to the limited depth of silicon available on the top film, most of the photons can

pass through the sensing regions without being absorbed. To overcome the barrier, a hybrid bulk/SOI pixel structure had been proposed [6-7]. The photodiode built on the bottom substrate. The performance of the APS is expected to be similar to the bulk technology with potentially higher speed due to the lower capacitance that the photos to drive in SOI technology. To improve on the diode dark current, implants hold the si-sio$_2$ interface in equilibrium to eliminate interface-related dark current generation. The surface implant also prevents a tunneling between heavily-doped areas, and reduces the surface electric field [8].

In this paper, we fabricated 32 × 32 hybrid bulk/FDSOI CMOS active pixel image sensor (APS) with a pinned photodiode on the handle wafer to optimize the formation of a photodiode, reduce dark current and transfer photocarriers completely. The pinned photodiode can be optimized for quantum efficiency and low dark current. First, the most wavelength is absorbed in visible range, as a photodiode is located in handle wafer. Second, the employing pinned photodiode is an effective device to reduce dark current. The source of dark current can be eliminated by the hybrid bulk/FDSOI APS process between localized oxidation of silicon and pinned photodiode. Third, the fully depleted SOI process enables the SOI image sensor to optimize photodiode because the pinned photodiode on the handle wafer is independent of the MOSFET device on seed wafer.

EXPERIMENT

The hybrid bulk/FDSOI CMOS active pixel image sensor (APS) is fabricated on UNIBOND wafer with a seed wafer thickness of 0.1 µm and a buried oxide (BOX) thickness of 0.2 µm. The fabricated APS is the conventional four-transistor type pixel structure which has a readout gate, a reset transistor, an amplification transistor, and a row address transistor [9]. The active pixel comprised of reset and source follower transistor on the SOI seed wafer, while a pinned photodiode, a readout gate, and a floating diffusion were fabricated on the SOI handle wafer. The effective size of photodiode is 20 µm * 20 µm and the transistor size of FDSOI is a width/length of 12 µm/ 5 µm.

The photodiode is formed by an extra etching step with one extra mask to remove the BOX layer on the SOI handle wafer. It is well known that a pinned photodiode as a photodiode is an easy and effective way to reduce the noise of dark current. We applied a pinned photodiode to the CMOS image sensor to reduce the surface dark current. The photodiode structure of p+/n-well/p-sub has a shallow junction with the depletion depth and the absorption depth. The depletion depth is controlled by an implantation concentration and drive-in time. In this pinned photodiode, the p+ region on the surface supresses the noise caused by the interface traps located on the surface of the photodiode (PD) and the trasfer gate. The concentration of n-well and p+ is very important to form perfect depletion layer and transfer charges. The pinned photodiode has an effective dimension of 20 µm * 20 µm.

Readout gate and Floating Diffusion (FD) is also fabricated on the SOI handle wafer. The concentration of FD is considered as the leakage current of FD and capacitance amplification. The channel stop process of the p-implant around the pinned photodiode and FD eliminates the defect of the Si-SiO$_2$ interface related to the generaton of dark current. The process of FDSOI transistor is simpler than bulk or partially-depleted (PD) SOI, which one mask step is saved at least, and is able to be scaled down without LOCOS process. The isolation way of the active silicon islands from one another is simple by mesa isolation technique. FDSOI transistors comprised of APS is fabricated with a convertional FDSOI CMOS process on the seed wafer. Figure 1 shows cross-sectional view of a hybrid bulk/FDSOI CMOS active one pixel image sensor placing the photodiode on the SOI handle wafer.

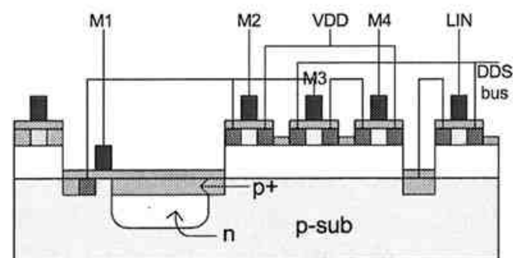


Figure 1. Cross-sectional view of a hybrid bulk/FD-SOI CMOS active one pixel image sensor placing the photodiode on the SOI handle wafer.

DISCUSSION

Dark current cannot be accurately determined analytically or using device simulation tools. The dark current can only be accurately determined experimentally. The leakage current between LOCOS and n-type region of the photodiode has been known as the main sources of junction leakage currents. By using Hybrid bulk/SOI pixel structure, the junction between LOCOS and n-type region of the photodiode can be eliminated and dark currents can be suppressed significantly. Figure 2 shows the dark current as a function of FD voltage in case of TX = 0 V and TX = 3.3 V. As the FD voltage is increased, the leakage current is increased gradually. We measured the leakage current in case of TX = 0 V and TX = 3.3 V, respectly. The result shows that leakage current is almost same, as the source of leakage current is removed by using SOI planner process.

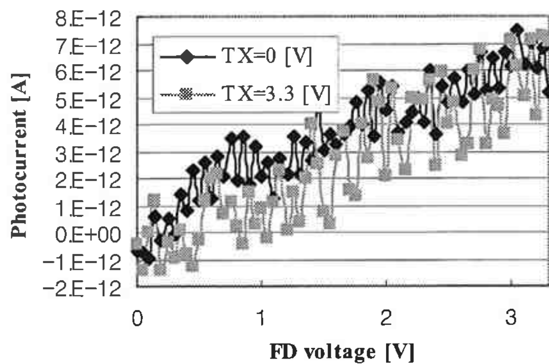


Figure 2. The dark current as a function of FD voltage in case of TX = 0 V and TX = 3.3 V.

Signal charges are transferred by a readout gate voltage. Figure 3 shows the photodiode operation by a readout gate voltage. The dark current is not changed by readout gate voltage in dark. When the white light source is illuminated, however, the output optical current is changed above the threshold voltage of readout gate at 3.3 V of FD voltage. The threshold voltage of the readout gate is about 0.7 V.

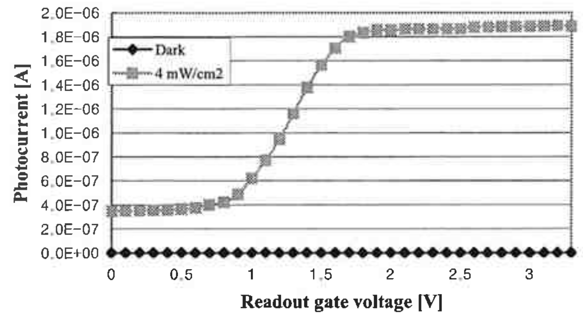
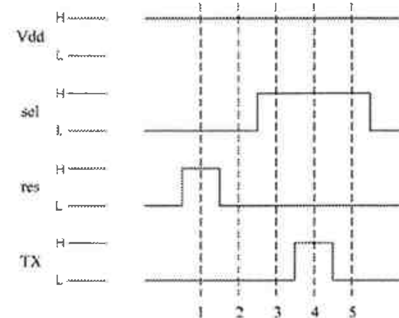
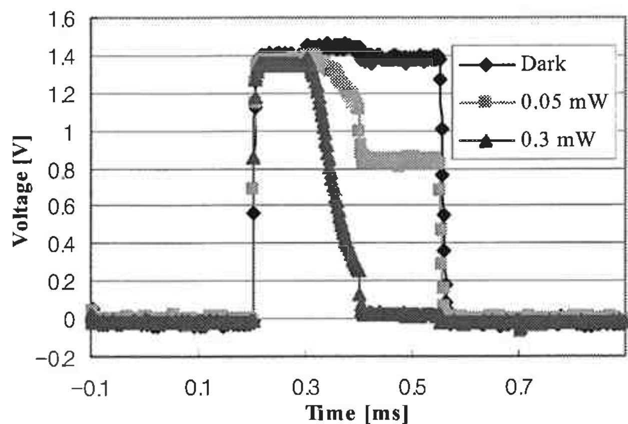


Figure 3. Photodiode operation by a readout gate voltage under dark current and 4 mW/cm^2 at 3.3 V of FD voltage.

The hybrid bulk/SOI CMOS APS configuration is shown Fig. 1. M1 is the readout gate, M2 is the reset gate for FD, M3 is the source follower, and M4 is the select gate. A series of pulses are applied to the gate of the reset transistor to reset the gate voltage of M2 to a high voltage before the start of the current integration. When M1 is applied high voltage, the photodiode will then discharge, the charge stored at FD and the resulting voltage is reflected by the source follower to the output. Figure 4 (a) shows timing chart for APS read out with $V_{DD,}$ select, reset, and readout gate. We measured the voltage output of the active pixel. When a readout gate is applied high voltage, electrons in a photodiode will transfer to floating diffusion and the resulting voltage is reflected by the source follower. To measure the output of APS, a V_{DD} of 3.3 V is applied and a 1.4 V is applied at the transistor for resistor. Figure 5 (b) shows the voltage output of the one pixel at a 3.3 V of V_{DD}. The results are the output voltage of the one pixel under different illumination intensities from a white light source.



(a)



(b)

Figure 4. (a) Timing chart for APS read out, (b) The output voltage of the one pixel under different illumination intensities from a white light source at a 3.3 V of V_{DD}. (Blue : Dark, Red : 50 μW, Brown : 300 μW)

The photograph of the overall architecture of 32 × 32 SOI CMOS APS is shown in Fig. 5. The image sensor consists of 32 × 32 array of pixels, vertical scanner, horrizontal scanner, and DDS (delta difference sampling) to suppress FPN.

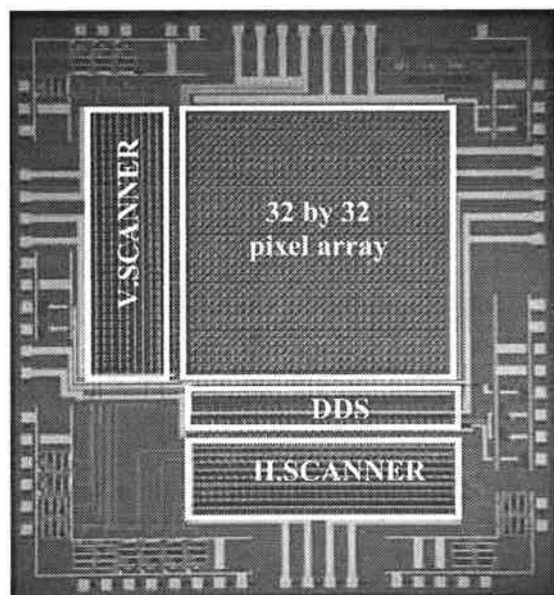


Figure 5. Photograph of fabricated 32 × 32 SOI CMOS active pixel sensor with vertical scanner, horizontal scanner, and delta difference sampling by 5 μm rule SOI process.

CONCLUSION

We have fabricated 32 × 32 hybrid bulk/FDSOI CMOS active pixel image sensor with a pinned photodiode on handle wafer. It could be optimized the photodiode, as a employing pinned photodiode process was independent of a transistor process on the SOI seed wafer. By using the hybrid one pixel structure, the source of dark current could be also eliminated between localized oxidation of silicon and pinned photodiode. We have shown that dark currents can be suppressed significantly. The SOI CMOS APS with pinned photodiode on handle wafer is able to use 4-transistor type CMOS active pixel sensor for high perfomance and space application.

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