

P7 APS Column Fixed Pattern Noise Reduction

Thalis Anaxagoras, Simon Triger, Nigel M. Allinson
Department of Electronic and Electrical Engineering
University of Sheffield, S1 3JD, UK

Renato Turchetta
Rutherford Appleton Laboratory, CCLRC,
Chilton, OX11 0QX, UK

T.anaxagoras@rl.ac.uk

Abstract

A significant shortcoming of Active Pixel Sensors (APS) is their high Fixed Pattern Noise (FPN). We present here simple techniques for reducing FPN in such sensors together with practical implementations in the AMS 0.35 μ m CMOS process. The first method is based on alternate column readouts and is effective in reducing column FPN. The two other approaches are based on applying varying voltages to the input of the column amplifiers and to the drain of the pixel reset transistors respectively. While the first of these approaches is again effective in decreasing column FPN, the second reduces both the pixel and column FPN. They are both effective in reducing non-linearities, respectively, in the response of the column amplifiers and in the combination of the pixel and column amplifiers. Simulation results reveal that the FPN can be reduced by up to 25 dB.

1. Introduction

An important factor limiting the performance of APS is the non-uniformity in response due to gain and offset variations at the pixel and column levels. The presence of amplifiers in each individual pixel means that CMOS sensors suffer from higher non-uniformity than CCDs, which are normally read-out through a few or even a single output amplifier [1]. A measure of the non-uniformity is given by the FPN, which can be defined as the spatial variations in pixel output under uniform illumination and is due to device and interconnect parameter variations (mismatches) across the sensor. Though FPN increases with illumination it produces more serious degradation in image quality at low illumination levels.

To counteract these variations, a one-time calibration procedure is normally used to reduce the effect of these fixed variations with typically off-chip digital calibration is used to correct the FPN. The simplest method requires recording two different uniform images of the array. The pixel gains and offsets are computed and stored externally to the APS chip. This one-time calibration procedure does not take into account variations in operating parameters with temperature, time or, as in some of our applications, radiation damage. An alternate technique involves measuring the column FPN by averaging all the pixels in a column in a dark image: this gives a reduction of the column offsets but not for any gain variations [2]. Scene-based algorithms have been developed for non-uniformity correction [3-5] with some encouraging results reported. There are two major problems with existing scene-based algorithms. Firstly, real-time hardware implementation is difficult because of the complicated computations involved and, secondly, the presence of ghosting artefacts.

Recent sensors have reduced FPN by using analogue-signal-processing circuits [7] such as correlated double sampling (CDS) circuits that are placed on the periphery of the pixel array. In CDS, the pixel output is sampled immediately after the reset operation at the beginning of the integration period and again at the end of the integration period. CDS does not cancel any gain variation FPN and requires additional circuitry on-chip.

2. Alternate column readout

The first test structure we are designing is based on alternate column readout. This structure is based on the ability to shift the information between two adjacent columns. In this way each column of pixels can be alternatively read-out through two column amplifiers, one corresponding to the selected column and the other to the neighbouring one. Fig. 1 shows a schematic of the architecture for three columns. Column FPN appears as "stripes" in the image (Fig. 2b) and can result in substantial image quality degradation. This method can be used in two ways. Firstly, by reading out the pixel of one column alternatively through the different columns to cancel some of the column FPN effects. This is illustrated in Fig. 2c. In this way, the column FPN will be averaged and so variations reduced. More reduction can be achieved by introducing more than two columns in the read-out scheme. An advantage of this method is no requirement for additional processing power or external memory; however, providing many alternate column read-outs requires extensive on-chip multiplexers. Only the average column FPN is reduced, but this is effective as the human eye is more sensitive to the structured appearance of column FPN effects than to the random noise of pixel FPN.

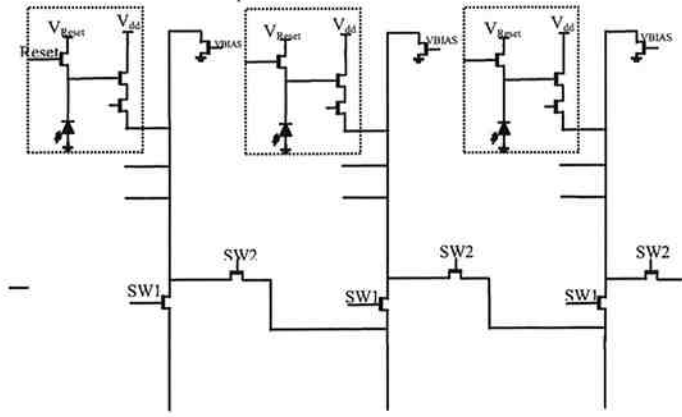


Fig. 1: Alternate column readout

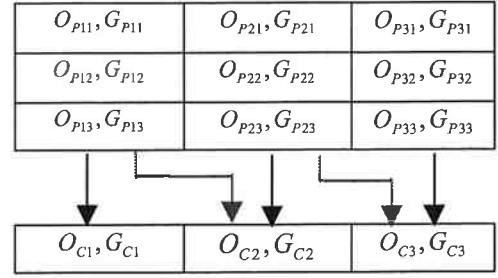


Fig. 3: 3x3 array/columns with gains and offsets indicated

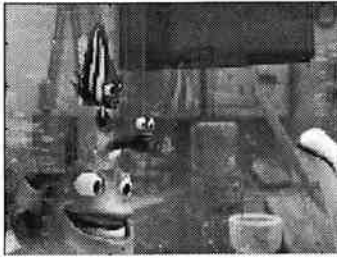


Fig. 2a: Original image

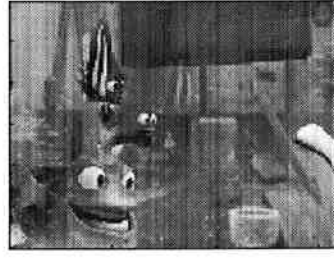


Fig. 2b: Image with column FPN

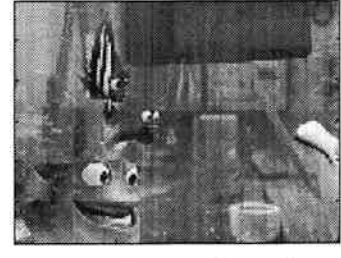


Fig. 2c: Alternate column readout

The second way of using this architecture is to find the ratio of the gains of the output buffers through simple calculations. In this manner, column gain variations can be compensated. This can be achieved by resetting the pixel with a given voltage and measuring the output of the pixel with zero exposure time. This has to be done for each pathway for the individual pixels. The values stored and used for the offset calibration. Assuming a 3x3 array with the corresponding gains and offsets shown in Fig. 3, where O_p/G_p and O_c/G_c are the pixel and column offsets/gains respectively. A concise relationship for the output of pixel (1, 1) is given by:

$$Y_{(P11)(C1)} = G_{P11}G_{C1}(\text{Signal}_{P11}) + G_{C1}O_{P11} + O_{C1} + N \quad (1)$$

Where N is the temporal noise. Temporal averaging of the results to improve accuracy can also be considered if temporal noise is a problem. The same pixel readout through the adjacent column is given by:

$$Y_{(P11)(C2)} = G_{P11}G_{C2}(\text{Signal}_{P11}) + G_{C2}O_{P11} + O_{C2} \quad (2)$$

The same procedure is carried out for the other columns and pixels. Namely,

$$Y_{(P21)(C2)} = G_{P21}G_{C2}(\text{Signal}_{P21}) + G_{C2}O_{P21} + O_{C2} \quad (3)$$

$$Y_{(P21)(C3)} = G_{P21}G_{C3}(\text{Signal}_{P21}) + G_{C3}O_{P21} + O_{C3} \quad (4)$$

$$Y_{(P31)(C3)} = G_{P31}G_{C3}(\text{Signal}_{P31}) + G_{C3}O_{P31} + O_{C3} \quad (5)$$

The offsets recorded and stored in a table

$$G_{C1}O_{P11} + O_{11} = O_{(P11)(C1)} \quad (6)$$

$$G_{C2}O_{P11} + O_{11} = O_{(P11)(C2)} \quad (7)$$

By subtracting these offsets from the measured values, the ratio between the columns can be found.

$$Y_{(P11)(C1)} - O_{(P11)(C1)} = G_{P11}G_{C1}(\text{Signal}_{P11}) \quad (8)$$

$$Y_{(P11)(C2)} - O_{(P11)(C2)} = G_{P11}G_{C2}(\text{Signal}_{P11}) \quad (9)$$

Dividing the two equations result to the ratio of column gains. In a similar manner all the ratios can be found.

$$\frac{G_{C1}}{G_{C2}}, \frac{G_{C2}}{G_{C3}}, \frac{G_{C3}}{G_{C4}} \quad (10)$$

By multiplying the array values with the appropriate ratio for each column, the column FPN completely cancels by assuming all the columns have the same gain. The accumulation of the correction terms is performed over an entire image. Unfortunately, this means that measurement errors in one correction term may be distributed across several other terms. To overcome this problem, averaging techniques can be used (e.g., using more than one pixel in each column) and the ratio is used only for a limited number of columns and not for the entire array.

3. Exploiting column reference signals

The calibration of a sensor can be performed by sequentially applying several reference signals at the sensor input, and measuring the sensor output signal. Here different voltages are applied at the output stage amplifiers and the corresponding output of the column measured. In this way the gains and offsets of each column can be determined. This architecture is shown in the Fig. 4. The proposed test structure has been examined for mismatches using a Monte Carlo simulation and so producing a best-fit line to calculate the gain and offset of each column.

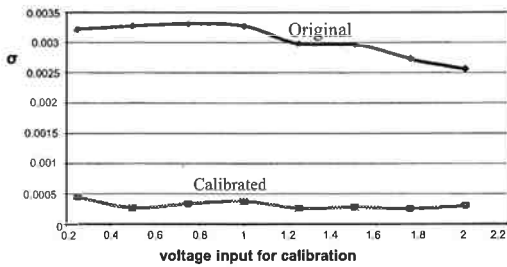


Fig. 5: S.D. for all columns vs. input voltage

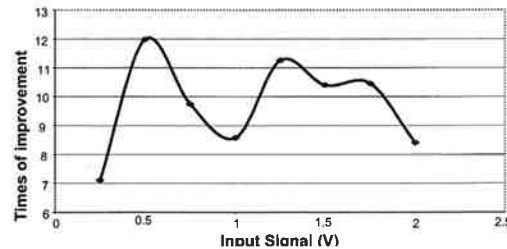


Fig. 6: Ratio of S.D. for output voltage after and before correction

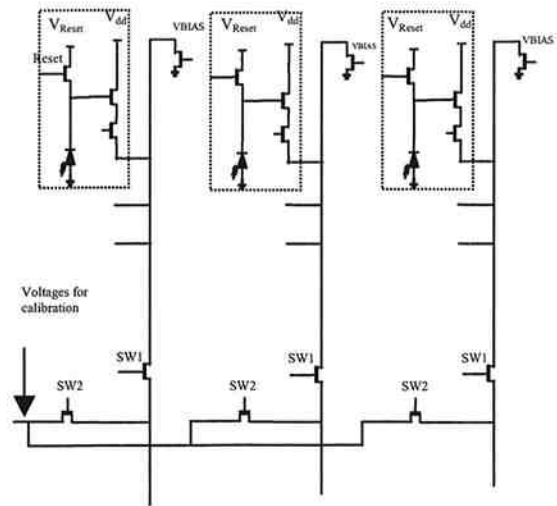


Fig. 4: Constant voltage method calibration

The offsets, O , and gains, G , could be found in the usual way as,

$$O = \frac{n(\sum xy) - (\sum x)(\sum y)}{n(\sum (x^2)) - (\sum x)^2} \quad G = \frac{(\sum y)(\sum (x^2)) - (\sum x)(\sum xy)}{n(\sum (x^2)) - (\sum x)^2} \quad (11)$$

where x is the input reference voltage and y is the output of a column amplifier.

The simulations indicate that the column FPN is reduced up to a factor of 12 (Fig. 6). This simple and efficient method can be used in a conventional APS to improve the column level FPN. Constant voltages can be applied at the read-out circuit during the exposure time for the calibration procedure, and averaging techniques can be used to improve further the sample accuracy by reducing the effect of thermal noise.

The practicality of this approach is demonstrated below by considering a typical imager requirement and could be implemented using a typical FPGA device. The time required to perform the calibration is proportional to the number of reference voltages applied. In total, the sum of the column outputs, the sum of the inputs, sum of the input square and the sum of the products need to be stored. By choosing the number of calibrated voltages, n , to be of power of 2 will minimise the number of multiplications. FPGA utilisation is limited by the amount of multipliers and here we assume an XC2VPX20 device with 88 available multipliers. In this case where the number of calibration voltages is 4 there will be 12 multiples per offset and gain calculation. Using 12 multipliers would allow 7 columns to be calibrated at any one time, with 75 sets of calibrations necessary for a 525 column sensor. Optimistically, assuming a 135 MHz clock, with an iterative divide process that takes 10 clock cycles to perform, 13.5 M divides can be performed per second and this equates to 180,000 frames/sec. In terms of memory requirements, for each calibration level one needs to store at least one 10-bit voltage input (assuming 10-bit ADC), 525 x 10 bit output voltage levels, 525 x 10 bit gain levels and 525x10 bit offsets level giving in total 15,760 bits. As the chosen FPGA has 88 x 18 kbit Block Select RAM, there will not be any need for external memory.

4. Exploiting pixel reference signals

The third method applies a reference voltage to V_{reset} , which is connected to a separate pad instead of being connected to V_{dd} . This method is similar to the previous one, but can take into account pixel-to-pixel variations.

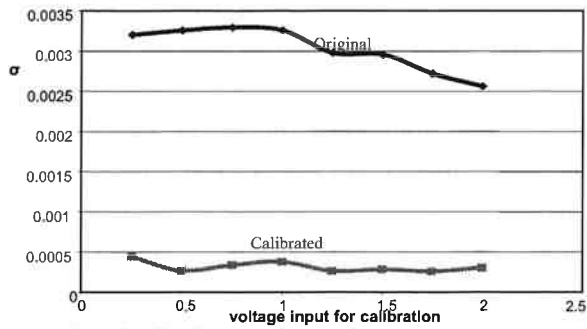


Fig. 7: S.D. for all columns vs. input voltage

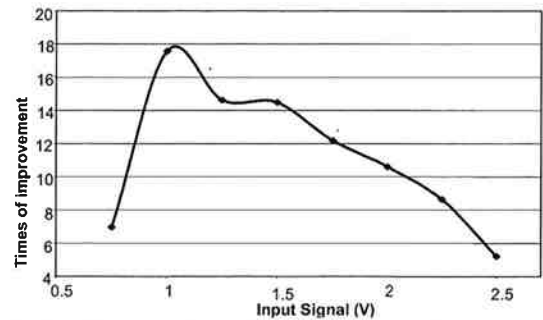


Fig. 8: Ratio of S.D. on output voltage after and before the correction.

Again a test structure was examined for mismatches using a Monte Carlo simulation and so produce the best-fit line (to estimate the gain and offset of each column). The simulations indicate that the FPN is reduced by up to 18 times. The results are presented in Figs. 7 and 8.

Although this technique is superior to the previous ones, there is a need to store the calibration parameters for each individual pixel separately. There are also timing requirements to take dark-field images at the corresponding reset values. Of course, this can only be undertaken periodically for updating the calibration parameters, in order not to increase the power consumption significantly. An FPGA solution by itself might not be sufficient and additional memory might be needed to store the data depending on the size of the array.

5. Conclusions

Three computational methods to reduce the effect of gain and offset FPN have been presented and these methods will be implemented in test structures that will be fabricated in a 0.35 μm CMOS technology.

6. Acknowledgements

This work is part of the UK Basic Technology Programme, Multi-dimensional Intelligent Integrated Imaging (EPSRC Ref. GR/S85733/01).

7. References

- [1] E. R. Fossum, "CMOS image sensors: electronic camera-on-a-chip," *IEEE Transactions on Electron Devices*, vol. 44, pp. 1689-98, 1997.
- [2] Albert Theuwissen "Course On Digital Imaging: Image Capturing, Image Sensors, Technologies and Applications", CEI-Europe Advance Technology Education, Nice, France, November 22-26, 2004.
- [3] J. G. Harris and Y.-M. Chiang, "Nonuniformity correction using the constant-statistics constraint: analog and digital implementations [for IR FPA]," *Proceedings of the SPIE - The International Society for Optical Engineering, Infrared Technology and Applications XXIII*, 20-25 April 1997, vol. 3061, pp. 895-905, 1997.
- [4] Y.-M. Chiang and J. G. Harris, "An analog integrated circuit for continuous-time gain and offset calibration of sensor arrays," *Analog Integrated Circuits and Signal Processing*, vol. 12, pp. 231-8, 1997.
- [5] B.M. Ratliff, M.M. Hayat, R.C. Hardie: "An algebraic algorithm for nonuniformity correction in focal-plane arrays," *The Journal of the Optical Society of America A*, vol. 19, p 1737-1747, September 2002
- [6] R.C. Hardie, M.M. Hayat, E. Armstrong, B. Yasuda: "Scenebased nonuniformity correction with video sequences and registration, *Applied Optics*", vol. 39, no. 8, p 1241-1250, March 2000
- [7] Guy Meynants, Bart Dierickx, Dirk Uwaerts, Jan Bogaerts "Fixed pattern noise suppression by a differential readout chain for a radiation tolerant image sensor" *IEEE workshop on Charge-Coupled Devices and Advanced Image Sensors*, pp. 56-59, June 2001.