A BACK-ILLUMINATED MEGAPIXEL CMOS IMAGE SENSOR

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Imaging with a back-illuminated CMOS imager provides a number of advantages, especially as the pixel size is reduced. These advantages include high (100%) fill-factor and increased quantum efficiency, efficient implementation of antireflection coatings, improved angular response, availability of the traditional "frontside" of the pixel to incorporate in-pixel processing circuits, and increased compatibility with the next generation metals (e.g Cu) and low-k dielectrics.

In this paper, we present the test and characterization results for a back-illuminated megapixel CMOS imager. The imager pixel consists of a standard junction photodiode coupled to a three transistor-per-pixel switched source-follower readout [1]. The imager also consists of integrated timing and control and bias generation circuits, and provides analog output. The analog column-scan circuits were implemented in such a way that the imager could be configured to run in off-chip correlated double-sampling (CDS) mode. The imager was originally designed for normal front-illuminated operation, and was fabricated in a commercially available 0.5 μm triple-metal CMOS-imager compatible process. For backside illumination, the imager was thinned by etching away the substrate was etched away in a post-fabrication processing step.

Figure 1 shows the schematic cross-section of the back-illuminated CMOS APS. The device structure consists of a low-doped (~ $3 \times 10^{14}/cm^3$) epitaxial p-type silicon, with the photo-detecting junction formed by a front-implanted n-well and the p-type epitaxial silicon. Photons enter the detector from the backside, and the resultant photo-electrons are collected in the front-side p-nwell junction.

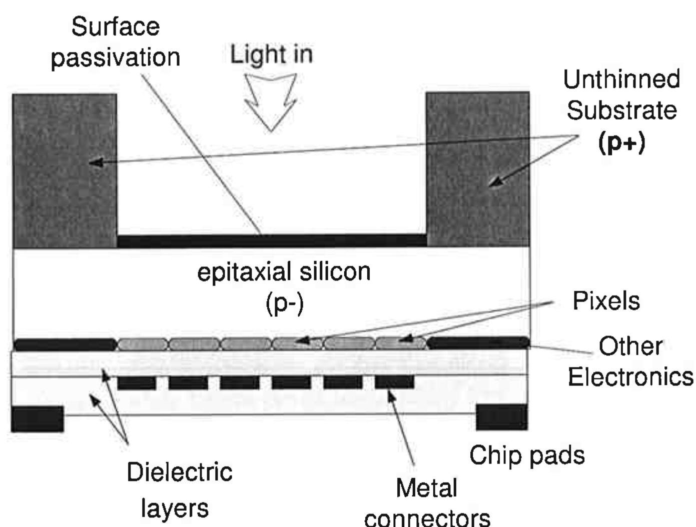

Figure 1: Schematic cross-section of the back-illuminated imager

The imager was thinned at an individual die level using a frame-thinning approach. Only the pixel area was thinned down to ~ 7-10 μm thickness (corresponding to epitaxial silicon thickness), leaving a thick peripheral region (~ 1 mm wide). A surface passivation step was then applied to the thinned silicon layer.

The resultant structure provides increased mechanical stability, a significant ease of die handling, and protection against wrinkling of the thinned die. This approach is well-suited for a CMOS imager, since the imager consists not only of the pixels, but the support and signal chain electronics along the periphery of the pixel array.

Backside thinning was carried out as follows. First, the front-side of the die is attached to a protective wax. Then a protective frame on the backside was created through deposition and patterning of a Si_3N_4 mask. The unmasked p^+ silicon substrate (with doping ~ $1 \times 10^{19}/cm^3$) was then etched using hot KOH down to within ~ 10 μm of the final silicon thickness. The remainder of the etching was carried out in $HF:HNO_3:CH_3COOH$ solution (HNA etch) [2]. HNA etches silicon through a redox reaction where the silicon oxidation rate is dependent on the doping concentration. Due to its doping concentration dependence, the etch-rate significantly slows down when the silicon substrate is etched, leaving an optically flat thin (~ 10 μm thick) epitaxial silicon layer. Following thinning, the front-side wax was removed, and the die was packaged in a standard pin-grid array (PGA) package (with its central portion removed to let light in) using a standard wire-bonding technique.

Passivation of the etched silicon presents a unique challenge. After thinning, the interface trap density at the unterminated silicon surface is unacceptably high, while a naturally formed native oxide (~20 °A thickness) causes the surface to become positively charged. Unwanted band-bending and the presence of dangling bonds result in a loss of QE and abnormally high dark currents, necessitating the use of post-metallization surface-passivation steps. Unfortunately, any post-metallization process step is challenging, since due to the presence of front-side metal with low melting point (~ 400°C), no high temperature step can be used. Thus, boron implantation and high-temperature furnace anneal is ruled out.

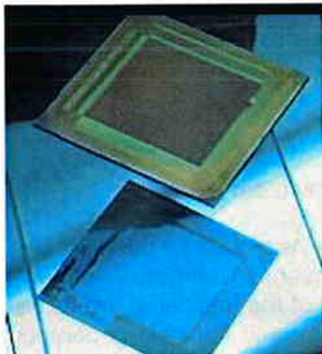

Figure 2: Photograph of the thinned megapixel imager

Self-passivation can achieved by controlling the HF concentration during the final stages of etching that leaves behind a 30-50°A oxide. However, the lack of a well-defined end-point of the etching process makes it difficult to carry out reliable self-passivation of the etched silicon surface. To get around this problem, some CCDs have used alternate passivation techniques that include UV-flooding, flash gates (MBE deposited mono-layer of metal), boron-doping followed by high-energy pulsed-laser anneal, and low-pressure oxide deposition [3,4,5,6].

We have used a delta-doping technique for surface passivation [7]. The technique consists of a low-temperature molecular beam epitaxy (MBE) that places an extremely high density of dopant atoms (> 10^{14} Boron/cm^2) within a few atomic layers of the surface with no observable crystal defects and no requirement for post-growth annealing, making it compatible with post-metallization processing. Delta-doping is carried out under ultra-high vacuum conditions (10^{-10} torr) using electron-beam evaporation of elemental silicon and thermal evaporation of elemental boron. The process steps are as follows. A 1 nm-thick p+ silicon layer was grown first, followed by depositing ~30% of a monolayer of boron atoms. 1.5 nm-thick capping layer of epitaxial silicon was then grown. After removal from the MBE system, oxidation of the silicon capping layer protects the buried delta-doped layer. Finally, the resultant optically flat surface allows easy deposition of anti-reflection coating using deposited oxides and plasma-enhanced silicon nitrides.

Figure 3: Captured image with two back-thinned megapixel imagers

Figure 2 shows the die level picture of the back-thinned imager. The unthinned frame is clearly visible in the picture. One of the advantages of the thinning approach described above is that the back-illuminated imager is packaged using conventional packaging techniques only.

Figure 3 shows captured images with two back-illuminated CMOS imagers. The problem with the first imager is clearly visible in figure 3 (left). Following thinning, the imager developed crystallographic defects resulting in the loss of one column and multiple imager rows. The second imager showed no such problems, resulting in an excellent quality image as shown in figure 3 (right). The circular aperture shown in the images correspond to the opening that was cut in the PGA package to let light in.

Without delta-doping, the imager showed very high dark currents, and was virtually inoperable. After delta-

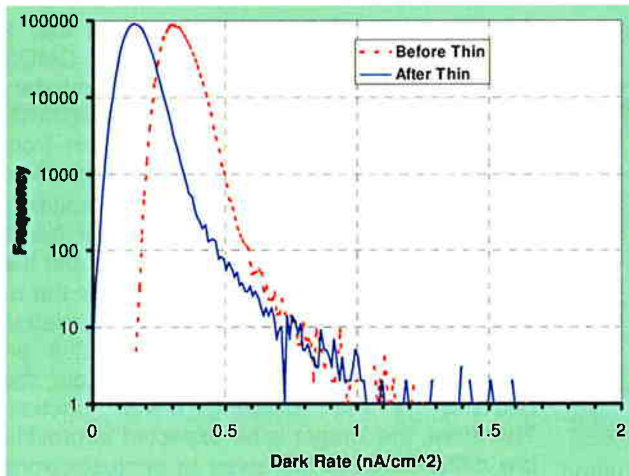

Figure 4: Dark current distribution of the megapixel imager before and after thinning

doping, however, the dark current was reduced to normal levels. In fact, as shown in figure 4, the modal dark current dropped below its original value. The modal dark rate before thinning was 294 pA/cm^2, and was reduced below 153 pA/cm^2, indicating the efficacy of delta-doping for trap interface trap passivation.

Figure 5 shows the measured quantum efficiency (QE) of the CMOS imager, before and after thinning. QE for the back-illuminated CMOS imager is shown as square dots, while the QEs for the same imager measured from the front-side - before (triangles) and after thinning (diamonds) - are shown in the same figure for comparison. Figure 5 clearly indicates the benefits of 100% fill-factor. Without any anti-reflection coating added to the backside, QE increased by a factor 2.6x in blue, 2.5x in green, and 2.7x in red.

We have compared the measured back-illuminated QE against existing back-illuminated imager QE models [8,9]. Figure 6 shows the measured QE before and after the application of anti-reflection coating. The measured data is shown in dots, and the modeled QE is shown as dashed lines. The data fits the model with a surface recombination velocity of 6x10^4 cm/s and an epitaxial silicon thickness of 7 μm. With reflection losses limiting the QE, it can be seen from figure 6 that, except at shorter wavelengths, the QE data without AR coating agrees with the modeled QE very well. Figure 6 also shows that with AR coating, QE increased to ~ 90% in green, although the variance from the model is larger, possibly indicating the need for improved AR coating design.

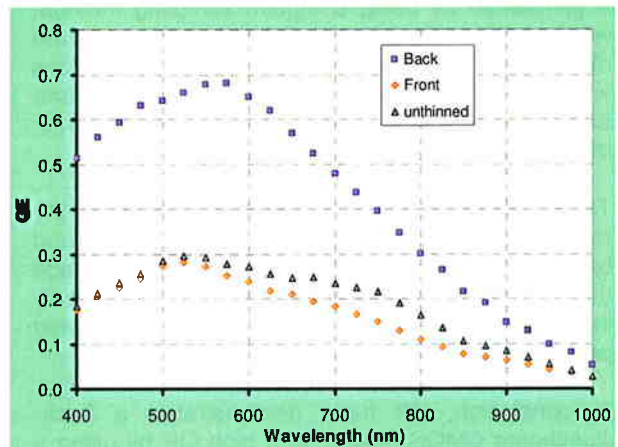

Figure 5: Measured QE of the megapixel imager – comparison between back and front illumination

A relatively fast drop off of the QE with increasing wavelength is indicative of the limited silicon thickness (~ 7 um) in the imaging area. In addition, since the imager was not originally designed for back-illumination, it did not have sufficient metal covering over the front-side of the pixel. As a result, the imager shows reduced red response due to a diminished optical collection of longer wavelength light. However, the QE in the red region is sufficient for consumer imaging applications.

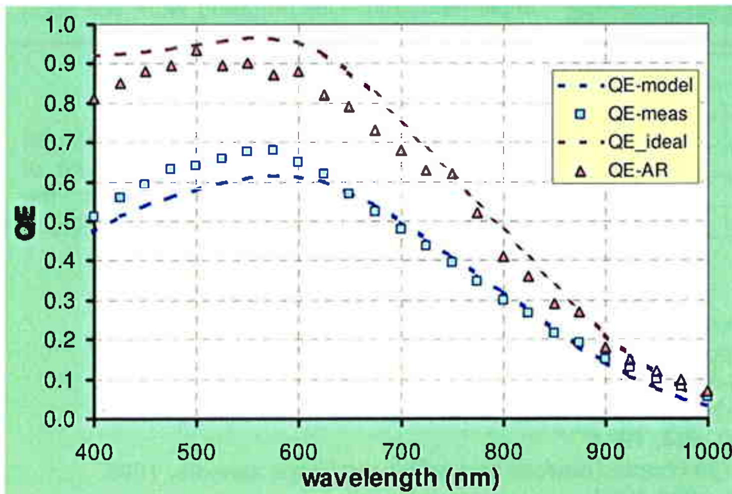

Figure 6: QE – measurement and model – w/ and w/o AR coating

While modulation transfer function (MTF) has not been measured yet, certain observations about the diffusion cross-talk between pixels can be made. Figure 7 shows that the modeled 1-D dopant concentration from the backside surface (origin) to the frontside nwell area. The p-substrate doping is ~ 1x10^7/μm^3, the epi-doping is 3x10^2/μm^3, and the n-well doping is ~ 6x10^4/μm^3.

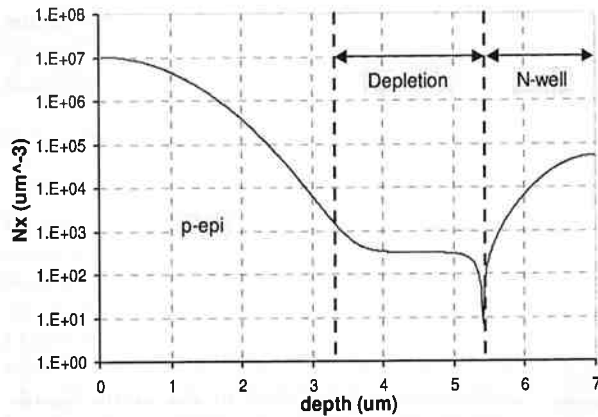

Figure 7: 1-D model of doping concentration variation from the backside surface to the front

As a result of high-temperature steps that a wafer undergoes during a typical CMOS fabrication process, an abrupt boundary between the p^+-substrate and the p-epitaxial region no longer exists. It can be seen from figure 7 that the doping concentration gradient extends as much as 4 μm into the epitaxial region from the backside. On the other hand, the depletion region between the n-well and the p-epitaxial region extends ~ 2 μm below the n-well junction. The presence of the depletion region and the doping gradient creates an electric field to drive the electrons from the backside to the collecting n-well junction. Therefore, the imager is be expected to provide low diffusion cross-talk even to photoelectrons created by short wavelength (blue) light.

For measuring noise, the megapixel imager was operated in CDS mode. Off-chip CDS was implemented by using a 4-point sampling method, where both reset and signal levels were acquired differentially. A low modal noise of ~ 8 electrons was measured at room temperature, both before and after thinning, with no noticeable degradation in the spatial distribution of noise.

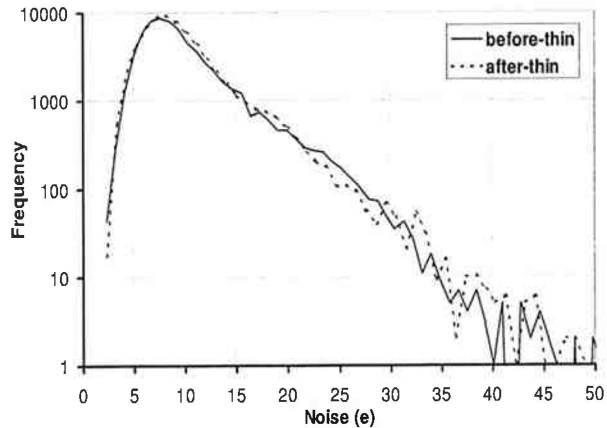

Figure 8: Measured noise histogram

Table 1 shows the summary of performance for the megapixel imager operated both under front- and back-illumination. It indicates that the backside thinning and back-illumination has expectedly increased the QE without introducing any unwanted performance degradation.

In conclusion, we have demonstrated a back-illuminated CMOS Imager with high QE by using a successful backside thinning and MBE-based surface passivation process. The main disadvantages of the thinning process are the absence of proper etch-stop required for accurate and reliable thinning, and the use of MBE for surface passivation, posing problems for wafer-level thinning and manufacturable back-illuminated imager implementation. Our on-going work will soon solve the twin problems.

Table 1: Performance comparison

Characteristics	Front-illum. (no thinning)	Back-illumination
Format	1024x1024	1024x1024
Pixel Pitch	8 μm	8 μm
QE @ 550 nm	25%	80%
Mean dark rate @ 296K	294 pA/cm^2	153 pA/cm^2
Modal read noise @ 2 MHz	7.6 e$^-$	8.2 e$^-$
PRNU @ 1/3 full-well	< 1.3%	< 1.3%
Signal handling capacity	170 ke$^-$	170 ke$^-$

Acknowledgments:

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