

A Low-Noise Signal Readout Circuit Using Double-Stage Noise Cancelling Architecture for CMOS Image Sensors

Nobuhiro Kawai[†], and Shoji Kawahito[‡]

[†]Graduate School of Electronic Science and Technology, Shizuoka University
3-5-1, Johoku, Hamamatsu, 432-8011 JAPAN

[‡]Research Institute of Electronics, Shizuoka University

E-mail: {nkawai, kawahito}@idl.rie.shizuoka.ac.jp

Abstract

This paper describes the effectiveness of a high-gain column double-stage noise canceller for CMOS image sensors. The signal path examined includes a pixel source follower, a noise-cancelling switched-capacitor (SC) amplifier, and two sample-and-hold circuits in each column. It is revealed that the total read noise consists of two major components of the SC amplifier. The analysis suggests that a very low-noise CMOS image sensor can be realized using the high-gain column double-stage noise-cancelling architecture. An experimental CMOS line sensor chip with the low-noise read circuits is implemented using $0.25\mu\text{m}$ CMOS technology. Very low-noise level of $34.2\ \mu\text{V}_{\text{rms}}$ is achieved. This corresponds to the equivalent number of noise electrons of less than 1.

I Introduction

One of the most important factors of CMOS image sensors is noise performance. Recently, very low-

noise CMOS image sensors have been reported [1,2]. The temporal read noise of the signal path of a CMOS image sensor including a pixel source follower, a column noise-cancelling switched-capacitor (SC) amplifier, and two sample-and-hold (S/H) capacitors has been analyzed by the authors [3], and it is shown that the high-gain double-stage noise canceller can reduce the read noise effectively. In this paper, we present results of an implemented experimental CMOS image sensor which has the column double-stage noise-cancelling architecture. As a result of the measurement, it is found that the input referred noise can be reduced to $34.2\ \mu\text{V}_{\text{rms}}$. The equivalent noise electron of smaller than 1 is obtained using a pixel device with high conversion gain. This result suggests the possibility of photon count imaging using CMOS image sensors which have the proposed double-stage noise-cancelling architecture without photo-electron multiplication.

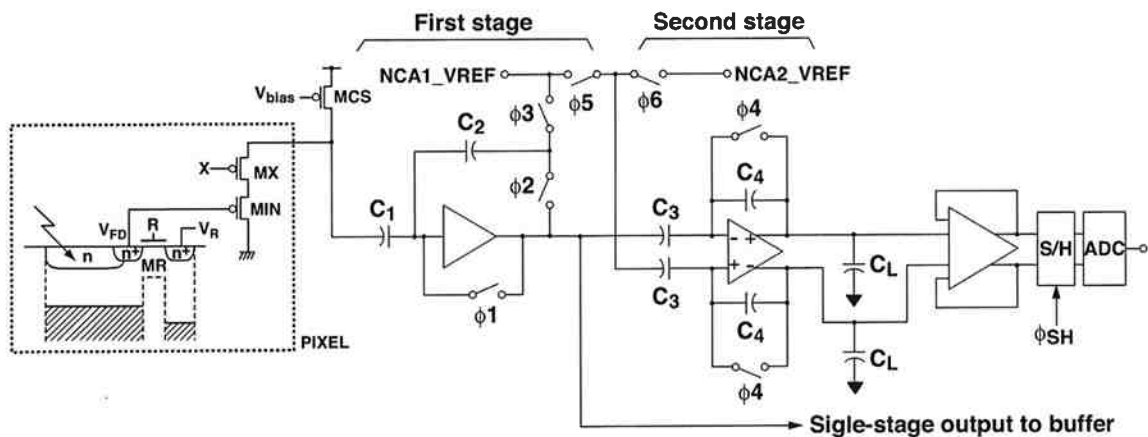


Fig. 1. Three-transistor APS and double-stage column noise canceller.

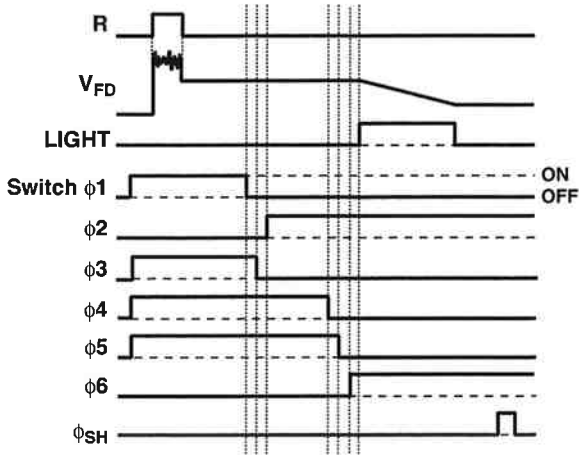


Fig. 2. Switching diagram for double-stage column noise canceller.

II Double-stage noise-cancelling architecture

Figure 1 shows the circuit diagram of the signal chain of the experimental CMOS image sensor. The timing diagram is shown in Fig. 2. In order to demonstrate the low-noise signal readout while using a standard 3 transistor active pixel circuit, a special sensor operation is used for reset noise cancelling. When the floating diffusion in the pixel is reset, both the first and the second SC amplifier stages are reset. Then, the first stage is prepared for the amplification by turning on the switch controlled by ϕ_2 . The second stage samples the output of the first stage by turning off the switch controlled by ϕ_4 . After that, the photo diode is illuminated, and the signal level appears at the second stage output.

III Noise analysis of the switched-capacitor amplifier

There are two major noise components in the first stage; the noise charge sampled at the charge summation node of the SC amplifier and transferred to the capacitor C_2 , and the direct noise component due to the source follower and the noise-cancelling amplifier sampled directly at the second stage. Our analysis shows that the direct noise components are closely related to the SC amplifier gain, and can be significantly reduced by using a large gain, suggesting the possibility of an extremely low-noise readout circuit using this double-stage noise-cancelling architecture.

Figure 3 shows the estimated input-referred noise of the first SC amplifier including the thermal and $1/f$ noise as a function of the gain of the first SC amplifier in [3]. In this figure, N_f , L and W of $\sqrt{N_fWL}$ are the flicker noise coefficient, the channel length

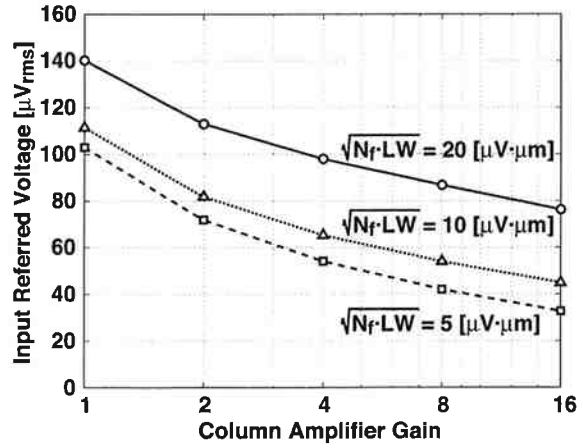


Fig. 3. Estimated input-referred noise voltage as a function of column amplifier gain.



Fig. 4. Photograph of the CMOS line image sensor.

and the channel width of MOSFETs. At a gain of 16, the total noise can be reduced to less than $40 \mu V_{rms}$ for $\sqrt{N_fWL} = 5 \mu V \mu m$.

IV Implementation and measurement of an experimental CMOS line image sensor

An experimental very low-noise CMOS line image sensor shown in Fig. 4 is designed and implemented

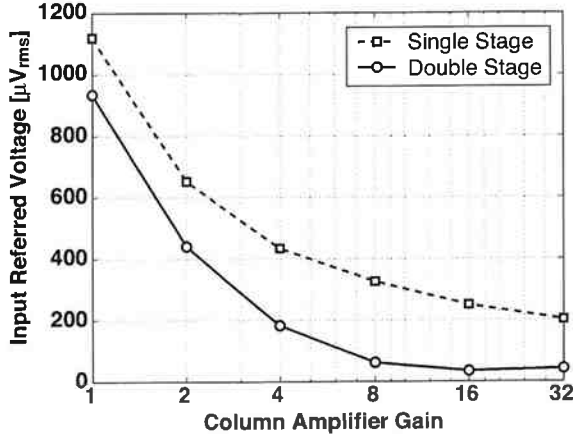


Fig. 5. Measured input-referred noise voltage as a function of column amplifier gain.

using $0.25\mu\text{m}$ CMOS image sensor process to investigate the noise reduction effect of the high-gain double-stage noise-cancelling architecture. Figure 5 shows the measured input-referred read noise voltage as a function of the column amplifier gain in the case of $C_3 = C_4$ in Fig. 1. Because the result of Fig. 5 includes the noise components of the sensor chip and the outside system, the noise level for small gain is much larger than the result of Fig. 3 which includes only from the pixel source follower to the first SC amplifier. The input-referred noise can be reduced to $34.2\mu\text{V}_{\text{rms}}$ using the high-gain double-stage noise-cancelling architecture at a gain of 16, while the single-stage noise canceller has the noise level of $250\mu\text{V}_{\text{rms}}$. Therefore, the double-stage noise-cancelling architecture can reduce the read noise to $1/7$ of the single-stage architecture.

The conversion gain of the pixel which has a low-capacitance floating diffusion is $77.0\mu\text{V}/e^-$ which is measured by the shot noise measurement. The measured input-referred noise in the design with this high conversion gain pixel is $48.5\mu\text{V}_{\text{rms}}$, hence the number of the equivalent noise electron is 0.63.

V Possibility of photon count imaging with a CMOS image sensor

The possibility of photon count imaging using a CMOS image sensor is investigated in this section using the results of above measurements.

The incoming number of photons is fluctuated, and this fluctuation follows Poisson distribution. The fluctuation is observed as photon shot noise. The probability density of Poisson distribution $p(x)$ is written as

$$p(x) = \frac{\mu^x}{x!} \exp\{-\mu\} \quad (1)$$

where μ is the average of the signal electrons. The

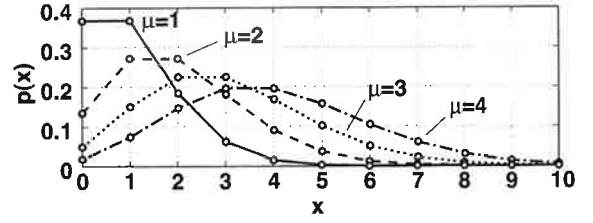


Fig. 6. Poisson distribution of photon shot noise.

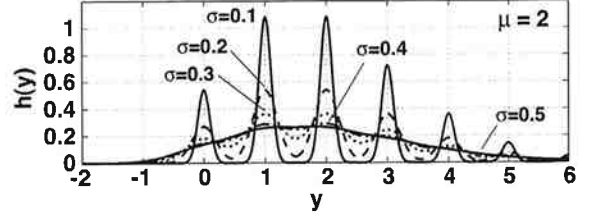


Fig. 7. Probability density when the circuit noise exists.

probability density for $\mu = 1, 2, 3$ and 4 is shown in Fig. 6. Ideally, the voltage of the image sensor output is discrete if there is no additional noise. However, if random read noise is superimposed, the probability density function in the case of $\mu = 2$ and $\sigma = 0.1$ to 0.5 becomes as shown in Fig. 7. It follows

$$h(y) = \sum_{x=0}^{\infty} \frac{\mu^x}{x!} \exp\{-\mu\} \frac{1}{\sqrt{2\pi}\sigma} \exp\left\{-\frac{(y-x)^2}{2\sigma^2}\right\}. \quad (2)$$

In the case of $\sigma = 0.1$, the discrete signal levels can be clearly discriminated each other, and photon counting becomes possible. However, for $\sigma = 0.5$, there is no signal peak and discrete signal levels can not be detected.

Discrimination of the signal from the circuit noise means the quantization by setting the threshold levels at the middle of the discrete signal levels. If the noise amplitude is small enough, the read noise is further reduced by the quantization [4]. Let assume the number of the detected electrons is i . Since the noise disturbs the exact counting of the number of electrons, it is miscounted to $i + 1$. The noise power due to this miscounting is given by

$$P = \Delta^2 \int_{-0.5\Delta}^{0.5\Delta} N(\varepsilon) d\varepsilon \quad (3)$$

where

$$N(\varepsilon) = \frac{1}{\sqrt{2\pi}\sigma_n} \exp\left\{-\frac{\varepsilon^2}{2\sigma_n^2}\right\}. \quad (4)$$

Δ is quantization step, and σ_n is the standard deviation of the circuit noise.

By adding up all the noise components due to miscounting to i , the noise power after quantization is given by

$$P_n = \sum_{j=-\infty}^{\infty} \int_{(r(j)-0.5)\Delta}^{(r(j)+0.5)\Delta} N(\varepsilon) r^2(j) \Delta^2 d\varepsilon \quad (5)$$

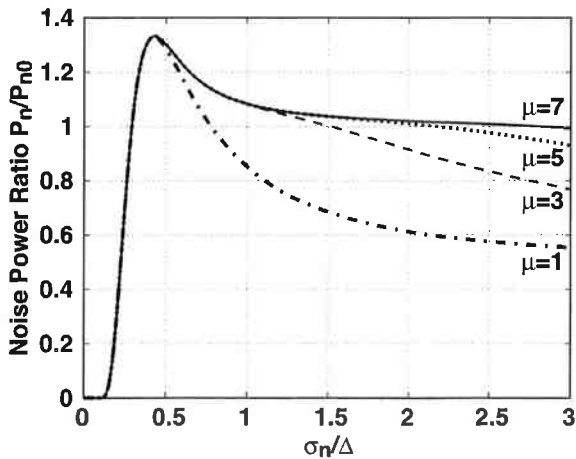


Fig. 8. Normalized noise power as a function of σ_n/Δ for $\mu = 1, 3, 5$ and 7 .

where

$$r(j) = \begin{cases} \mu & (j \leq 0) \\ |\mu - j| & (j > 0). \end{cases} \quad (6)$$

On the other hand, the noise power of the circuit, P_{n0} , before quantization is calculated as follows

$$\begin{aligned} P_{n0} &= \sigma_n^2 \int_{-\infty}^{\infty} N(\varepsilon) d\varepsilon \\ &= \sigma_n^2. \end{aligned} \quad (7)$$

Figure 8 shows the noise power after quantization normalized by P_{n0} as a function of σ_n/Δ , which means the equivalent noise electron number. In this calculation, the number of signal electrons is assumed to be positive or zero. Hence, the normalized noise power approaches 0.5 for $\sigma_n \gg 1$. On the other hand, from Fig. 8, it is found that the signal detection without the influence of read noise is possible if the read noise is less than 0.1 electrons.

Figure 9 shows the probability densities for the case that the signal electron number is 2 and the noises are 0.3 and 0.63. If the read noise is reduced to 0.3 electrons, the signal peaks can be clearly seen. However, from Fig. 8, the quantization do not have noise reduction effect in the noise level of 0.3 electrons. On the other hand, in the case of the noise is 0.63 electrons, which is measured a value, the signal peaks disappear.

Though the realization of the photon counting in CMOS image sensors is not realistic at the moment, it will be realized in the near future by the development of a higher conversion gain pixel and a further low-noise readout technology.

VI Conclusion

This paper presented the high-gain column double-stage noise-cancelling circuit and its analysis and

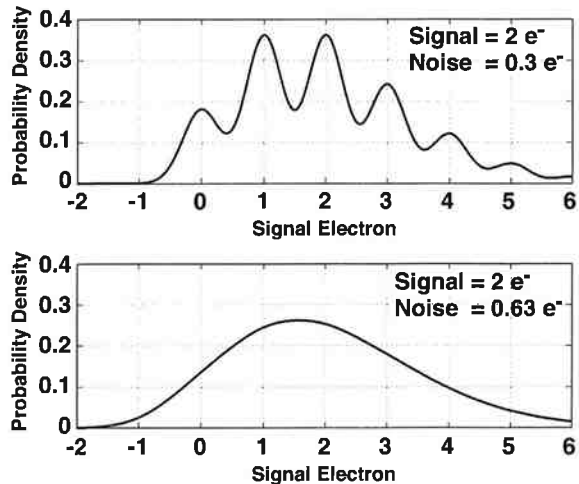


Fig. 9. Poisson distribution with circuit noise.

measurement. It was confirmed that the effectiveness of proposed double-stage architecture by the measurement of an experimental CMOS line sensor chip. The double-stage noise canceller has 1/7 of the read noise of the single-stage architecture. A possibility of photon count imaging in CMOS technology is discussed.

Acknowledgment

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