R7 Pixel-Pixel Fixed Pattern Noise in CMOS Image Sensors due to Readout Parasitic Capacitance

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ABSTRACT

It is demonstrated that parasitic capacitance between the CDS sampling capacitors in the column circuits of CMOS imagers give rise to image pixel-pixel fixed pattern noise and crosstalk due to source follower Vt distributions. An improved CDS sampling timing is proposed to eliminate the problem.

I. INTRODUCTION

CMOS image sensors achieve very low levels of pixel-pixel fixed pattern noise (PPFPN) by a technique commonly referred to as *Correlated Double Sampling* (CDS). In its most general sense, CDS is applied to remove both kTC noise and pixel offsets from active pixel arrays. However, for most 3T pixel arrays operated in a "read-first, reset-later" mode, the function is only to remove pixel offsets. 4T pinned photodiode pixels are able to operate in a "reset-first, read-later" mode and cancel both pixel offsets and kTC noise. In this paper, we demonstrate a source of residual error after the elimination of pixel offsets by CDS due to parasitic capacitances in the column readout circuits and propose an improved CDS timing.

Variations in the threshold voltage of each pixel source follower transistor would be seen directly in the output image if no measures were taken to avoid this non-uniformity. Threshold variations of several 100's of millivolts peak-to-peak are commonly found due to the small size of the pixel MOS transistor required for high fill-factor [1]. CDS eliminates these offsets by sampling the pixel output, once after light integration and then again after reset and subtracting the two sampled voltages. Sampling is performed on parallel grounded capacitors in each column and subtraction is achieved via a difference amplifier. This structure is commonly found in "crowbar" analogue readouts or in column parallel analogue to digital converters [2-4]. Another technique uses only one capacitor in series to perform both sampling and subtraction [5-7]. The analysis in this paper applies only to the former case.

II. ANALYSIS

Consider the circuit in Fig. 1 where there is a small parasitic capacitance C_p between the two identical capacitor top plates, C_{blk} and C_{sig}, with value C_s. This parasitic is difficult to avoid in practice unless special shielding precautions are taken, especially given the confined space available in columns matched to small pixel dimensions.
Let voltages on the two capacitors before sampling be related to the voltages from reading the previous image line:

$$V_{blk}(t0) = VR(i, j-1) \quad (1)$$

$$V_{sig}(t0) = VS(i, j-1) \quad (2)$$

where VR(i,j) is the reset voltage and VS(i,j) is the integrated light signal voltage of pixel at coordinate (i,j).
$V_{blk}(t0)$ and $V_{sig}(t0)$ are the voltages on capacitors C_{blk} and C_{sig} at time t0 (Fig. 2).
For 3T active pixels, the signal sample is taken first at time t1.

$$V_{blk}(t1) = VR(i, j-1) + \frac{C_p}{C_s} \times (VS(i, j) - VS(i, j-1)) \quad (3)$$

$$V_{sig}(t1) = VS(i, j) \quad (4)$$

At time t2 the reset sample is taken:

$$V_{blk}(t2) = VR(i, j)) \quad (5)$$

$$V_{sig}(t2) = VS(i, j) + \frac{C_p}{C_s} \times (VRi, j) - V_{blk}(t1)) \quad (6)$$

which for $C_p << C_s$ is approximately:

$$V_{sig}(t2) = VS(i, j) + \frac{C_p}{C_s} \times (VR(i, j) - VR(i, j-1)) \quad (7)$$

The result is differenced to produce the output voltage as:

$$V_{diff} = V_{blk}(t2) - V_{sig}(t2) \quad (8)$$

$$V_{diff} = (VR(i,j) - VS(i,j)) \quad (9)$$
$$-\frac{C_p}{C_s} \times (VR(i,j) - VR(i,j-1))$$

Note that the terms VR(i,j-1) and VR(i,j) contain uncorrelated source follower threshold variations. Thus a PPFPN of RMS amplitude Cp/Cs x sqrt(2) x σ(Vtn) would be expected in the image.
In a "crowbar" readout the initial voltages are

$$V_{blk}(t0) = (VR(i,j-1) + VS(i,j-1))/2 \quad (10)$$

$$V_{sig}(t0) = (VR(i,j-1) + VS(i,j-1))/2 \quad (11)$$

$$V_{diff} = (VR(i,j) - VS(i,j)) \quad (12)$$
$$-\frac{C_p}{C_s} \times VRi,j - VRi,j-1 + VSi,j-1/2$$

causing an additional problem of signal crosstalk between successive video lines.
In 4T pinned-photodiode pixels the sequence of sampling reset and signal voltages is reversed and the result is

$$V_{diff} = (VR(i,j) - VS(i,j)) \quad (13)$$
$$-\frac{C_p}{C_s} \times (VS(i,j) - VS(i,j-1))$$

This represents both PPFPN and signal crosstalk.

III. PARASITIC INSENSITIVE CDS TIMING

A timing is shown in Fig. 3 which can alleviate the problem [8]. During the first sample, both capacitors are precharged to the pixel voltage.

$$V_{blk}(t1) = VR(i,j) \quad (14)$$

$$V_{sig}(t1) = VS(i,j) \quad (15)$$

At time t2 the following result is now obtained:

$$V_{blk}(t2) = VR(i,j)$$

$$V_{sig}(t2) = VS(i,j) - \frac{C_p}{C_s} \times (VS(i,j) - VR(i,j)) \quad (16)$$

giving

$$V_{diff} = \frac{(C_p + C_s)}{C_s} \times (VR(i,j) - VS(i,j)) \quad (17)$$

This timing causes the voltage step across the parasitic capacitance to be proportional to the pixel signal and thus the error voltage caused during the second sampling interval is transformed into a gain error. If C_p has a low variability from column to column then the effect appears as a very slight increase in readout sensitivity.

This analysis can be further generalised to the case of a parasitic capacitance between neighbouring columns (Fig. 4) In this case we have an additional term due to the column to column parasitic capacitance C_{pp} which will tend to increase the level of PPFPN still further as well as introduce column to column signal crosstalk.

IV. MEASURED RESULTS

Fig. 5 shows the achieved improvement due to this timing mode in a 0.35μm SXGA sensor. 256 frames were averaged to sufficiently attenuate the temporal noise and vertical FPN has been learnt and subtracted by post processing. The RMS image PPFPN with conventional CDS timing is 750μV RMS commensurate with Cp=4.5fF and Cs=500fF, σ(Vtn)=40mV. The image sigma is reduced to 130μV RMS by applying the proposed CDS timing. This level is expected from reduction of kT/C reset noise by averaging 256 frames.

V. CONCLUSIONS

Pixel-pixel fixed pattern noise due to pixel source follower Vtn distributions can be removed by applying an improved CDS timing.

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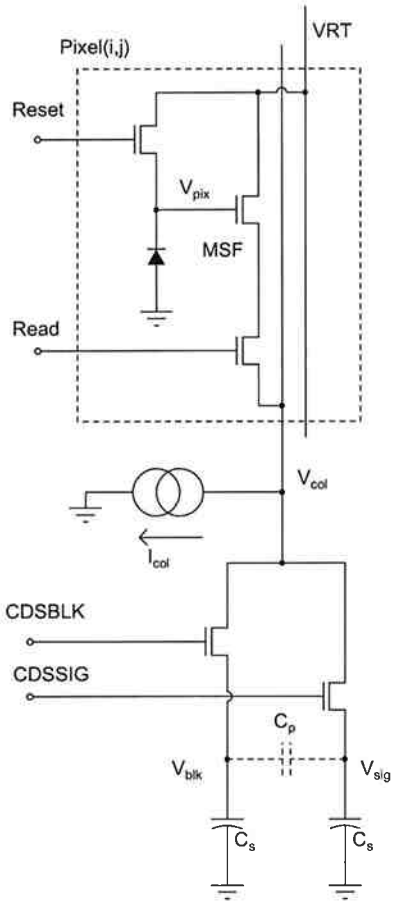

Figure 1. Single 3T pixel with CDS capacitors and parasitic capacitance

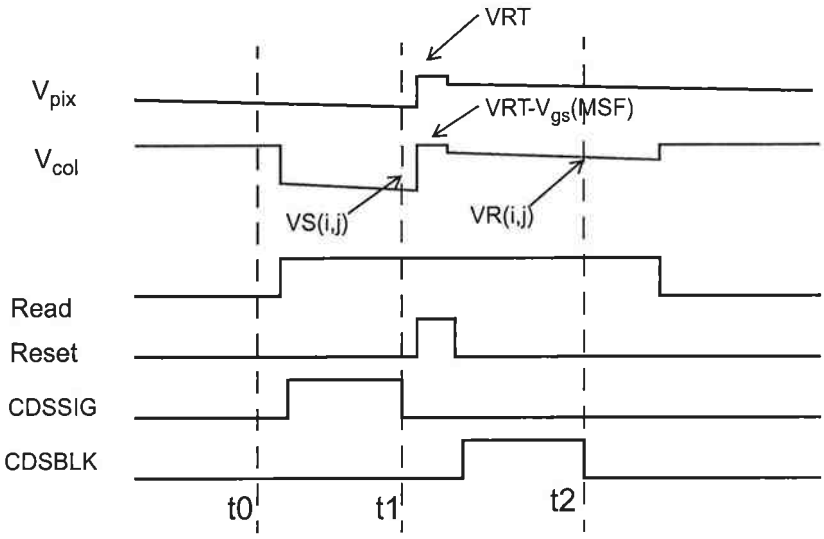

Figure 2. Timing of 3T pixel showing CDS sampling instants

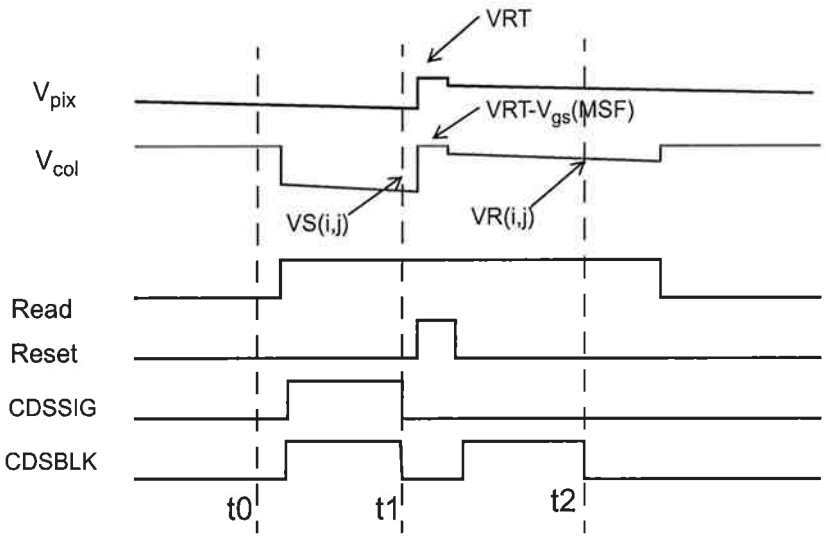

Figure 3. Proposed low-PPFPN CDS timing

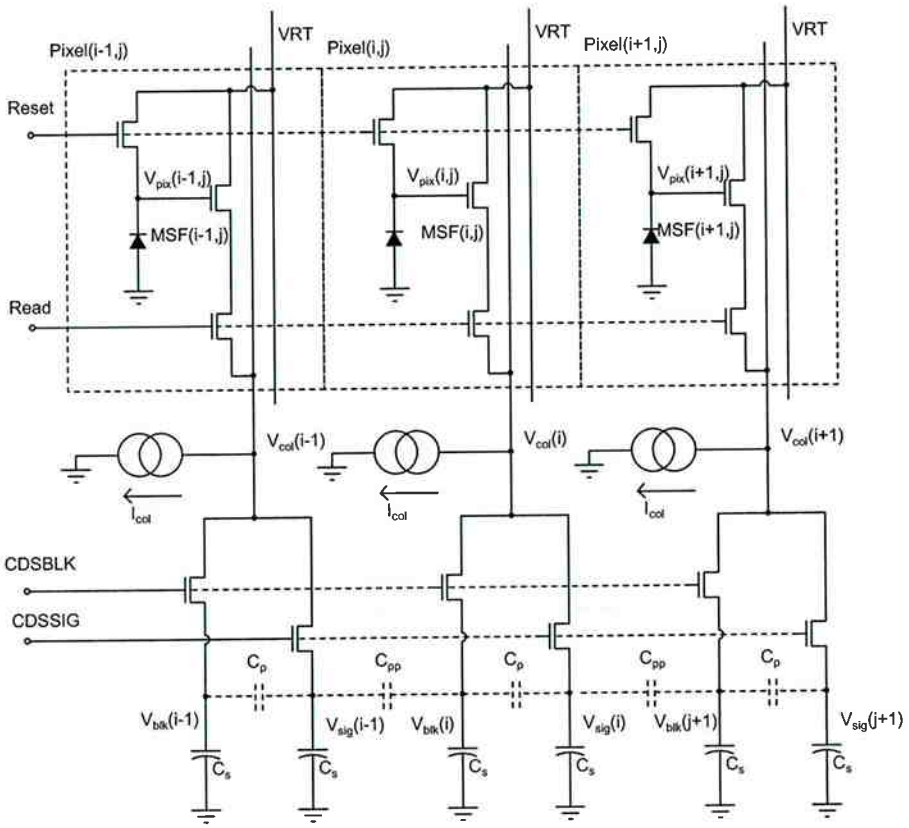

Figure 4. General case of multiple columns showing parasitic capacitances

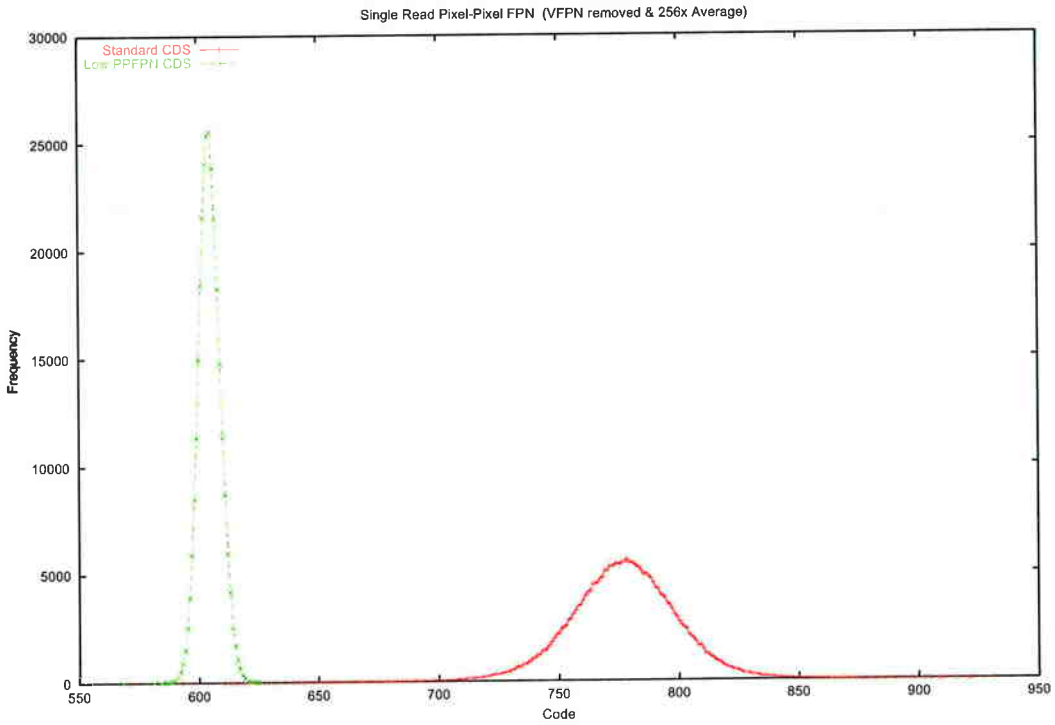

Figure 5. Image histograms of an 0.35µm SXGA sensor with standard CDS timing (+) and low-PPFN timing (x). Vertical FPN has been removed and 256 frames have been averaged toattenuate temporal noise.