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Accurate Simulation and Modeling of Reset Noise in 3T CMOS Active Pixels

T. Lulé, R. Henderson*, L. Simony†, F. Mütze, S. Benthien, M. Sommer

ST Microelectronics, Imaging Division, 12 rue Jules Horowitz – B.P. 217, F-38109 Grenoble Cedex
Tel: +33 4 76 58 59 35, Tarek.Lule@st.com

*Univ. of Edinburgh, Inst. of Micro and Nano Systems, West Mains Road, Edinburgh EH9 3JF, UK,

†ST Microelectronics, Central R&D, 850 rue Jean Monnet, F-38926 Crolles Cedex

Abstract – kTC noise of pixel reset operation is investigated in more details using the 3T type pixel as example. While in some cases the noise power is given by classical kT/C, in many others, a more complex formula needs to be applied that takes into account the bandwidth of the reset noise with respect to the bandwidth of the source follower driver.

I. Introduction

CMOS image sensors have come a long way from their early trials to today's high performance levels, most notably regarding pixel noise levels [1]. While very early the kTC noise of pixel reset operation was identified as a major noise source, introduction of the photo gate [2] or pinned photodiode [3] structures in conjunction with true correlated double sampling (CDS) proved effective in virtually eliminating this noise source, rendering its further investigation uninteresting for many applications. Still, a number of groups work on methods to reduce kTC noise [4, 5] while others develop CMOS type image sensors for applications where true CDS is not possible [6] or impracticable [7].

II. Standard Case kTC Noise

In the past, kTC noise, wherever it was not removed by one of the abovementioned means, has been accepted as a fundamental source of noise with a given formula (in voltage) in the case of hard reset of

$$u_n = \sqrt{\frac{kT}{C_{int}}} \qquad (1)$$

For soft reset operation, a reduction effect of reset noise with respect this formula has been repetitively reported and different explanations given (see e.g. [8]). However, for hard reset mode, deviations from this formula have been observed frequently but have been skipped over by vague explanations or ignored completely. In order to better understand the source and nature of the kTC noise, analytical formulation and simulation based on ELDO were employed together to arrive at a more general approach and formulas for the input floating diffusion capacitance and related kTC noise.

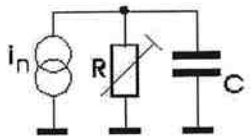

Figure 1, Configuration where kTC Noise Formula Applies

Figure 1 shows the standard sample configurations for true kTC noise, a "reset" resistance between a DC source and a capacitor as for a 3T type pixel. The thermal noise voltage density of the resistance

$$du_n^2 = 4kT \cdot R \cdot df \qquad (2)$$

integrated over the spectrum leads, due to the introduction of the pole formed by R and the capacitors,

$$\omega_p = \frac{1}{C \cdot R} \qquad \int_0^{\infty} \frac{1}{1 + \frac{\omega^2}{\omega_p^2}} df = \frac{\omega_p}{4} \qquad (3)$$

to an elimination of R and thus to the above kTC formula. Thus the kTC noise voltage after switching off is given by the capacitance only that is seen by the resistance, while the total noise energy is independent of all resistance and capacitances:

$$E_{n\_tot} = \frac{1}{2} \cdot U^2 \cdot C = \frac{kT}{2} \qquad (4)$$

Already more complex, Figure 2 shows the principle schematic of a 3T source follower pixel to be investigated furthermore, including some coupling capacitances between the input and the output of the source follower driver, a large part of which stems from C_{gs_drv} the gate to source overlap and the most of the gate to channel capacitance of the driver itself.

III. KTC NOISE IN SOURCE FOLLOWER PIXEL

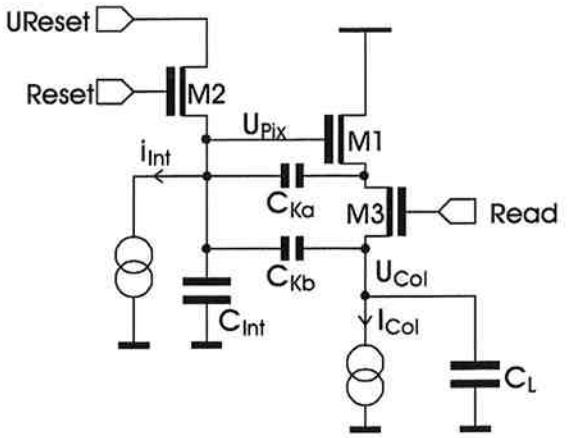

Figure 2, Schematic of 3T Type Pixel with Important Coupling Capacitances

Figure 3 shows the AC equivalent circuit, where the resistance of the read switch has been neglected, the reset is represented by gds and a noise source i_{nth} and the coupling capacitances C_{Ka} and C_{Kb} have been lumped into C2. It is assumed here that the read switch is on and thus the source follower is operational during the reset operation.

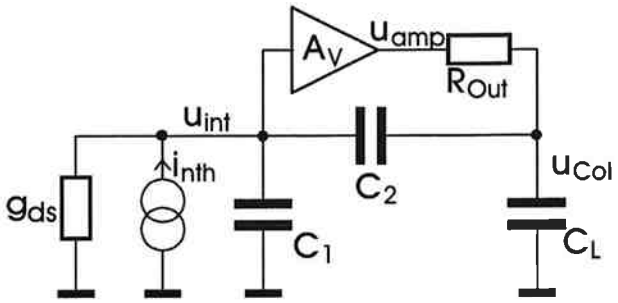

Figure 3, AC Equivalent Circuit of Figure 2

Solving the equation for input voltage generated by i_{nth} with the reset off (gds = ∝) yields a frequency dependent expression with a zero and two poles, of which one represents the integrating property of a purely capacitive input:

$$v_{int} = \frac{i_{nth}}{s\cdot\left[C_1 + C_2\cdot(1 - A_v)\right]} \cdot \frac{s\cdot(C_2 + C_L)\cdot R_{out} + 1}{1 + s\cdot R_{out}\cdot\left[\frac{C_1\cdot C_2 + C_1\cdot C_L + C_2\cdot C_L}{C_1 + C_2\cdot(1 - A_v)}\right]} \qquad (5)$$

wherein the open loop output resistance and gain of the source follower have been inserted as

$$R_{out} = \frac{1}{g_{m1} + g_{mb1} + g_{ds1} + g_{icol}} \qquad A_V = g_{m1}\cdot R_{out} \qquad (6)$$

For very small and very large frequencies the formula becomes:

$$s << \frac{1}{C_L\cdot R_{out}} : v_{int} = \frac{i_{nth}}{s\cdot\left[C_1 + C_2\cdot(1 - A_v)\right]} \qquad (7)$$

$$s >> \frac{1}{C_L\cdot R_{out}} : v_{int} = \frac{i_{nth}}{s}\cdot\frac{1}{C_1 + \frac{C_2\cdot C_L}{C_2 + C_L}} \qquad (8)$$

In both cases the current source sees a purely capacitive input, whereby the effect of C_2 is attenuated by A_v for low frequencies whereas for high frequencies the source follower becomes ineffective and C_2 appears in series with C_L.

For comparison all parasitic capacitances of a 3um 3T pixel designed in 0.18um technology were extracted and an AC simulation performed with the reset switch off. To bias the floating diffusion, a resistance of 1POhm was put between U_{Reset} and U_{Int} (large enough to shift its pole with C_{int} to below 1Hz) while an AC source was put between input and ground. From the transistor parameters in the ELDO output file and the parasitic capacitance netlist, the following values were calculated for the parameters used above:

$$\begin{aligned} &C_1 = 3.63\text{fF} \quad C_2 = 3.75\text{fF} \quad C_L = 1.50\text{pF} \\ &A_v = 0.73 \quad R_o = 31.09\text{k}\Omega \quad R_{reset} = 78.13\text{k}\Omega \end{aligned} \qquad (9)$$

from which the LF and HF input capacitance and the pole and zero should be:

$$\begin{aligned} &C_1 + (1 - A_v)\cdot C_2 = 4.65\text{fF} \qquad \frac{1}{2\cdot\pi\cdot R_o\cdot C_L} = 3.42\text{MHz} \\ &C_1 + \frac{C_2\cdot C_L}{C_2 + C_L} = 7.36\text{fF} \qquad \frac{C_1 + (1 - A_v)\cdot C_2}{2\cdot\pi\cdot R_o\cdot C_L\cdot(C_1 + C_2)} = 2.16\text{MHz} \end{aligned} \qquad (10)$$

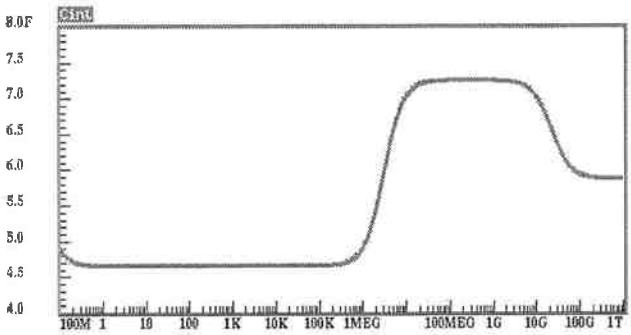

Figure 4, Input Capacitance versus Frequency of Figure 2

The input referred capacitance over the frequency was extracted and plotted in Figure 4 by inserting the voltage magnitude from the AC simulation in the following calculation:

$$C(f) = \frac{|i_{int}|}{2\cdot\pi\cdot f\cdot|v_{int}(f)|} \qquad (11)$$

The capacitance curve shows the zero and pole around 3MHz in accordance to the calculations. At lower frequencies the input capacitance is reduced to 4.651fF matching the above result, while at higher frequencies C_2 adds fully to C_1 (keeping in mind that $C_L >> C_2$) to make a total of 7.25fF. The absolute values from the simulation and from hand calculation match to within a few percent for the low to mid frequency range. At 20GHz the capacitance rolls off to a reduced value. This additional pole/zero pair is introduced by the read transistor which separates part of the coupling capacitances C_{Ka} of Figure 2 from the large grounding capacitance C_L at the output thereby reducing the effective value for C_2 to C_{Kb} only. From this analysis already the simple application of the traditional kTC noise formula to a case where the capacitance is so strongly frequency dependent becomes insufficient.

Next we look at the same circuit with reset on. The voltage created by any input current is described by the following formula in the s domain with two poles and a zero, again neglecting the read switch resistance (see (18) below)

After some calculations it can be shown that for small R_{res}, the input impedance can be approximated by a single pole at

$$f_p = \frac{1}{2\cdot\pi\cdot R_{res}\cdot(C_1 + C_2)} = 276\text{MHz} \qquad (12)$$

with the example value of the Reset resistance as given in equations (9). This pole is essentially dominated by the high frequency capacitance $C_1 + C_2$ because the noise at the input has a high bandwidth. For confirmation, the pixel is simulated with reset on and the same AC current source at the input, to yield a pole at 262 MHz, noticeably deviating from the calculations. The cause can be found in an additional input capacitance due to the reset switch being turned on strongly of

$$\delta C_{ddRes} = 0.414\text{fF} \qquad (13)$$

which can become a considerable extra portion of the total input capacitance. Looking at only the thermal noise voltage density generated by the reset transistor extracted from simulations, the pole is found at 264 MHz as well. However, the simulated amplitude (of the reset transistor thermal noise only) is in discrepancy to traditional calculations of

calculation $$v_{nReset} = \sqrt{4kT\cdot R_{reset}} = 29\frac{nV}{\sqrt{Hz}} \qquad (14)$$

simulation $$v_{thResSim} = 42.9\frac{nV}{\sqrt{Hz}} \qquad (15)$$

Thus, according to the model of this 0.18um technology NMOS, its thermal noise at strong inversion is 20% higher than standard calculation would indicate, while it becomes comparable under weak inversion. This increase in thermal noise needs to be integrated over all frequencies to provide the value for the kTC noise. Thus the increased thermal noise produces an increased kTC noise after reset is switched off.

Using an empirical number of $\rho_{th} = 1.2$ for the increased thermal noise contribution, we have in total a noise voltage formula on the input while reset is on of:

$$v_{totkTC} = \rho_{th}\cdot\sqrt{\frac{kT}{C_1 + C_2 + \delta C_{ddRes}}} = 872\mu V \qquad (16)$$

The same can be done by numerically integrating the spectrum that was generated by the simulator. This yields a well matching value of 881uV, which is only slightly below the calculated one. This confirms that the AC model given in Figure 3 is sufficiently close the much more detailed AC model employed by a SPICE based simulator, not at least since the pole of the reset switch with the input capacitance is still below the pole given by the read switch resistance that was neglected in the above calculations.

This confirms that the kTC noise voltage can actually be simulated by AC simulation, except for the last step that is to follow: When the reset switch is released, the noise charge on the increased input capacitance that can be calculated from above formula is redistributed to the reduced input capacitance as given above to yield an even larger kTC noise voltage of:

$$v_{kTCeff} = \rho_{th}\cdot\frac{\sqrt{kT\cdot(C_1 + C_2 + \delta C_{ddRes})}}{C_1 + (1 - A_v)\cdot C_2} = \rho_{th}\cdot\sqrt{\frac{kT}{C_{int}}\cdot\left(1 + \frac{A_v\cdot C_2}{C_{int}} + \frac{\delta C_{ddRes}}{C_{int}}\right)} \qquad (17)$$

With the numbers given above we find a total kTC noise at the input of

new $$v_{in\_kTC} = 1.459\text{mV}$$

traditional $$\sqrt{\frac{kT}{C_{int\_eff}}} = 0.943\text{mV}$$

This increased kTC noise is due to the three contributions discussed above as can be seen in formula 17: the extra contribution of C_2 for high frequencies, the additional capacitance of the reset transistor while it is turned on and finally the increased thermal noise voltage of the reset transistor while it is on. The whole procedure of determining the various capacitances versus frequency in the different operating modes (Reset

ON and OFF) as well as the other parameters needed above and calculating the kTC noise with the above formula was applied to a range of different test pixels with different input capacitances.

IV. Measurements

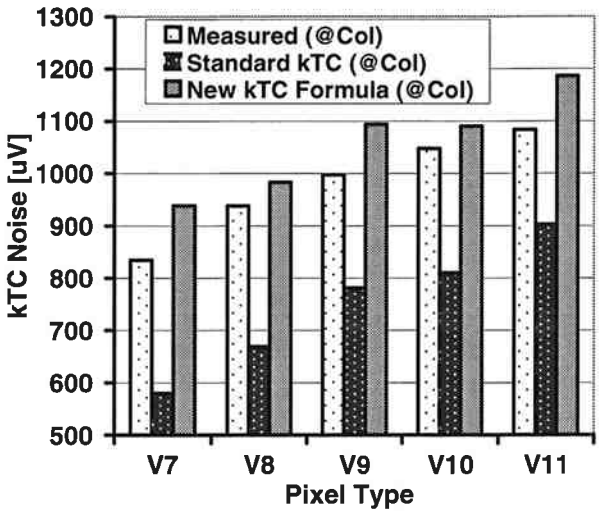

Figure 5, kTC Noise Measurements versus Standard and New Formula for Different Pixels

The calculated kTC noise results from the standard and the new formulas are compared in Figure 5 with actual measured kTC noise from manufactured parts, in all cases referring the noise to the column line. It was found that measurement results are now 5-10% below the calculated values as opposed to 50% above the traditional calculations. In the case of the sample pixel used for above calculations, a single kTC noise of 940 μV was measured on the column line, whereas the standard kT/C formula, using the C from the photon shot noise based conversion gain measurements, gives 680 μV and the formula 1060 μV.

The overestimation might be due to the inaccuracy to determine the actual capacitances from extraction or from the charge conversion gain measurements. Another explanation could be the fact that some of the increased kTC noise is relaxed during the transition of the reset transistor through the weak inversion region. Then, the thermal noise factor is reduced and also the input capacitance is reduced once the pole of the reset transistor with the input capacitances comes in the region of the pole of the amplifier. This relaxation effect can occur if the read transistor is on during the reset, while it cannot happen with read off.

V. Conclusion

Overall an improved formula for kTC noise was found that includes the three largest contributors to increased kTC noise that are needed to match measurements better with calculations without adding too much extra complexity to the result, by performing appropriate approximations in the underlying calculations.

$$v_{int}(s) = \frac{i_{nth}(s)\cdot R_{res}\cdot\left[1 + s\cdot(C_2 + C_L)\cdot R_{Out}\right]}{1 + s\cdot R_{res}\cdot(C_1 + C_2 - C_2\cdot A_v) + s\cdot R_{Out}\cdot(C_2 + C_L) + s^2\cdot(C_1\cdot C_2 + C_1\cdot C_L + C_2\cdot C_L)\cdot R_{Out}\cdot R_{res}} \quad (18)$$

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