A low power single chip VGA camera

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A flexible single chip VGA camera function was designed using APS pixel technology in a dedicated 0.28 um Philips CMOS process (1P/4M). The chip is designed targeting the cellular phone market for which key parameters are size, cost and performance. Table 1 summarizes some device reference data.
The chip offers an 8-bit parallel YUV/RGB output stream up to VGA resolution formats. Sub-VGA resolutions are supported by means of down-scaling and/or Region Of Interest (ROI) selection.
The video stream is conditioned via an on-chip micro-controller that performs the auto-loop (AWB, AE) calculations and device control. Besides this it supports a high level camera interface to ease the device application.
A fully programmable frame-format allows it to handle a wide range of input frequencies up to 15 MHz for 15 FPS. Synchronisation codes as defined in the CCIR656 standard can optionally be merged into the video stream. The chip is programmable via a standard I2C interface.
Some other supported hardware features are, a.o.: hor./vert. mirroring, white-blemish and shading correction.
The device architecture is depicted in figure 1. The VGA pixel array is using, a three transistor pixel cell, an RGB-Bayer color filter pattern and micro-lenses. The main pixel performance characteristics are summarised in table 2.
The pixel array output signal is corrected for Fixed Pattern Noise (FPN) by means of a Correlated Double Sampling (CDS) circuit. The succeeding signal processing chain is separated into a raw RGB processing part, were the sequential raw RGB data is processed, a Camera Signal Processing (CSP) block, were the RGB data is processed in parallel an output scaler were the resolution scaling is performed and an output formatter which converts the processed video stream to the desired output format.
To match the CDS output signal with the input range of the Analog to Digital Converter an Analog Programmable Gain Amplifier (APGA) can optionally be activated. In APGA bypass mode the CDS output signal is directly quantised and the power consumption of the APGA is saved. The high performance 12-bit ADC allows it to perform signal gaining in the digital domain (DPGA) without sacrificing signal to noise performance. The ADC is build using a pipeline architecture with 1.5 bit resolution per stage.
Behind the digital gain stage the raw video signal can be corrected for white defects by means of an on-the-fly Defect Pixel Correction (DPC) algorithm. The succeeding shading correction circuit enables it to correct for optical shading.
The corrected raw RGB data stream is successively applied to the Camera Signal Processing core which converts the sequential pixel data to a parallel YUV444 data stream.
The processing steps successively passed for this conversion are : color interpolation, matrix color correction, white-balance, gamma-correction and RGB2YUV-conversion. Parallel to the conversion a contour signal is generated and finally merged into the luma (Y) signal.
The CSP is equipped with a measurement engine that performs measurements in the different color domains and luminance domain. The measurement results are input for the embedded micro-controller to control the device auto loops.
The scaler behind the CSP performs the resolution scaling and region of interest selection. QVGA, QQGVGA and sub-QCIF output streams are supported maintaining the Field Of View. Down-sampling ratio's up to five times are supported
The output formatter converts the processed YUV 444 signal to the desired RGB or YUV output format. For an RGB output stream the YUV data is converted back to the RGB domain. A noise shaper is included to mask the data truncation of the differrent supported RGB output formats (565, 555 and 444).
For a YUV422 output format, the YUV 444 data is bandwidth limited, in advance of data sample decimation, to suppress possible alliasing effects. Besides the signal formatting also resolution scaling, ROI selection, data clipping and merging of CCIR656 synchronisation codes are handled by the output formatter.
The embedded 80C51 micro-controller performs the auto-loop calculations and device function control. Each frame-time the micro-controller is triggered to capture the measurement data of the previous frame and to perform the calculations. As a result the different controls are tuned to achieve a stable signal quality under varying ambient conditions. Figure 2 depicts a sample picture taken with the device.

References:

1. J.Hurwitz et al., "A Miniature Imaging Module For Mobile Applications," ISSCC Digest of Technical Papers, February 2001.
2. H. Tian, B. Fowler, and A. El Gamal, Analysis of Temporal Noise in CMOS Photodiode Active Pixel Sensor, In *IEEE Journal of Solid State Circuits*, Vol.36, No.1, Pages 92-101, January 2001.
3. A. Abo, P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter" *IEEE J. Solid-State Circuits*, vol. 34, no. 5, May 1999.

Table 1: Device reference data

Parameter	
Technology	0.28 micron 1P/4M
Image resolution	640 x 480 (VGA)
Output format	8-bit parallel YUV / RGB
Supply voltage	2.8 volt +- 0.2 V
Power consumption	
- 15fps YUV	55 mW
- power down	4 µW
Input clock	12 MHz
Frame-rate	15 fps
ADC resolution	12 bit
Signal to Noise ratio	40 dB@ 50 lux, 15 fps
F2.5	
Control Interface	I^2C
Chip dimensions	4.85 x 5.4 mm^2

Table 2: Pixel characteristics (T_{int} = 1/30 sec, T_{colour} = 3200 K)

Parameter	Conditions	Typ	Unit
Pixel size		5.0 x 5.0	μm^2
Output saturation voltage	At analog sensor output, Gain = 0dB	1100	mV
Conversion Gain	At analog sensor output, Gain = 0dB	52	µV/e-
Photodiode dark current	T_{amb} = 25 °C	0.1	nA/cm^2
	T_{amb} = 60 °C	1.6	nA/cm^2
Fixed pattern noise	T_{amb} = 25 °C	0.3	mV_{rms}
	T_{amb} = 60 °C	2.4	mV_{rms}
Random noise	T_{amb} = 25 °C	1.7	mV_{rms}
Dynamic Range	T_{amb} = 25 °C	56	dB
Sensitivity	Gain = 0 dB		
- red	IR cut-off @ 650 nm	70	mV/lx
- green		67	mV/lx
- blue		44	mV/lx

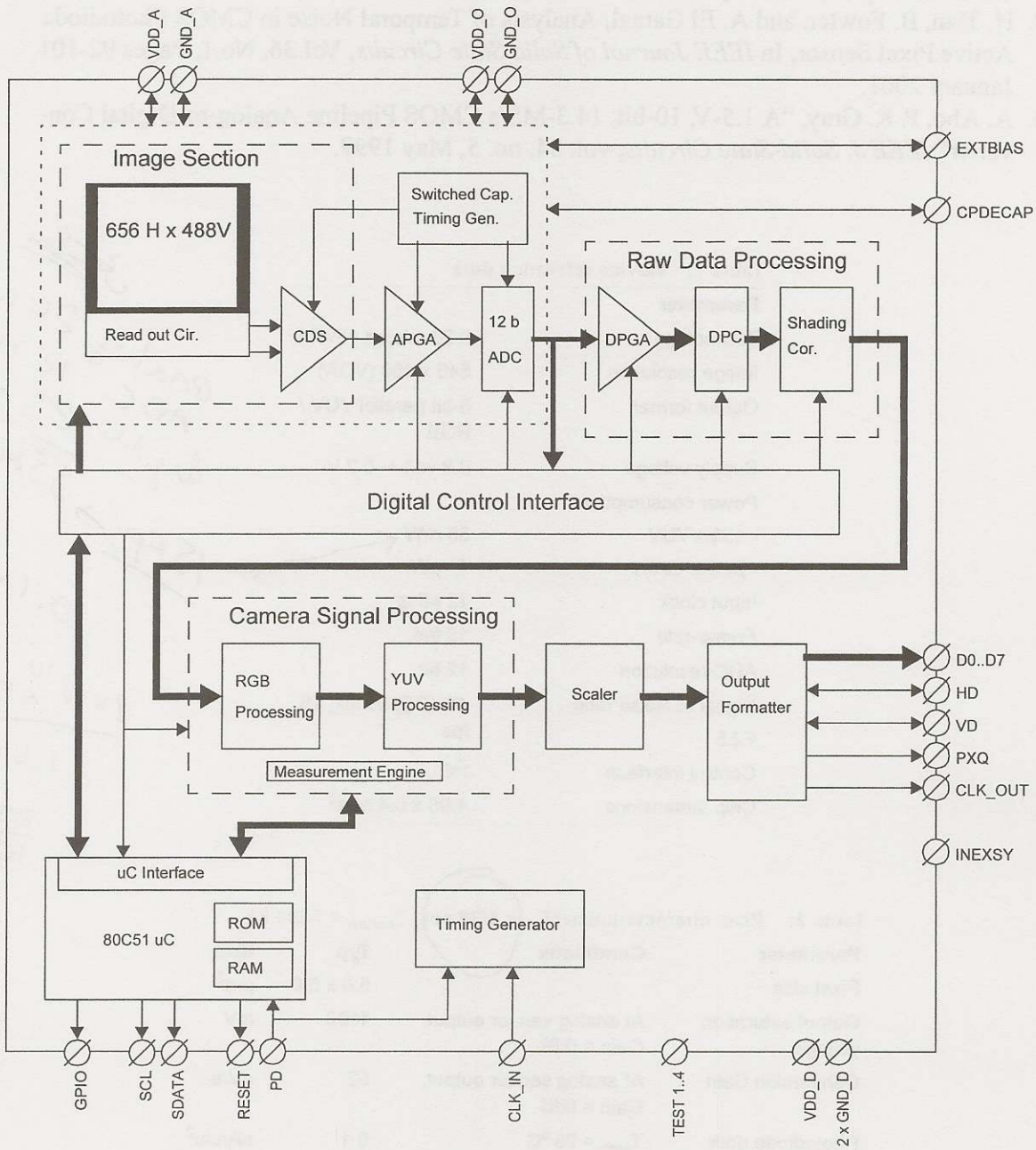

Figure 1 : Device architecture

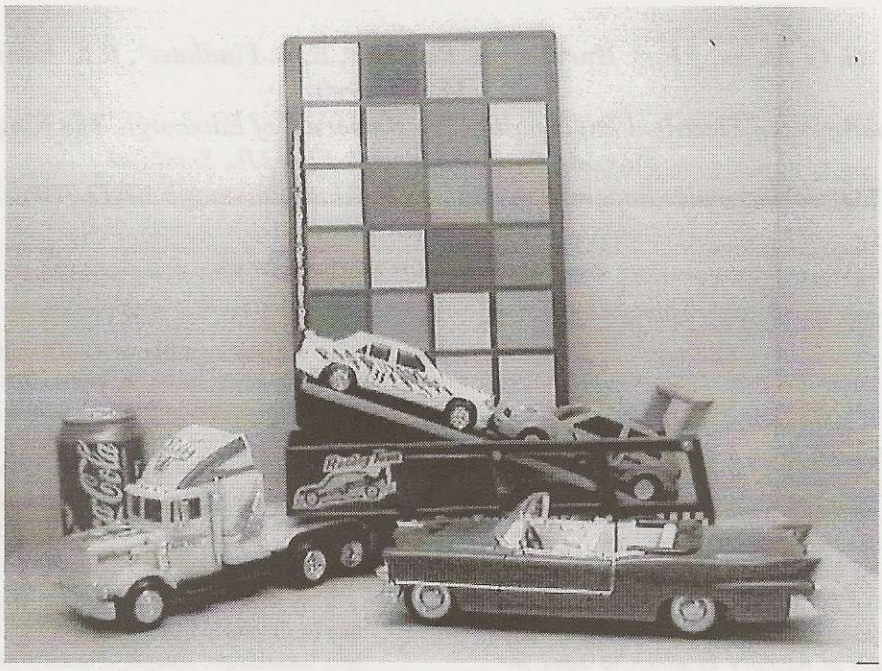

Figure 2 : Captured image from the sensor