Low Power Two-Chip Image Sensor Solution for High-End Scientific Applications

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ABSTRACT

A high performance imaging system consisting of a CMOS-based hybrid imager and a fully programmable control and digitization ASIC is presented. The extremely low noise imager offers 2k x 2k pixels at frame rates up to 80 Hz. It can be used for visible as well as infrared applications by selecting the appropriate detector material. Especially for astronomy applications, the sensor features the so-called guide mode which enables star tracking during both the integration and readout phases. The additional companion ASIC performs all functions necessary to operate the imager. It provides the required clocks, biases and power supplies to the sensor and, at the same time, receives the analog sensor output and converts it to digital data. As a consequence, the interface to the user is completely digital and therefore robust against any possible signal-to-noise degradation.

1. INTRODUCTION

The trend for CMOS-based image sensors has been to integrate more and more functionality on the sensor itself in order to achieve low power and compact imaging systems on chip (iSoC). This approach has been succesfully demonstrated by various iSoCs which, as a bare minimum, include timing control and A/D conversion, but often comprise additional sophisticated image processing functionality [1,2,3]. However, although the system-on-chip approach leads to user-friendly and compact image sensor solutions, it can be of limited use for very high-end applications. Some of the reasons are power consumption restrictions at the sensor, possible yield reduction, electrical or optical crosstalk, non-optimal digital performance due to large feature size of the CMOS imager process or simply area restrictions.

We present a two-chip imaging system consisting of a 4 Megapixel focal plane array and a supporting control ASIC optimized for astronomical sensors [4]. The focal plane array is a so-called hybrid detector comprising a CMOS-based readout chip and a visible or infrared detector array. The hybrid approach results in high detector quantum efficiency and close to 100% fill factor while, at the same time, offering the complete pixel area for CMOS circuitry. The architecture and the performance of this imager (called HAWAII-2RG) are described in Section 2.

Traditionally, such imagers are operated using controllers made of discrete electronics. Our approach eliminates most of the external electronics by combining control logic, bias generation and A/D conversion in a single companion chip. This chip, called SIDECAR for System for Image Digitization, Enhancement, Control And Retrieval, is a fully programmable microcontroller-based system comprising multi-channel clock and bias generation as well as 36 channels of 16-bit (500 kHz) and 12-bit (10 MHz) ADCs. The SIDECAR ASIC is described in Section 3.

2. HAWAII-2RG HYBRID IMAGER

The HAWAII-2RG imager is a 4 Megapixel CMOS readout circuit that can be mated to visible or infrared detector arrays using a special bump-bonding technique [5]. The basic block diagram including the pixel array, the column buffers and the fast and slow scanners is shown in Fig. 1. All I/O pads are located at the top in order to open the door for larger arrays comprised of several 2k x 2k sensors. The block

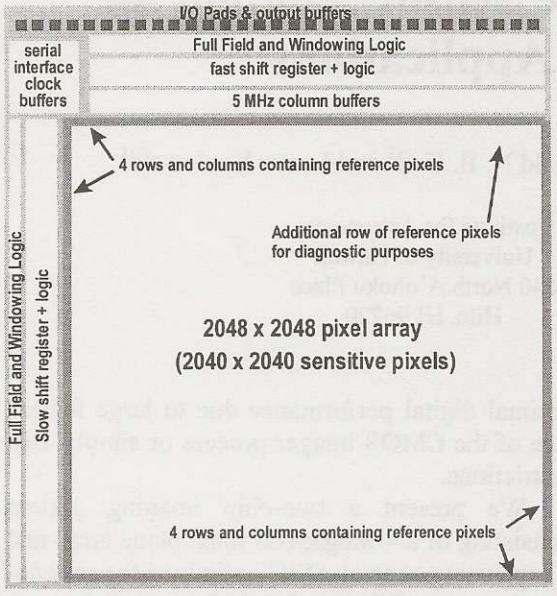

Figure 1: HAWAII-2RG block diagram.

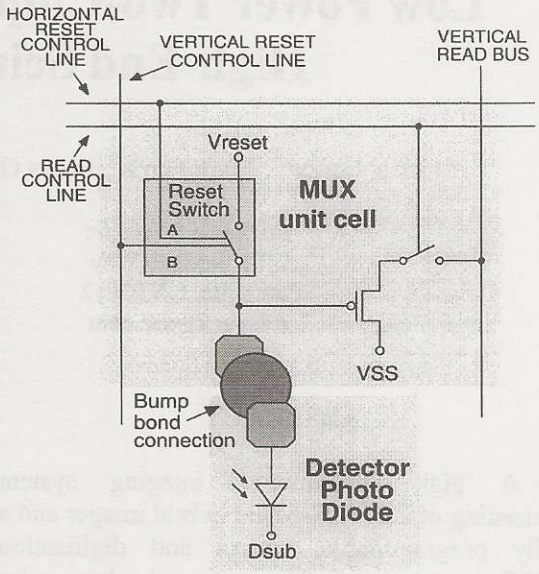

Figure 2: Pixel schematic diagram.

Figure 3: Example Image for Guide Mode Operation

diagram also identifies four rows of reference pixels surrounding the array. They serve as baseline references for signal drift due to temperature or bias voltage variations.

The pixel, which is shown in Fig. 2, follows the basic 3-transistor active pixel architecture with the exception of a more complex reset circuitry. The implemented reset configuration not only enables global and line-by-line reset schemes, but also offers the option of single pixel reset. Combining the single pixel reset with the imager's windowing capability results in a unique operating mode which can be used for telescope guiding in astronomical application. It allows the user to read and reset a subwindow independently of the remaining pixels in the full field. As a consequence, one can read a small guide window at a high frame rate seamlessly interleaved with non-destructive readout or while performing long integrations with the full field detector array.

An example for the operation of a 16 x 16 guide window using a HgCdTe infrared detector can be seen in Fig. 3. The image is obtained by first resetting and reading the full array, then resetting and reading the small window in the center 5000 times and finally reading the full field again. The displayed image is the difference between the second and the first read (true CDS) and therefore shows no kTC noise. Since the sensor was not illuminated, the image is characterized by the dark current distribution of the detector array. The important result to note is, that there is no crosstalk from the subwindow or its corresponding rows or columns into the rest of the array. We have performed experiments interspersing a 16 read – reset – 16 read sequence on an 8x8 subwindow between readout of each 8 lines of the full array (a 32Hz update rate) with no effect on the full frame data.

Table 1 summarizes the important sensor properties and measurement results. In the slow scientific readout mode (100 kHz per channel), it provides a linear dynamic range in excess of 80 dB and a CDS read noise of 12e-. Sixteen

multiple non-destructive reads reduce the noise to levels below 4e-. Fig. 4 shows a fully functional packaged HAWAII-2RG which covers an area of approx. 16 cm². It is designed in a 0.25 µm CMOS process using a special stitching technique which composes the imager of several independent exposures.

Table 1: HAWAII-2RG Characteristics

Resolution	2048 x 2048 pixels
Pixel Size	18 x 18 µm²
Die Dimension	40 x 39 mm²
Technology	0.25 µm CMOS, stitched
Output Channels	1, 4 or 32 selectable
Readout Speed	100 - 500 kHz / 5 - 10 MHz selectable
Power Dissipation	300 µW per channel (slow)
Max. Frame Rate	80 frames / s
Reset Modes	Pixel-by-pixel, line-by-line & global reset
Scanning Direction	Selectable
Window Mode	Any rectangular shape
Guide Mode	Independent read & reset of full field & subwindow
Temperature range	<30 K – 300 K
Dynamic range	> 80 dB
Full-Well	Detector dependent, typically 60 to 200 ke- for HgCdTe
Read Noise	<12 e- CDS (~ 40 µV) <4 e- using 16 multiple samples
Dark Current	< 0.004 e-/s for HgCdTe (5µm cutoff) at T < 45 K

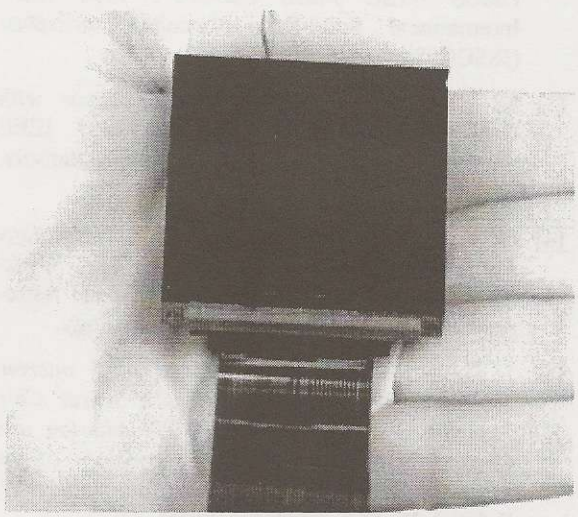

Figure 4: Fully functional packaged HAWAII-2RG

3. SIDECAR CONTROL ASIC

The SIDECAR ASIC represents a fully programmable control and digitization system for analog image sensors. It can be placed close to the sensor, even on the same package, thus minimizing power consumption due to smaller capacitance and potential noise pickup on the analog signal lines. The basic architecture can be divided into the following major blocks: analog bias generator, analog to digital converter, digital control and timing generation, data memory/ processing, and digital data interface (Fig. 5).

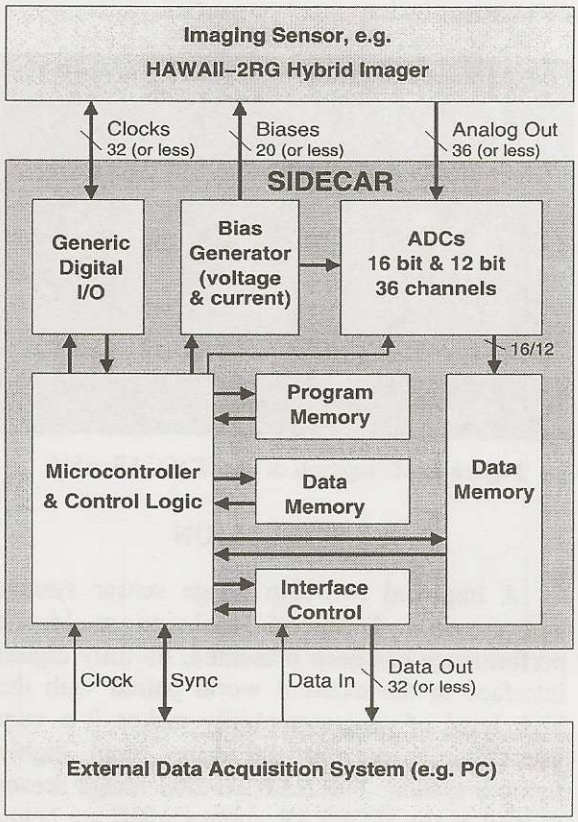

Figure 5: Simplified block diagram of the SIDECAR

The analog bias generator consists of 20 independent channels, each of which is comprised of a 10-bit digital-to-analog converter and an output buffer with adjustable driver strength. They basically represent programmable current and voltage sources. For reading out the analog detector signals, the ASIC provides 36 analog input channels. They can be digitized by on-chip ADCs offering 16-bit resolution at sample rates up to 500 kHz and 12-bit resolution at sample rates up to 10 MHz.

A fully programmable and application optimized microcontroller is responsible for the overall ASIC control and for generating the specific timing patterns of the image sensor clocks. A total of 32 digital I/O channels can be individually adjusted for driver strength and signal direction. Due to additional on-chip memory, simple data processing functions like pixel averaging or data sorting are possible. Finally, a serial and a parallel data interface are implemented to read the digitized pixel values and to program the ASIC. Fig. 6 shows a micrograph of the SIDECAR chip. Table 1 summarizes its important properties.

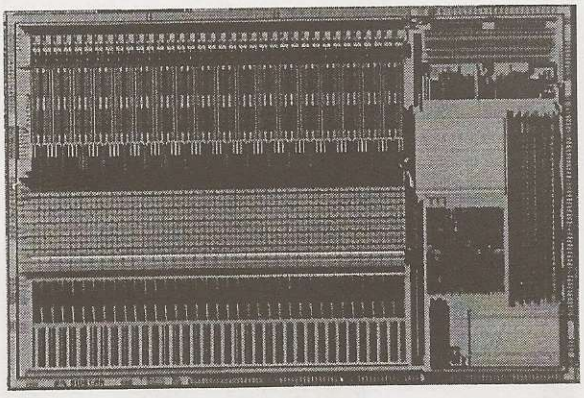

Figure 6: Micrograph of the SIDECAR ASIC

4. CONCLUSION

A high-end two-chip image sensor system that provides 4 Mpixel resolution at 16 bit performance has been presented. Its fully digital interface to the external world paired with the high level of programmability makes it a very user-friendly and, at the same time, highly flexible system. The HAWAII-2RG image sensor as well as the SIDECAR control ASIC are being considered by NASA for use in the James Webb (next generation) Space Telescope (JWST).

5. ACKNOWLEDGEMENTS

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Table 2: SIDECAR ASIC Characteristics

Die Dimension	22 x 14.5 mm²
Technology	0.25 µm CMOS
Analog Input	36 independent channels, fully differential
PreAmplifiers	Programmable gain (-3 to 27 dB) and bandwidth
16 bit ADCs	1 mW / channel at 100 kHz, up to 500 kHz sample rate
12 bit ADCs	10 mW / channel at 5 MHz, up to 10 Mhz sample rate
Bias Outputs	20 output channels, selectable voltage or current DACs
Digital I/O	32 channels,fully programmable
Microcontroller	16 bit RISC, low power, excellent arithmetic capabilities
Program Memory	16 kwords, 16 bit / word
Data Memory (µC)	8 kwords, 16 bit / word
Data Memory (ADC)	36 kwords, 24 bit / word
Arrayprocessor	Adding & multiplying and DMA control per ADC channel
Digital Interface	LVDS or CMOS, custom serial protocol, up to 32 parallel lines
Temperature range	30 K – 300 K
Radiation	Complete design is single event upset protected

5. REFERENCES

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