High-Speed Photo Line Sensors

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A bilinear line sensor with a spatial resolution of 2x2048 pixels has been developed for high-speed imaging and applications in machine vision. The sensor delivers up to 320 million pixels/s or 80'000 lines/s at the full resolution of 2x2048 pixels using 8 analog output channels. It is one of the fastest line sensors worldwide. This sensor is moreover to a large extent programmable, providing for example numerous addressing modes and the capability of defining regions of interest (ROI). The modular architecture allows the sensor to be easily adapted/scaled to other chip sizes and sensor resolutions.

The 2x2k image sensor has been manufactured in a 0.5 μm mixed-signal CMOS technology. The present paper describes the architecture of this high-speed line sensor, as well as experimental results on the electro-optical performances. Finally, further developments or potential improvements are discussed.

Keywords: *Optical line sensor; High-speed; Color line sensor; CMOS imager*

Introduction

Line sensors play a key role in numerous application fields and products, such as scanners, fax machines, spectroscopy and machine vision. The present 2x2k image sensor targets high-speed imaging in the visible and near infrared range of the electromagnetic spectrum. Typical applications can be found in machine vision, for example quality control and high-throughput document scanning systems. High-speed line image sensing is an active field of research and development. Worldwide the fastest line imagers reach up to 40 Mpixels/s [1], 60 Mpixels/s [2], or even 100 Mpixels/s [3].

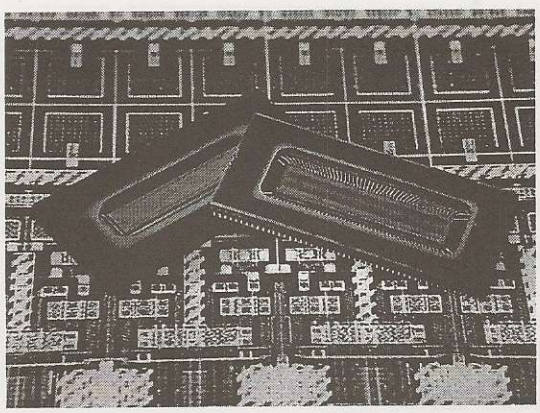

Figure 1: Micrograph of packaged 2x2k sensor (in front)

The present 2x2k imager delivers up to 320 Mpixels/s, corresponding to a line rate of 80 kHz at the full spatial resolution. Defining smaller regions to be read-out allows the line rate to be further increased. The 2x2k sensor is based on a massively parallel architecture and an optimal use of the available light, thanks to an on-chip frame storage allowing the concurrent integration and read-out of the optical information: during integration or the exposure time the data acquired in the previous frame is read-out.

Sensor Architecture and Design

The present optical line sensor was targeted for high-speed applications of up to 320 Mpixels/s, corresponding to a frame rate of more than 80'000 frames/s at the full resolution of 2x2048 pixels. Therefore, special attention has to be paid to the architecture of the sensor in order to guarantee the very-high data throughput and the correct operation at the analog output interface. In particular, there are two crucial issues that have to be addressed in such demanding environments: sufficient speed of the data path and an integrate-while-readout capability of the sensor. Both of these requirements were considered for the present design. In the following we will describe the basic architecture of the 2x2k sensor before discussing some special features and design issues of the sensor.

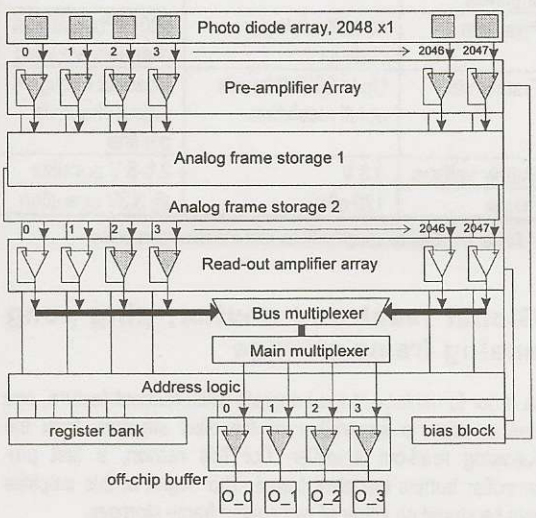

Figure 2: Architectural block diagram of a single line of the 2x2k sensor. Active elements are shown in gray.

The complete sensor consists of two identical sensor lines with 2048 pixels each. Figure 2 depicts the architecture of one of these two optical sensor lines. The chosen approach mainly

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consists in successively merging the analog signals from a massively parallel input layer into an output layer with up to 4 analog output channels. A single sensor line is formed by the 2048x1 photo-diode array, whose pre-amplified output signals feed into either of two analog storage banks. The two analog frame-storage memory banks enable the integrate-while-readout feature, i.e., the continuous operation at very-high speeds. Then, the two storage banks are connected to an array of read-out amplifiers through a 2-to-1 analog multiplexing array. The read-out amplifiers distribute their signal onto a 16-channel analog bus, which is afterwards multiplexed down to the 4 output channels by an analog multiplexing block. The output pads are finally driven by a set of 4 analog buffers. In addition to the analog signal path there are registers, holding the address of the current and the pre-selected blocks of read-out amplifiers as well as the analog biasing circuitry on the chip. The main device specifications and electrical properties of the 2x2k sensor chip can be found in Table 1.

Description	Value	Comment
Architecture	2 lines with 2048 pixels each	Designed as a 3-stage APS with electronic shutter
Imager size	4.46 x 19.8 mm²	
Pixel count	2x2048	
Pixel size	6.5x6.5 µm²	Sensitive area
Pixel pitch	9.5 µm	
Full well cap.	>490'000 e⁻	Programmable
Output channels	1-4 per line	
Pixel rate	40 MPixels/s per channel	320 MPixels/s if all channels are used
Frame rate	Up to 80'000 lines/s at full resolution	Readout through 4 output channels per line
Supply voltage	3.3 V	2.6-5 V possible
Power	170 mW	@ 3.3V operation

Table 1: Device specifications and electrical properties

Global reset and shutter, ping-pong analog frame storage

In order to implement the integrate-while-readout feature, one has to allow a separation of the pixel structure from the following read-out amplifier. For this reason, a first pre-amplifier buffers the pixel signal. The output of this amplifier can be stored on either of two analog frame storages.

The analog storage banks are built as a ping-pong style sample-and-hold (S/H) circuit as shown in Figure 3 [4]. During the sampling operation onto one of the two storage capacitors, the read-out amplifiers are connected to the other storage capacitor. The selected read-out amplifiers then pass the buffered signal to the intermediate 16-channel wide analog bus.

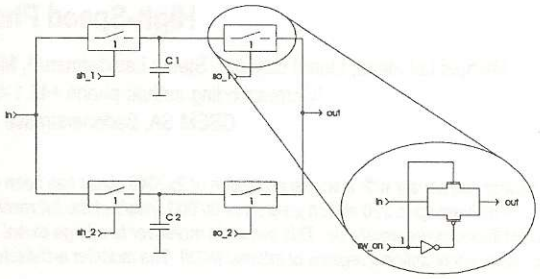

Figure 3: Schematic of the double analog frame storage

The integration period is equally long for each pixel: the reset signal is applied in parallel on all pixels and toggling from the sample mode to the hold mode in the ping-pong S/H is also initiated at the same time for all pixels. By doing so, a global-shutter mechanism is implemented. It has the advantage that no geometrical distortion can arise from the sampling process. Figure 4 shows a rough sketch of the control-signal timing at the sensor level.

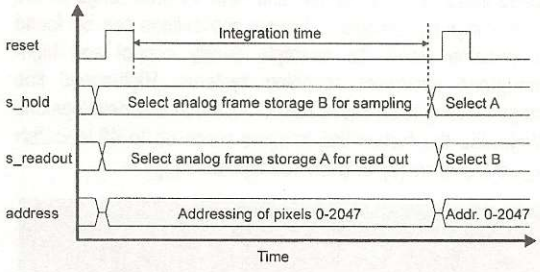

Figure 4: Timing diagram showing the concurrent integration and read-out of the sensor

Parallel read-out data path

The second key to successful implementation of high-speed sensors is the ability to read out the data quickly enough. Usually, this can be accomplished by using a massively parallel approach in the data-path architecture. This considerably relaxes the speed requirements for the different amplifier stages.

The present sensor design can handle speeds of up to 320 MPixels/s or 160 MPixels/s per line, respectively. Each line consists of 2048 pixels, which results in the 80'000 kframes/s output rate. So the pixel pre-amplifiers must be able to handle a maximum speed of 80 kPixels/s. This seems to be quite low, but the amplifiers have to match the pixel pitch of 9.5 µm. Furthermore, all amplifiers operate in parallel and therefore consume a considerable amount of power. Hence, there are still some challenges in the design of these pre-amplifier stages.

Following the ping-pong S/H stages we encounter the read-out amplifiers. Here a total of 16 out of the 2048 amplifiers per side are active at the same time. For power saving reasons, all the others are switched off. They are controlled by a selection signal of the address logic and hence act also as a 2048-to-16 multiplexer. Therefore, these amplifiers have to handle a

speed of 160 MPixels/s divided by 16, resulting in 10 MPixels/s.

The outputs of the 16 active read-out amplifiers are multiplexed to four off-chip buffers. The speed requirement is therefore again increased by a factor of four, resulting finally in the 40 MPixels/s per channel.

Because the output buffers are located in the center of the chip, a novel architectural approach is used to scale down the requirements for the read-out amplifiers. Instead of spreading the intermediate analog bus over the complete length of the sensor line of about 20 mm, which would result in an enormous capacitive load for these amplifiers, it is split into a left and a right half bus. A bus multiplexing stage selects therefore either the left or right half-side bus and passes it to the main multiplexing stage. By doing so, the parasitic capacitance of the bus line as well as the number of inactive read-out amplifiers with their output capacitances is cut by a factor of two.

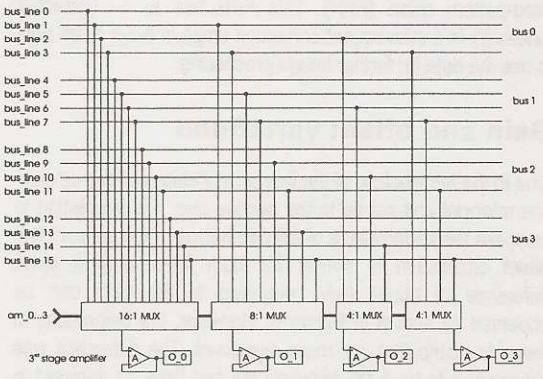

Figure 5: Output-channel multiplexing stage

Another novel approach is also included in the main multiplexing stage allowing lower costs for systems having lower speed requirements. As shown in Figure 5, only the off-chip buffers two and three exhibit the 4:1 multiplexers described above, whereas the off-chip buffer one is preceded by an 8:1 multiplexer and the off-chip buffer zero preceded by a 16:1 multiplexer. This allows the sensor to be readout with only two or even one channel per line. The maximum pixel rate per channel remains at the same level, i.e., the maximum pixel rate of the whole sensor is still either 160 MPixels/s when using two channels per sensor line or 80 MPixels/s using only one channel per sensor line. For the further digital signal processing, only four or even two high-speed A/D converters are required, thus lowering the costs of the system significantly. The whole circuit can also be run at lower clock rates, making the sensor useful for applications with even lower requirements. One can also think of applications in which the sensor has to be synchronized to some other modules, e.g., to a conveyor belt.

Adjustable full-well capacity

The optically active pixel consists of an n-well/p-substrate photodiode. This type of photodiode proved to have the best performance features in terms of quantum efficiency, spectral sensitivity and dark current contribution in this specific 0.5 µm CMOS process.

In an active-pixel sensor (APS), the parasitic capacitance of the photo-sensitive diode is normally used directly as the integration capacitance. In the 2x2k sensor, two additional capacitances can be operated in parallel to enlarge the so-called full well capacity, i.e., the maximum amount of electrical charge that can be collected in the pixel. A large full well capacity leads to a higher shot noise limited signal-to-noise ratio (SNR); see Table 2. However note that the additional capacitances lower the sensitivity and the conversion gain of the opto-electronic sensor.

Element	Cap.	Full Well @ 2V signal	Shot noise	maximum SNR
Diode	39 fF	490'000 e^-	700 e^-	57 dB
Diode + 1st capacitance	60 fF	755'000 e^-	870 e^-	59 dB
Diode + 2nd capacitance	81 fF	1'000'000 e^-	1'000 e^-	60 dB
Diode + both capacitances	102 fF	1'300'000 e^-	1'140 e^-	61 dB

Table 2: Maximum full-well capacity and SNR versus the input capacitance of the sensing node

Flexible control schemes

CDS stage

All the control signals and the addressing signals are provided through the pads. This allows for a very flexible use of the sensor in many different circumstances. For example, one of the analog frame-storage blocks can be used to latch the reset value of the pixel. While the pixels are integrating the incoming light, this reset value can be read-out and stored in the digital signal processing (DSP) part of the imager system. When the optical integration process is finished, the externally latched reset values can be subtracted directly from the pixel signal. This algorithm implements the correlated double sampling (CDS) as an off-chip process. For lower-speed applications the CDS algorithm will eliminate reset noise (kTC-noise) and fixed pattern noise (FPN), as well as to a large extent flicker (1/f) noise[5].

High dynamic-range operation

For applications requiring a high dynamic range (DR), the two analog frame storage blocks can be used to implement a 'one-step, dual-integration' function, i.e., two different integration times without the need to capture two completely different frames: After the reset phase and a first integration period of, e.g., 10 µs the current value is stored in the first analog storage bank. While this first integration step is read out, the pixels are integrating further and after the second integration period with a total of, e.g., 100 µs the final value is stored in the second analog frame storage. During the reset phase of the pixels and during the start of the subsequent short integration period, the signal of the second, longer integration

period can be read out. This extends the DR by the ratio between the two integration periods, in this example by a factor of 10 or 20 dB, respectively.

Flexible addressing and regions-of-interest

The addressing of the pixels is also directly controlled through the accessible pads. This allows additional flexibility within the read-out modes. For example, depending on the application in mind, the pixels can be read out from left to right or from right to left.

Furthermore, the sensor has not necessarily to be read out as a whole. Regions-of-interest (ROI) can be defined with a granularity of 4 pixels, i.e., the sensor could be read out from pixel 256 to pixel 495. A settling time of only 0.3µs is required, corresponding to 12 pixel clocks with a pixel rate of 40MPixels/s, before the read out of a new line can start. For example, if only a quarter of the sensor is read out, frame rates up to 320 kframes/s can be achieved. Using the flexible addressing modes of the sensor, it is even possible to define multiple ROIs.

Sensor Implementation

The sensor was designed in a standard 0.5 µm CMOS process with three metal layers and double poly for poly-poly capacitances. Eldo Spice simulations of the complete analog data path as well as the digital glue logic were carried-out using BSim3v3 transistor models in the Mentor design environment.

The layout was designed in a completely modular fashion. The maximum mask reticle size that the foundry could handle is 20 mm in both directions and thus limited the number of sensor elements in one direction. The reticle size was utilized almost perfectly: With a pixel pitch of 9.5 µm, the 2048 pixels of the present sensor span almost 19.5 mm in width. The photodiode itself was designed as an n-well in the p-substrate. The design rule between neighboring n-wells is 3 µm, so the active pixel area was drawn as a square with 6.5 µm sides . The pixel pre-amplifier and the ping-pong S/H stages match the pixel pitch of 9.5 µm in order to create a very compact layout.

After fabrication at the silicon foundry, the dies were bonded into a custom-made 98-pin glass lid array (GLA) constructed from polymer laminate materials. This allows for high-density interconnects, thermal matching to the PCB, and for low non-recurring engineering (NRE).

Measurement results

The actual sensor was characterized in the radiometric measurement laboratory of CSEM in Zurich. Standard parameters of optical sensors such as sensitivity, signal swing, dynamic range, saturation exposure, fixed pattern noise and power consumption were extracted from the measurements. These results are summarized in Table 3.

Opto-electrical properties	Value	Comment
Spectral range	400 to 900nm	
Sensitivity	9 V/µJ.cm^{-2}	@ 626 nm
Voltage swing	1.7 V	Output voltage range of the sensor
Dynamic range	63 dB	
Saturation exposure	0.175 µJ/cm^2	@ 626 nm
Fixed Pattern Noise	27 mV or 1.6 %	rms value
Temporal Noise	1.2 mV or 0.07 %	rms value

Table 3: Measurements of the opto-electrical properties of the 2x2k sensor

The main observation of the in-depth analysis of the characterization results is that the missing double sampling signal chain in the sensor architecture leads to a relatively high fixed-pattern noise (FPN). This FPN has to be corrected externally in a subsequent correction stage in order to be able to use the data for further image processing.

Gain and offset variations

Due to the architecture of the line sensor chip with one sensor-line mirrored and paired to the second one, it is interesting to compare the performance of the two halves of the sensor: The offset distribution is similar for both lines; only a small difference of about 4mV compared to the FPN can be observed as shown in Figure 6. However, the differences in the gain distribution are more significant. The difference was determined to be 1.4% between the two lines as depicted in Figure 7. These results can be explained by different sense node capacitances due to the different orientation of the elements.

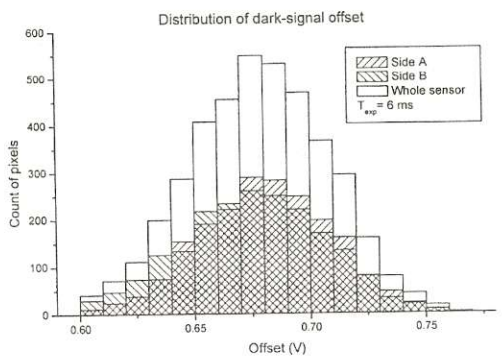

Figure 6: Offset distribution of the two sensor lines of the 2x2k line sensor

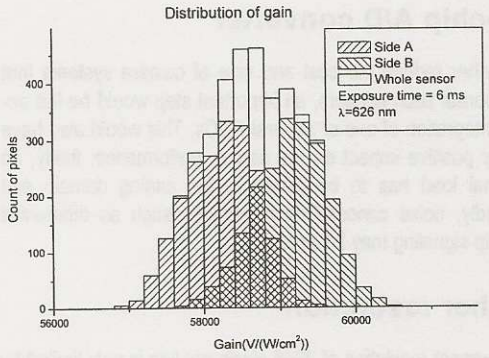

Figure 7: Gain distribution of the two sensor lines of the 2x2k line sensor

Figure 8 provides another interesting view of the sensor performance. In this representation, the pixels are shown with respect to their position. The distortion in offset and gain is coded with different gray levels. In places where the offset distribution is relatively uniform over the sensor area, the gain distribution diagram clearly shows that the pixels in the middle part of the sensor have slightly higher gains than the ones on either end of the sensor. The difference in the gain between the two sides is also visible.

Such diagrams can help in understanding layout problems, e.g., an asymmetric distribution of gain or offset may show a problem in the power routing. In this specific sensor, the distributions are within the expected tolerances, which prove the layout to be adequate.

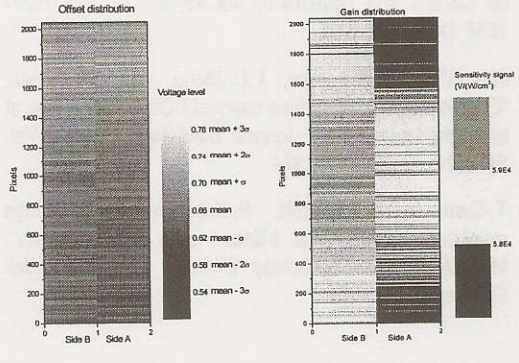

Figure 8: Offset (left) and gain (right) distortion with respect to the respective pixel position

Temperature dependency

The amount of dark signal is very much dependent on the temperature of the optically active silicon die. Since the radiometric measurement laboratory of CSEM is also equipped with a temperature chamber, the dependency of the dark signal with respect to the temperature was measured. The results of this investigation are plotted in Figure 9. This plot clearly shows that the temperature at which the dark signal becomes significant depends on the integration time. With an integration time of 6 ms, the dark signal becomes non-negligible when reaching temperatures higher than 60°C. But since the normal integration time for this high-speed line sensor will be in the range of a few microseconds, i.e., continuous read-out at 80'000 kframes/s allows a maximum integration time of about 10µs, the dark current will have no influence on the photo-generated sensor signal. From Figure 9 a doubling of the dark signal for every 7.5°C is extracted, which matches the theoretical value well.

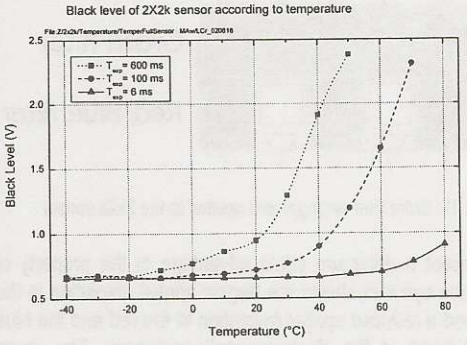

Figure 9: Dark signal with respect to temperature for various integration times

Adjustable full-well capacity

The effect of the adjustable full-well capacitance on the output signal sensitivity is shown in Figure 10. On the one hand, it can be clearly seen that the amount of charge being collected is increased with additional capacitances added to the sensitive node. On the other hand, the sensitivity of the output signal is decreased by the additional capacitances on the sensing node.

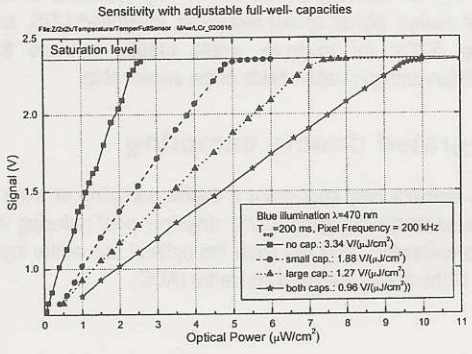

Figure 10: Sensitivity measurements with adjustable full-well capacitances

Color applications

Many applications call for color information to be extracted from the sensed image. The application of dielectric color filters was considered from the beginning of the design for this high-speed line sensor. The basic idea behind the specific arrangement of the pixels was to use the first line with a green color filter and the second line with an alternating blue/red color pattern; see Figure 11. With this kind of arrangement, we obtain the full information of the green channel for every pixel, whereas the blue and red information is only available on every second pixel. The full color information has to be interpolated, and therefore it has a slightly lower resolution [6].

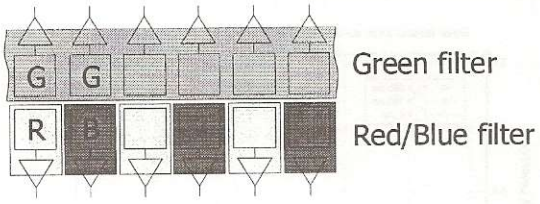

Figure 11: Color filter arrangement applied to the 2x2k sensor

The present architecture takes advantage of the property of the human eye that shows the largest spatial resolution in the green and a reduced spatial resolution in the red and the blue spectral band of the electromagnetic spectrum. The green pixels provide the information on luminance (brightness) at the full spatial resolution of 2048 pixels, whereas the alternating red and blue pixels provide chrominance information at smaller resolution. With this unique architecture, the color performance will be comparable to tri-linear CCD scanner lines.

Conclusions and Outlook

In this article we have presented a high-speed 2x2048 pixel line-sensor design that operates at speeds of up to 320 Mpixels/s. The sensor was designed and fabricated in a standard 0.5 µm CMOS semiconductor technology. Measurement results showed excellent performance in terms of speed as well as application-specific flexibility. In the near future we will concentrate on further improvements of the current design: higher spatial resolution, integrated CDS, and on-chip ADCs, for example, would greatly enhance the capabilities and application fields of the sensor chip.

Integrated double sampling

Future sensors may implement a double sampling or even a correlated double sampling (CDS) stage per pixel reducing the FPN considerably. This will allow the optimal use of the input range of the analog-to-digital converter (ADC).

On-chip A/D converter

To further reduce the cost and size of camera systems that incorporate such sensors, an important step would be the on-chip integration of one or several ADCs. This would also have a very positive impact on the sensor performance: firstly, no external load has to be driven in the analog domain and secondly, noise cancellation techniques such as differential on-chip signaling may be used.

Higher resolution

The present resolution of 2048 pixels per line is only limited by the reticle size of about 22 mm for the selected technology.. However the equipment of the foundries is changing constantly and in the near future we may have the possibility to produce significantly larger integrated circuit chips even without reticle stitching. As mentioned before, the concept of the presented sensor is completely modular and can be applied also to longer sensor lines. Therefore, combined with larger reticle sizes or stitching, it will allow the production of line sensors with for example a resolution of 4096 pixels or even higher without any change in the concept of the sensor.

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